

High Current Bias Resistor Transistor

PNP Silicon

Features

- Collector–Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 30 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain –
 $h_{FE} = 125 \text{ (Min) @ } I_C = 0.8 \text{ Adc}$
 $= 90 \text{ (Min) @ } I_C = 3.0 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.275 \text{ Vdc (Max) @ } I_C = 1.2 \text{ Adc}$
 $= 0.55 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- SOT-223 Surface Mount Packaging
- ESD Rating – Human Body Model: Class 1B
– Machine Model: Class B
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CB}	45	Vdc
Emitter–Base Voltage	V_{EB}	± 6.0	Vdc
Base Current – Continuous	I_B	1.0	Adc
Collector Current – Continuous – Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material	P_D	3.0 24 1.56 0.72	W mW/ $^\circ\text{C}$ W W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to $+150$	$^\circ\text{C}$

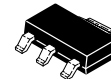
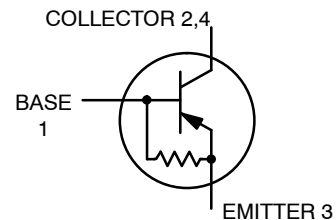
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



ON Semiconductor®

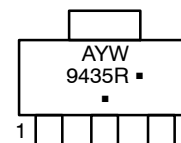
<http://onsemi.com>

POWER BJT
 $I_C = 3.0 \text{ AMPERES}$
 $BV_{CEO} = 30 \text{ VOLTS}$
 $V_{CE(sat)} = 0.275 \text{ VOLTS}$



**SOT-223
CASE 318E
STYLE 1**

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
9435R = Device Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSB9435T1G	SOT-223 (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSB9435T1G

THEMAL CHARACTERISTICS NSB9435T1G 热阻

Characteristic	Symbol	Value	Unit
Thermal Resistance			°C/W
Junction-to-Case	$R_{\theta JC}$	42	
Junction-to-Ambient on 1" sq.(645 sq. mm) Collector pad on FR-4 board material	$R_{\theta JA}$	80	
Junction-to-Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 board material	$R_{\theta JA}$	174	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 s	T_L	260	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 10 \text{ mAdc}$, $I_B = 0 \text{ Adc}$)	$V_{CE(sus)}$	30	–	–	Vdc
Emitter-Base Voltage ($I_E = 50 \mu\text{Adc}$, $I_C = 0 \text{ Adc}$)	V_{EBO}	6.0	–	–	Vdc
Collector Cutoff Current ($V_{CE} = 25 \text{ Vdc}$) ($V_{CE} = 25 \text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{CER}	– –	– –	20 200	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$)	I_{EBO}	–	–	700	μAdc

ON CHARACTERISTICS (Note 1)

Collector-Emitter Saturation Voltage ($I_C = 0.8 \text{ Adc}$, $I_B = 20 \text{ mAdc}$) ($I_C = 1.2 \text{ Adc}$, $I_B = 20 \text{ mAdc}$) ($I_C = 3.0 \text{ Adc}$, $I_B = 0.3 \text{ Adc}$)	$V_{CE(sat)}$	– – –	0.155 – –	0.210 0.275 0.550	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0 \text{ Adc}$, $I_B = 0.3 \text{ Adc}$)	$V_{BE(sat)}$	–	–	1.25	Vdc
Base-Emitter On Voltage ($I_C = 1.2 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	–	–	1.10	Vdc
DC Current Gain ($I_C = 0.8 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.2 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	125 110 90	220 – –	– – –	–
Resistor	R1	7.5	10	12.5	k Ω

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0 \text{ Adc}$, $f = 1.0 \text{ MHz}$)	C_{ob}	–	100	150	pF
Input Capacitance ($V_{EB} = 8.0 \text{ Vdc}$)	C_{ib}	–	135	–	pF
Current-Gain – Bandwidth Product (Note 2) ($I_C = 500 \text{ mA}$, $V_{CE} = 10 \text{ V}$, $F_{test} = 1.0 \text{ MHz}$)	f_T	–	110	–	MHz

1. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
2. $f_T = |h_{FE}| \cdot f_{test}$

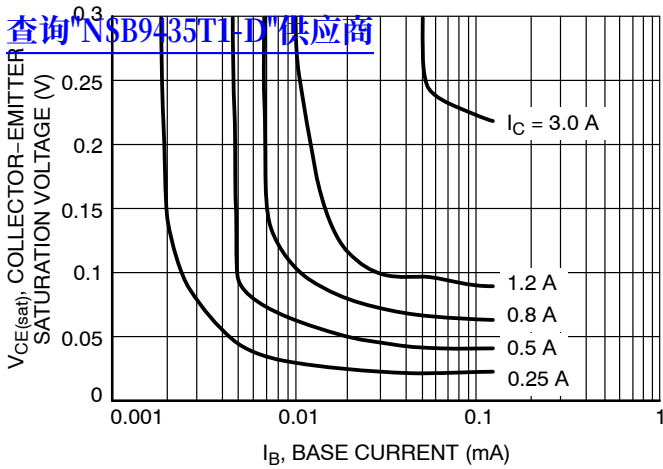


Figure 1. Collector Saturation Region

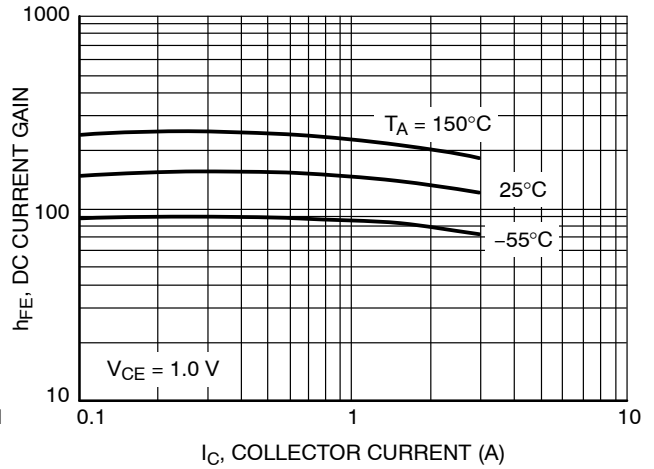


Figure 2. DC Current Gain

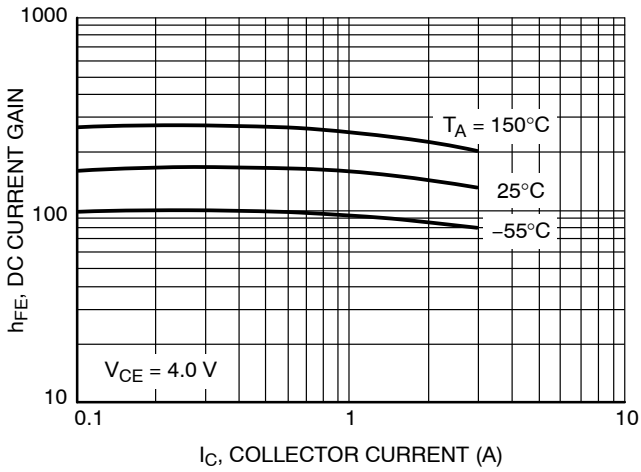


Figure 3. DC Current Gain

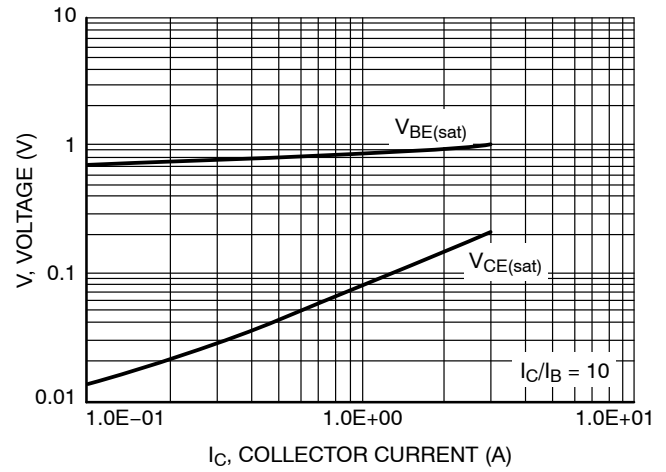


Figure 4. "ON" Voltages

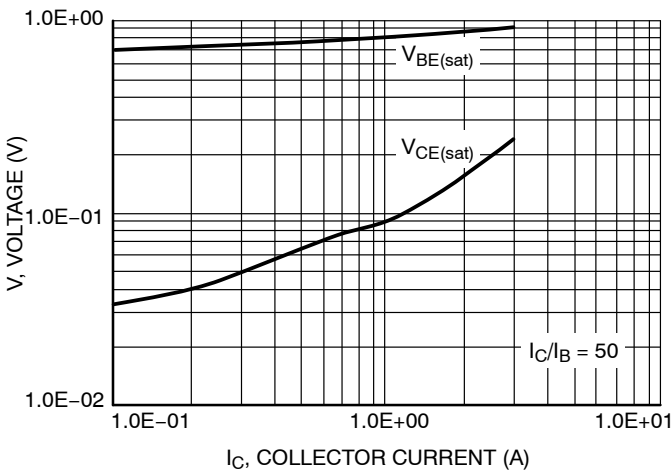


Figure 5. "ON" Voltages

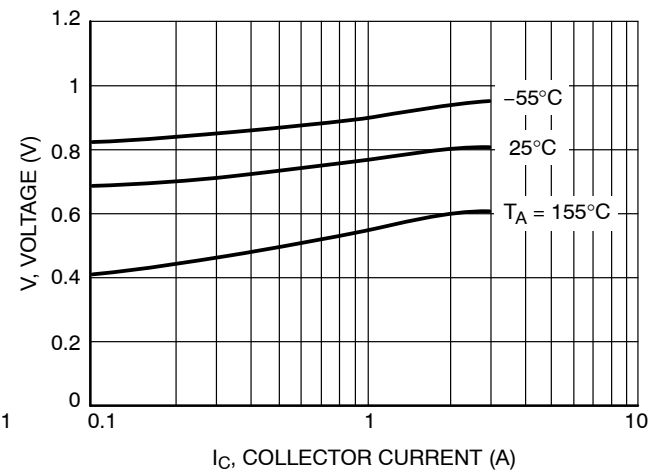
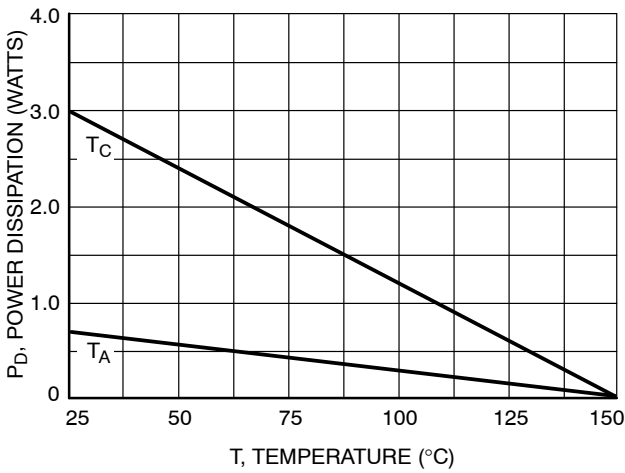
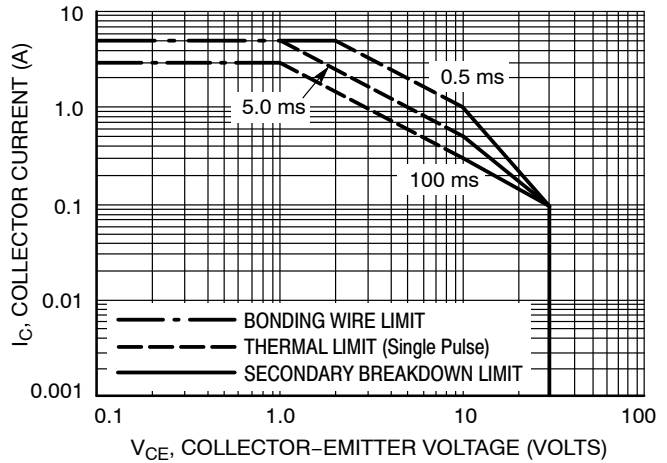
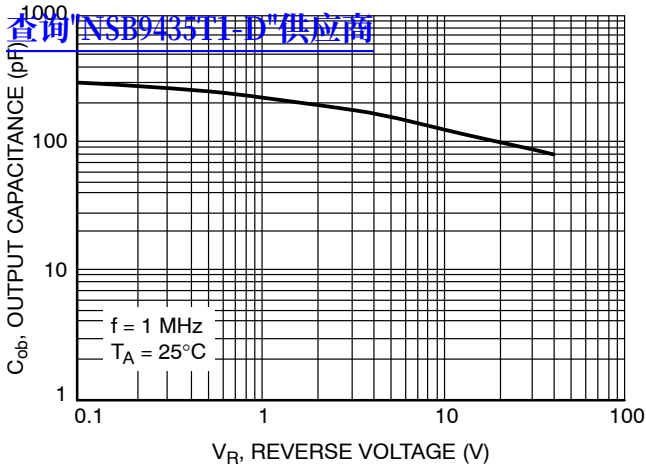
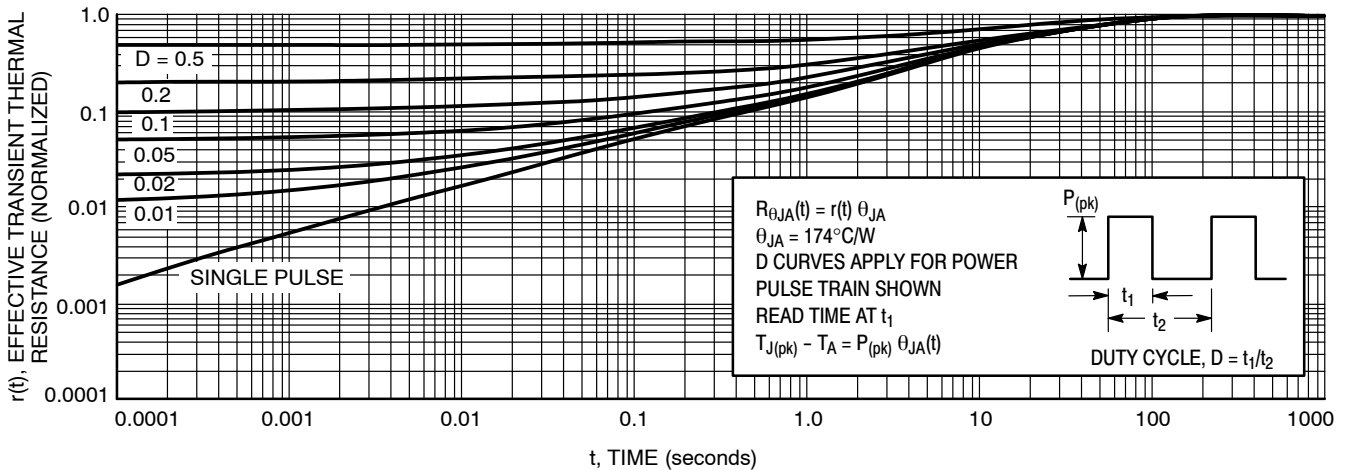


Figure 6. $V_{BE(on)}$ Voltage



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

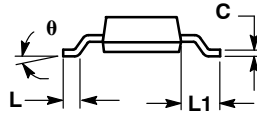
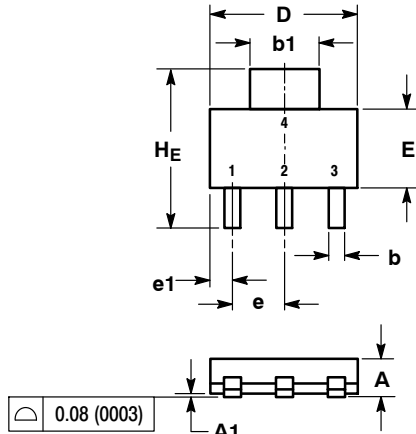


NSB9435T1G

查询"NSB9435T1-D"供应商

PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE N

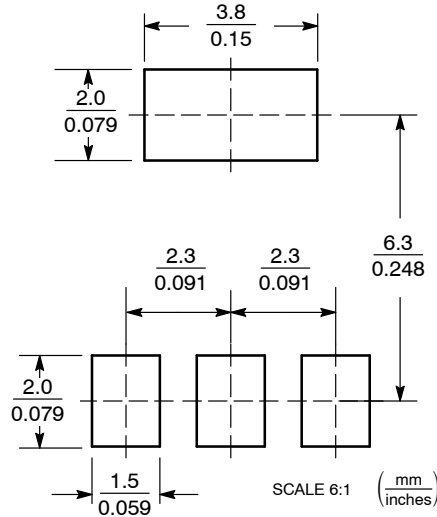


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
theta	0°	---	10°	0°	---	10°

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

NSB9435T1/D