7

DECchip 21052 Specifications

This chapter describes the mechanical and electrical specifications of the 21052.

7.1 Mechanical Specifications

The following sections describe the mechanical specifications of the 21052.

7.1.1 DECchip 21052 Package

The DECchip 21052 PCI chip is packaged in a 160-pin PQFP. Table 7–1 lists the mechanical specifications, and Figure 7–1 shows the package dimensions of the DECchip 21052.

Table 7–1 Lead Counts and Dimensional Attributes

Symbol	Limit	Dimensions in Millimeters
LL	REF	1.6
e	BSC	0.65
L	MIN	0.65
L	MAX	1.03
A	MAX	4.5
A1	MIN	0.25
A2	MIN	3.17
A2	MAX	3.67
b	MIN	0.22
b	MAX	0.38
c	MIN	0.12

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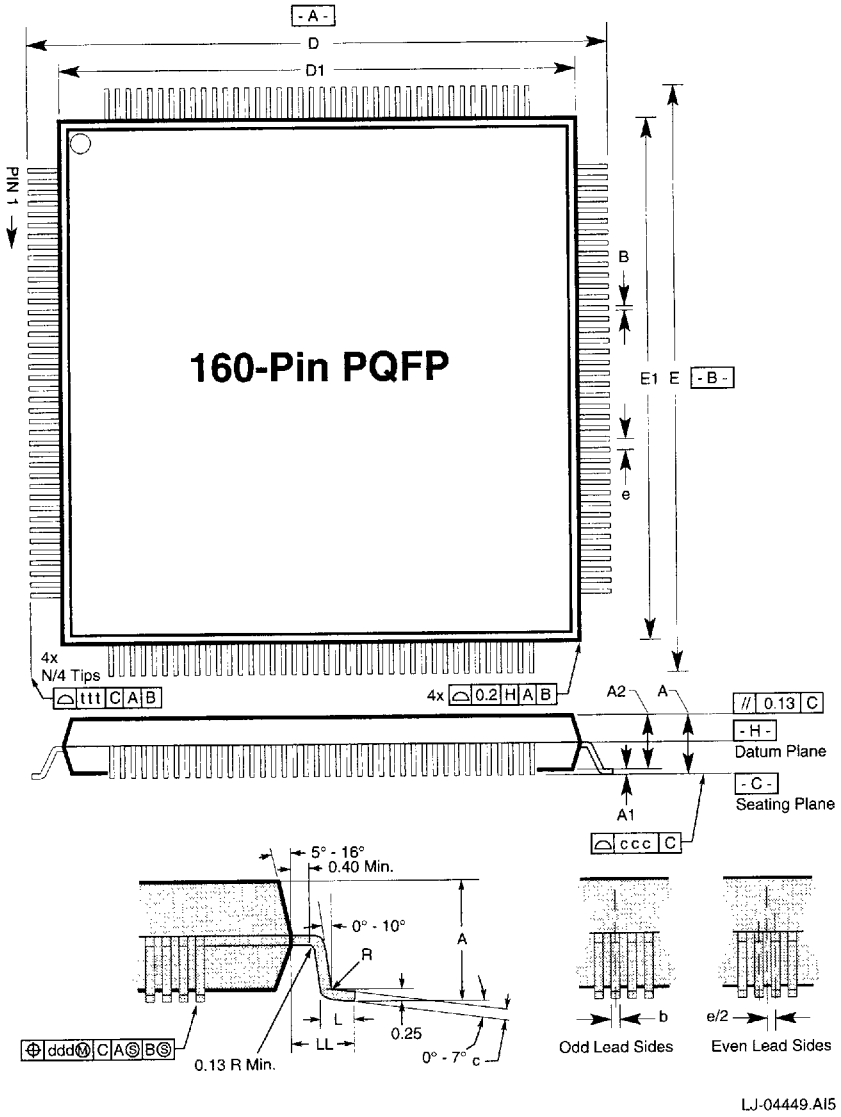
Table 7–1 (Cont.) Lead Counts and Dimensional Attributes

Symbol	Limit	Dimensions in Millimeters
c	MAX	0.23
ccc	–	0.1
ddd	–	0.13
ttt	–	0.25
D	BSC	31.2
D1	BSC	28
E	BSC	31.2
E1	BSC	28
R	MIN	0.13
R	MAX	0.3

Figure 7–1 Package Dimensions



7.1.2 Absolute Maximum Ratings

This section lists the absolute maximum ratings.

V_{DD}	3.0 V–3.6 V
T_J	100°C
T_A	70°C
P_{WC}	0.85 W
Storage temperature	–55°C to 125°C

7.2 Electrical Specifications

The following sections describe the electrical specifications of the 21052.

7.2.1 Interface Signal DC Electrical Specifications

Table 7–2 defines the dc parameters met by all 21052 signals.

Table 7–2 DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Units
V_{ih}	Input high voltage	–	.475 V_{DD}	5.5 V	V
V_{il}	Input low voltage	–	–0.5	.325 V_{DD}	V
I_{ih}	Input high leakage current[1]	V_{in} = 2.7 V	–	70	µA
I_{il}	Input low leakage current[1]	0<V_{in}<V_{DD}	–	±10	µA
V_{oh}[2]	Output high voltage	I_{out} = –500 µA	.9 V_{DD}	–	V
V_{oh5V}[3]	Output high voltage	I_{out} = –2 mA	2.4	–	V
V_{ol}[2]	Output low voltage	I_{out} = 1500 µA	–	.1 V_{DD}	V
V_{ol5V}[3,4]	Output low voltage	I_{out} = 6 mA or I_{out} = 3 mA	.55	–	V
C_{in}	Input pin capacitance	–	–	10	pF

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Table 7–2 (Cont.) DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Units
C_{IDSEL}	**p_idsel** pin capacitance	–	–	8	pF
C_{clk}	**p_clk**, **s_clk** pin capacitance	–	5	12	pF

Footnotes:

1. Input high leakage current and input low leakage current include I_{ozl} or I_{ozh} leakage current for bidirectional signals.
2. For 3.3-volt signaling environment.
3. For 5.5-volt signaling environment.
4. Most output low voltage signals have 3 mA of current. The following output low voltage signals have 6 mA of low output current:

p_frame_l	**p_trdy_l**	**p_irdy_l**	**p_devsel_l**
p_stop_l	**p_serr_l**	**p_perr_l**	**p_lock_l**
s_frame_l	**s_trdy_l**	**s_irdy**	**s_devsel_l**
s_stop_l	**s_perr_l**	**s_lock_l**	

7.2.2 Interface Signal AC Timing Specifications

Table 7–3 and Figure 7–2 show the **p_clk** and **s_clk** ac timing.

Table 7–3 p_clk and s_clk AC Timing

Symbol	Parameter	Minimum	Maximum	Units	Notes
T_{cyc}	***x*clk** cycle time	30	–	ns	–
T_{high}	***x*clk** high time	12	–	ns	@1.5 V and @1 V/ns
T_{low}	***x*clk** low time	12	–	ns	@1.5 V and @1 V/ns
	Slew rate	1	4	V/ns	0.4 to 2.4 V
T_{skew}	Delay from **p_clk** to **s_clk**	0	7	ns	@ 1.5 V

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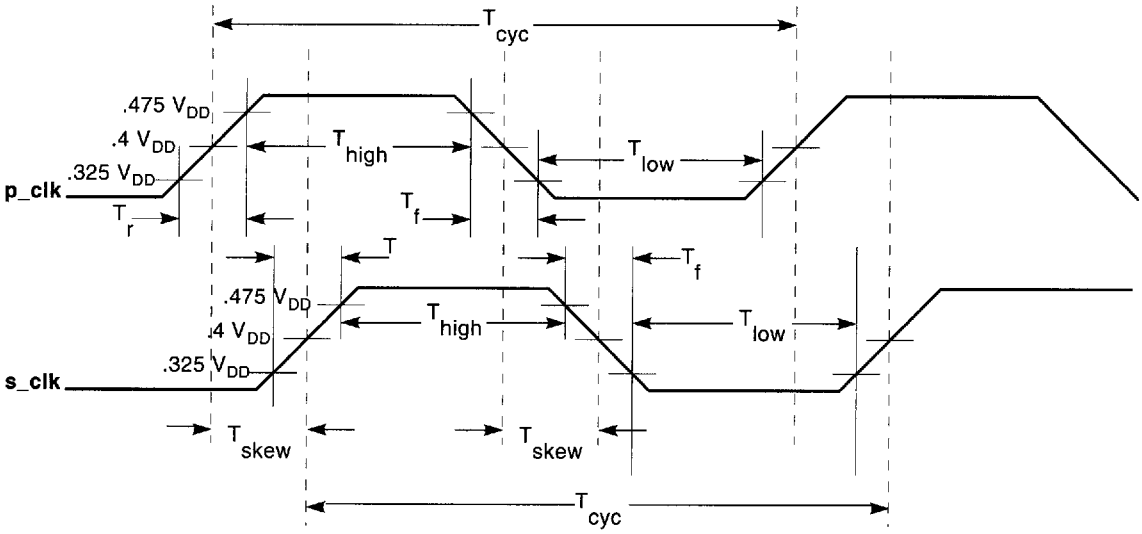
Table 7–3 (Cont.) p_clk and s_clk AC Timing

Symbol	Parameter	Minimum	Maximum	Units	Notes
T_{sclkr}	**p_clk** rising to **s_clk_ o<4:0>** rising	0	5	ns	@1.5 V[1]
T_{sclkf}	**p_clk** falling to **s_clk_ o<4:0>** falling	0	5	ns	@1.5 V[1]

[1]Measured with 30 pF lumped load.

Figure 7–2 p_clk and s_clk AC Timing



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7.2.3 Input Signal AC Timing Specifications

Table 7–4 and Figure 7–3 show the input signal ac timings, and Table 7–5 shows the timing specifications for ***x*rst_l**.

Table 7–4 Input Signal AC Timings

Symbol	Parameter	Minimum	Maximum	Units
T_{val}	***x*clk**-to-***x*signal** valid delay—bused signals[1, 2, 3]	2	11	ns
T_{val} (ptp)	***x*clk**-to-***x*signal** valid delay—point-to-point [1, 2, 3]	2	12	ns
T_{on}	Float-to-active delay [1]	2	–	ns
T_{off}	Active-to-float delay [1]	–	28	ns
T_{su}	Input setup time to ***x*clk**— bused signals[1, 3]	7	–	ns
T_{su} (ptp)	Input setup time to ***x*clk**—point-to-point[1, 3]	10, 12	–	ns
T_h	Input signal hold time from ***x*clk**[1]	0	–	ns

[1]All primary interface signals are used by **p_clk** and all secondary interface signals are used by **s_clk**.

[2]Minimum times measured with 0-pF equivalent load. Maximum times measured with 50-pF equivalent load.

[3]Point-to-point signals are **p_req_l**, **s_req_l<3:0>**, **p_gnt_l**, **s_gnt_l<3:0>**, and **s_cfn_l**.
All other PCI signals are shared.
All ***x*gnt_l** signals and **s_cfn_l** have a setup time of 10 ns.
***x*req_l** has a setup time of 12 ns.

Figure 7–3 AC Timing Waveforms

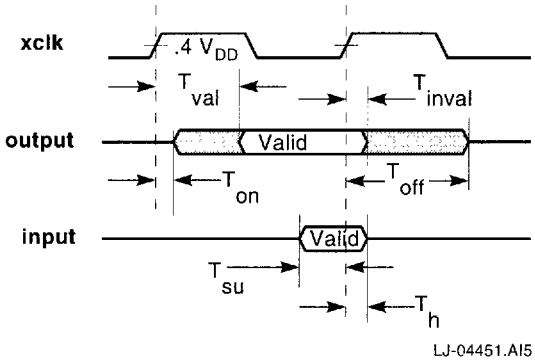

Table 7–5 *x*rst_l Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
T_{prst}	**p_rst_l** active time after power stable	1	–	µS
$T_{prst-clk}$	**p_rst_l** active time after **p_clk** stable	100	–	µS
$T_{prst-off}$	**p_rst_l** active to output float delay	–	40	ns
T_{srst}	**s_rst_l** active after **p_rst_l** assertion	–	40	ns
$T_{srst-on}$	**s_rst_l** active time after **s_clk** stable	100	–	µS
$T_{srst-off}$	**s_rst_l** active to secondary output float delay	–	40	ns