

Power MOSFET

30 V, 4.6 A, μ Cool™ Dual N-Channel,
2x2 mm WDFN Package

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88
- Lowest $R_{DS(on)}$ Solution in 2x2 mm Package
- 1.5 V $R_{DS(on)}$ Rating for Operation at Low Voltage Gate Drive Logic Level
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- DC-DC Converters (Buck and Boost Circuits)
- Low Side Load Switch
- Optimized for Battery and Load Management Applications in Portable Equipment such as, Cell Phones, PDA's, Media Players, etc.
- Level Shift for High Side Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	± 8.0	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	3.7	A
		$T_A = 85^{\circ}\text{C}$		2.7	
	$t \leq 5 \text{ s}$	$T_A = 25^{\circ}\text{C}$		4.6	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	1.5	W
	$t \leq 5 \text{ s}$			2.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	2.5	A
		$T_A = 85^{\circ}\text{C}$		1.8	
Power Dissipation (Note 2)			$T_A = 25^{\circ}\text{C}$	P_D	0.71
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	20	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode) (Note 2)			I_S	2.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

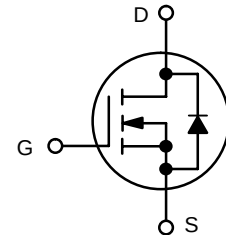
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz Cu.



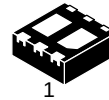
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$V_{(BR)DS}$	$R_{DS(on)}$ MAX	I_D MAX (Note 1)
30 V	70 m Ω @ 4.5 V	4.6 A
	90 m Ω @ 2.5 V	
	125 m Ω @ 1.8 V	
	250 m Ω @ 1.5 V	



N-CHANNEL MOSFET



WDFN6
CASE 506AN

MARKING DIAGRAM



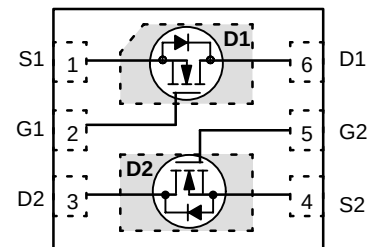
JF = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJD4116NT1G	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTLJD4116N

THEMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
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SINGLE OPERATION (SELF-HEATED)

Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	54	

DUAL OPERATION (EQUALLY HEATED)

Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	133	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

NTLJD4116N

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, Ref to 25°C		18.1		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1.0	μA
		T _J = 25°C				
		T _J = 85°C			10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8.0 V			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	0.4	0.7	1.0	V
Negative Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J			2.8		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 2.0 A		47	70	mΩ
		V _{GS} = 2.5 V, I _D = 2.0 A		56	90	
		V _{GS} = 1.8 V, I _D = 1.8 A		88	125	
		V _{GS} = 1.5 V, I _D = 1.5 A		133	250	
Forward Transconductance	g _{FS}	V _{DS} = 5.0 V, I _D = 2.0 A		4.5		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 15 V		427		pF
Output Capacitance	C _{OSS}			51		
Reverse Transfer Capacitance	C _{RSS}			32		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 2.0 A		5.4	6.5	nC
Threshold Gate Charge	Q _{G(TH)}			0.5		
Gate-to-Source Charge	Q _{GS}			0.8		
Gate-to-Drain Charge	Q _{GD}			1.24		
Gate Resistance	R _G			0.37		Ω

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DD} = 15 V, I _D = 2.0 A, R _G = 2.0 Ω		4.8		ns
Rise Time	t _r			11.8		
Turn-Off Delay Time	t _{d(OFF)}			14.2		
Fall Time	t _f			1.7		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.0 A	T _J = 25°C		0.78	1.2	V
			T _J = 125°C		0.62		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /dt _i = 100 A/μs, I _S = 2.0 A		10.5			ns
Charge Time	t _a			7.6			
Discharge Time	t _b			2.9			
Reverse Recovery Time	Q _{RR}			5.0			nC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

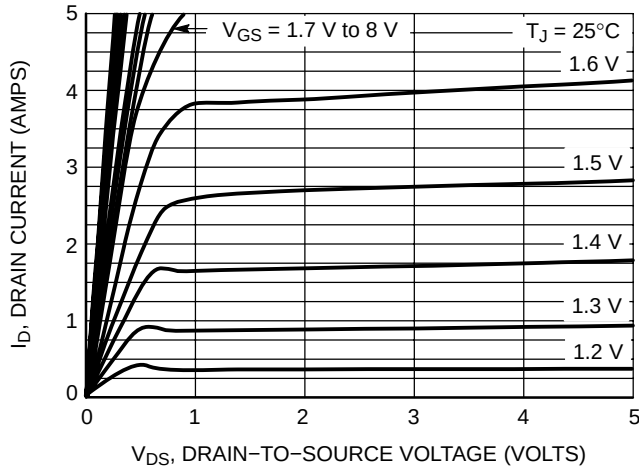


Figure 1. On-Region Characteristics

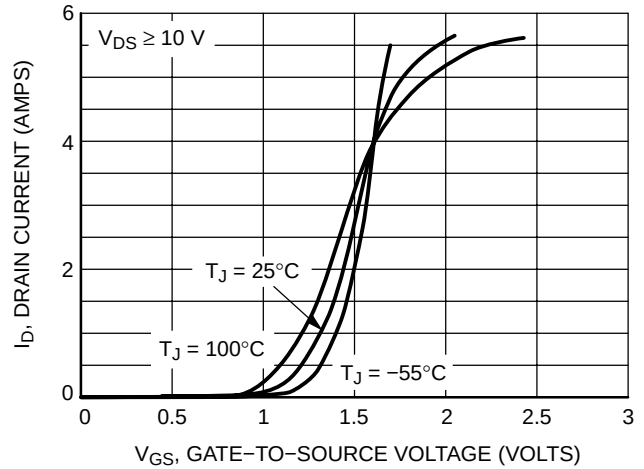


Figure 2. Transfer Characteristics

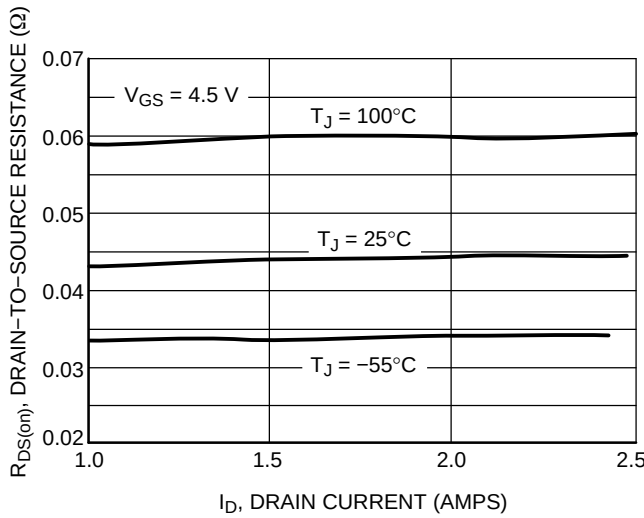


Figure 3. On-Resistance versus Drain Current

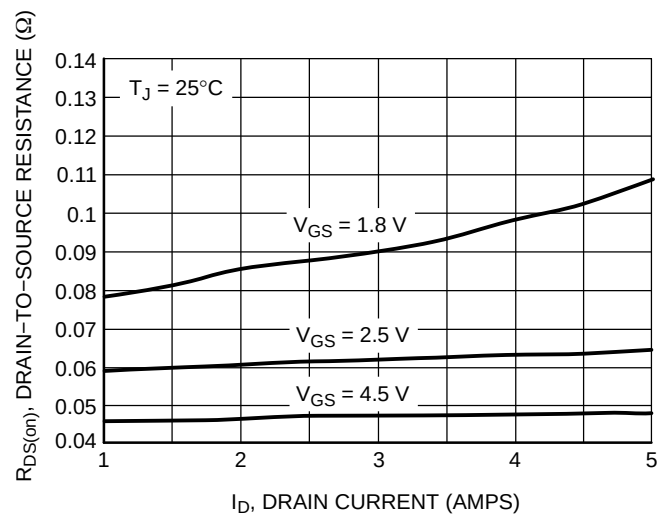


Figure 4. On-Resistance versus Drain Current and Gate Voltage

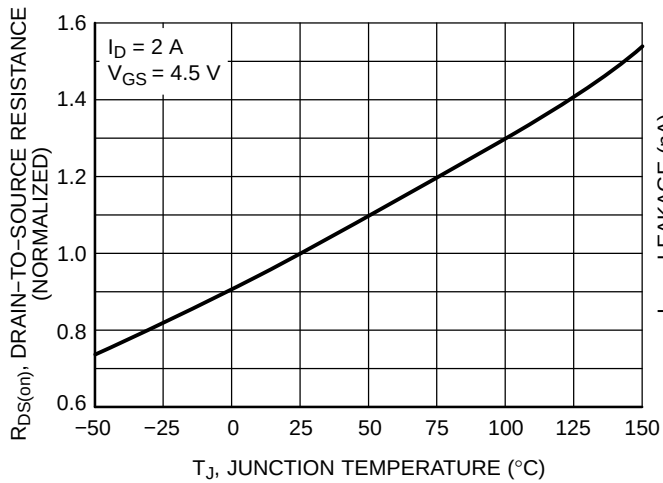


Figure 5. On-Resistance Variation with Temperature

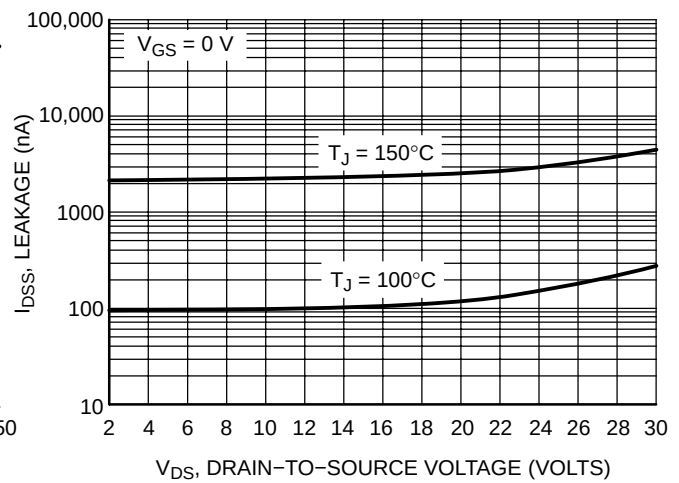


Figure 6. Drain-to-Source Leakage Current versus Voltage

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

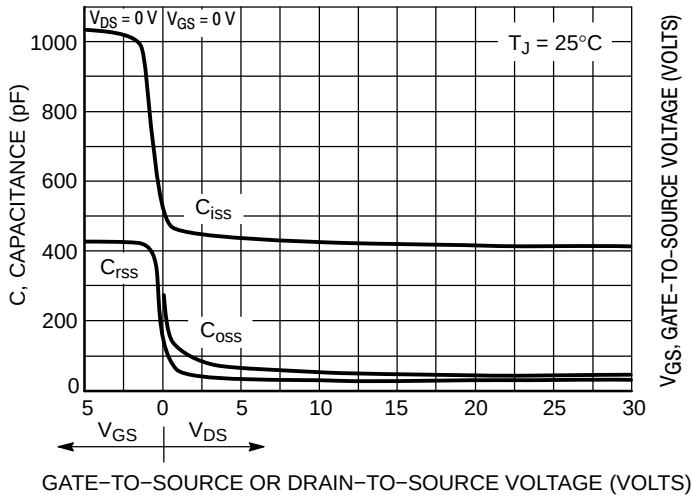


Figure 7. Capacitance Variation

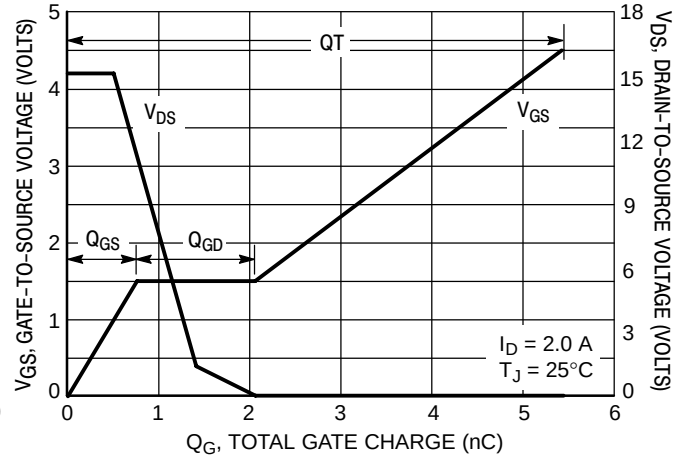


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

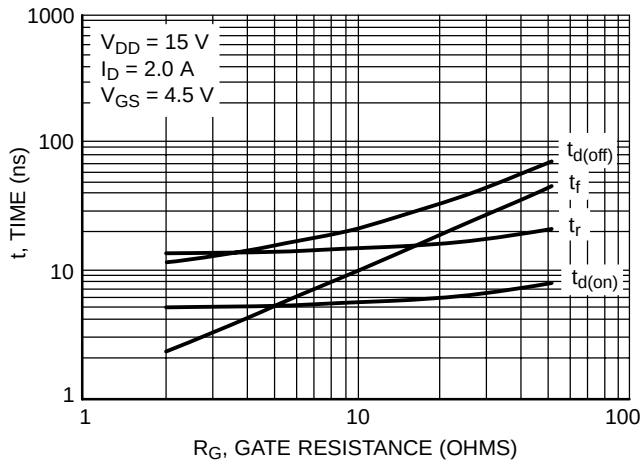


Figure 9. Resistive Switching Time Variation versus Gate Resistance

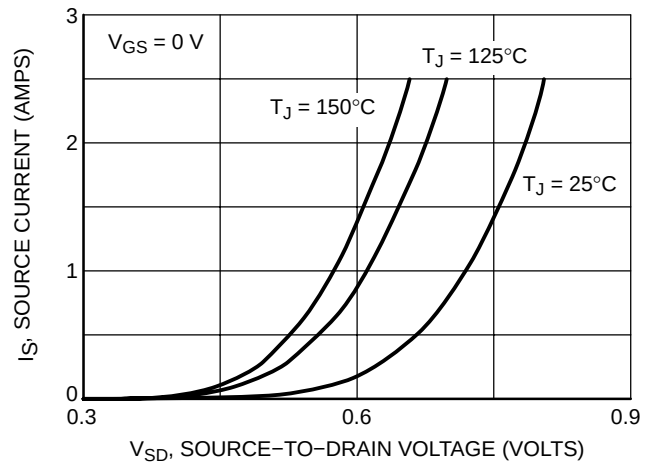


Figure 10. Diode Forward Voltage versus Current

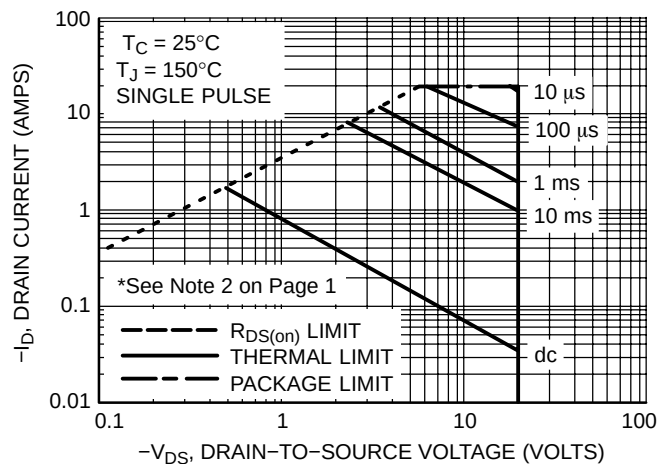


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

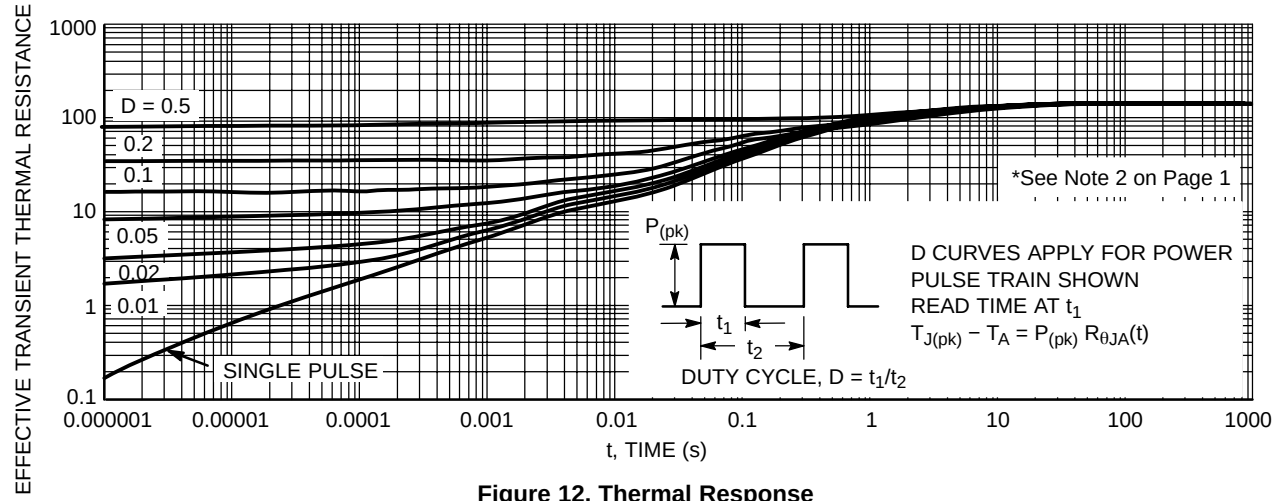


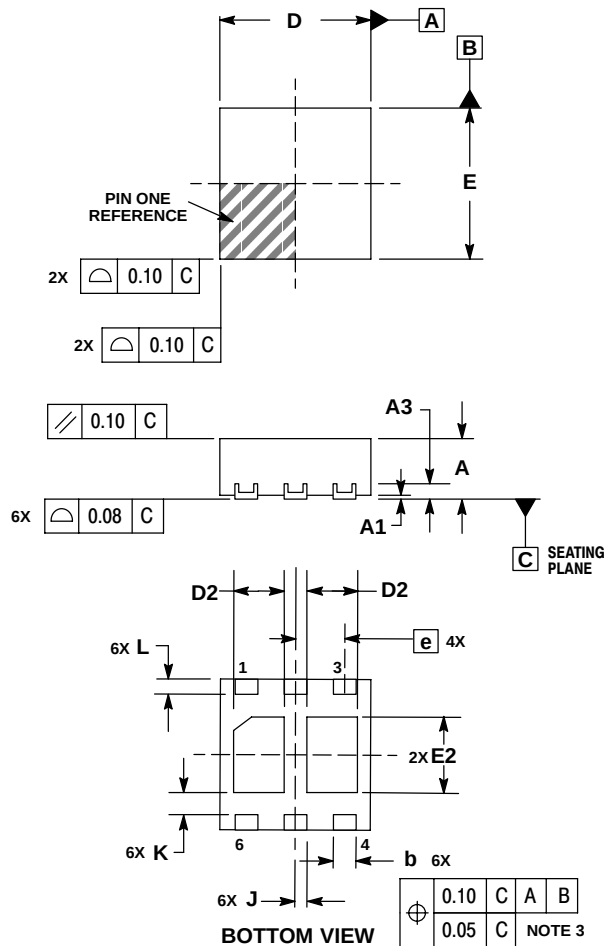
Figure 12. Thermal Response

NTLJD4116N

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PACKAGE DIMENSIONS

WDFN6, 2x2
CASE 506AN-01
ISSUE B

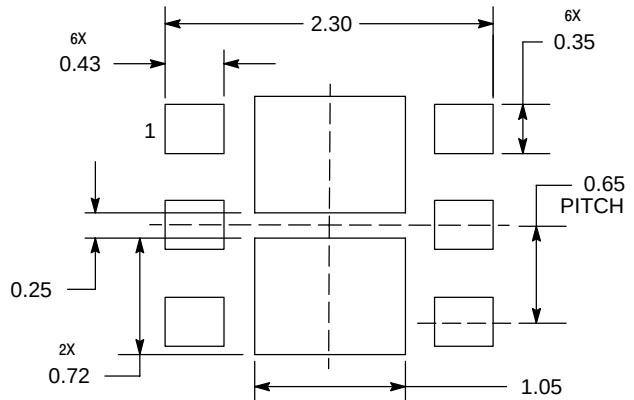


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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