

查询"74HC4316D.T"供应商
QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance:
160 Ω (typ.) at $V_{CC} - V_{EE} = 4.5\text{ V}$
120 Ω (typ.) at $V_{CC} - V_{EE} = 6.0\text{ V}$
80 Ω (typ.) at $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation:
to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I²C category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4316 are high-speed Si-gate CMOS devices. They are compliant with JEDEC standard no. 7A.

The 74HC/HCT4316 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (E) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range: $V_{CC} \geq (V_Y, V_Z) \geq V_{EE}$. Inputs nY and nZ are electrically equivalent terminals.

V_{CC} and GND are the supply voltage pins for the digital control inputs (E and nS). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V. See the "4016" for the version without logic level translation.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PZH}	turn "ON" time E to V _{OS} nS to V _{OS}	C _L = 15 pF R _L = 1 kΩ V _{CC} = 5 V	19	19	ns
			16	17	ns
t _{PZL}	turn "ON" time E to V _{OS} nS to V _{OS}		19	24	ns
			16	21	ns
t _{PHZ} / t _{PLZ}	turn "OFF" time E to V _{OS} nS to V _{OS}		20	21	ns
			16	19	ns
C _I	input capacitance	3.5	3.5	pF	
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	13	14	pF
C _S	max. switch capacitance		5	5	pF

$V_{EE} = \text{GND} = 0\text{ V}$; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

f_i = input frequency in MHz
f_o = output frequency in MHz
Σ{(C_L + C_S) × V_{CC}² × f_o} = sum of outputs
C_L = output load capacitance in pF
C_S = max. switch capacitance in pF
V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

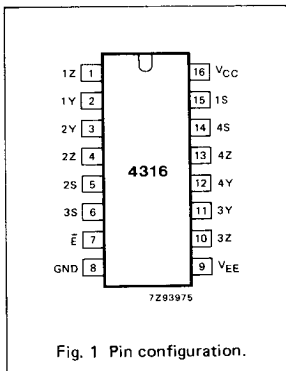


Fig. 1 Pin configuration.

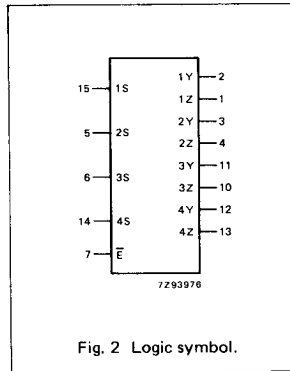


Fig. 2 Logic symbol.

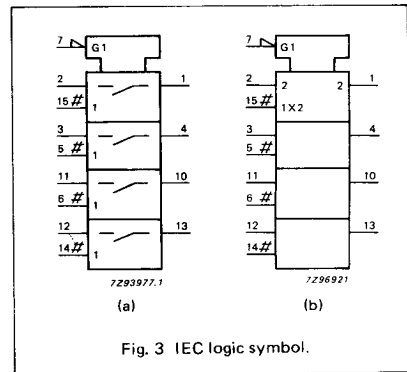


Fig. 3 IEC logic symbol.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Z to 4Z	independent inputs/outputs
2, 3, 11, 12	1Y to 4Y	independent inputs/outputs
7	\bar{E}	enable input (active LOW)
8	GND	ground (0 V)
9	V _{EE}	negative supply voltage
15, 5, 6, 14	1S to 4S	select inputs (active HIGH)
16	V _{CC}	positive supply voltage

FUNCTION TABLE

INPUTS		SWITCH
\bar{E}	nS	
L	L	off
L	H	on
H	X	off

H = HIGH voltage level
L = LOW voltage level
X = don't care

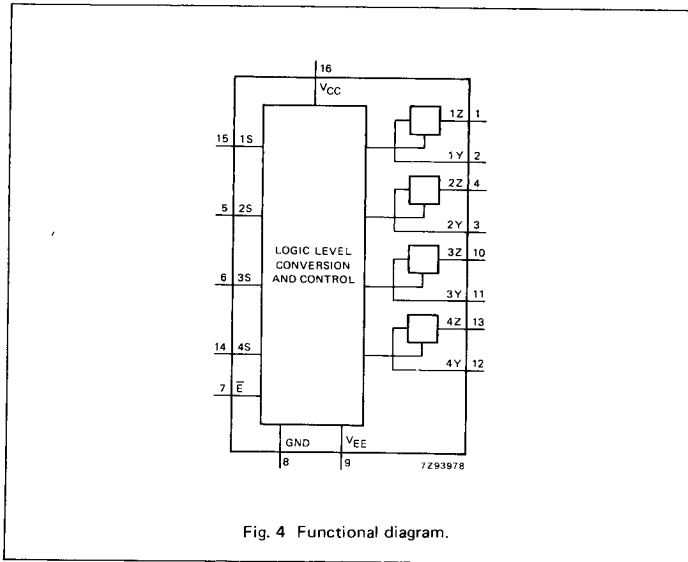


Fig. 4 Functional diagram.

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

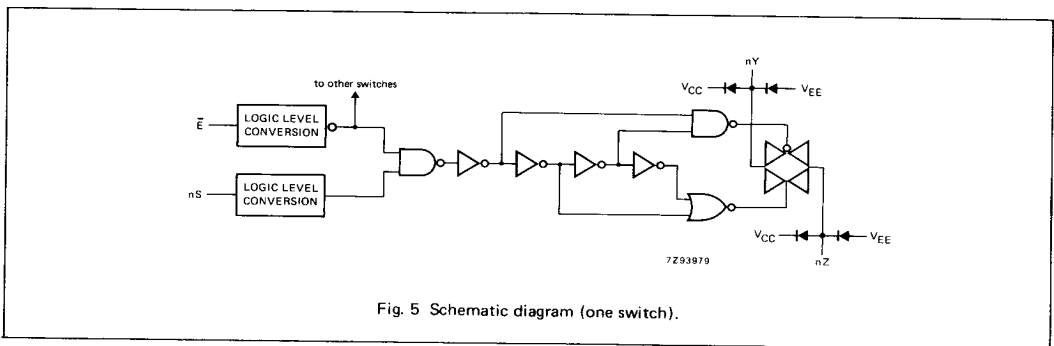


Fig. 5 Schematic diagram (one switch).

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Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to $V_{EE} = \text{GND}$ (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC};$ $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	-65	+150	$^{\circ}\text{C}$	
P_{tot}	power dissipation per package				for temperature range: -40 to $+125^{\circ}\text{C}$ 74HC/HCT
	plastic DIL		750	mW	above $+70^{\circ}\text{C}$: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above $+70^{\circ}\text{C}$: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminal Y_n . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	-40		+85	-40		+85	$^{\circ}\text{C}$	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	-40		+125	-40		+125	$^{\circ}\text{C}$	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

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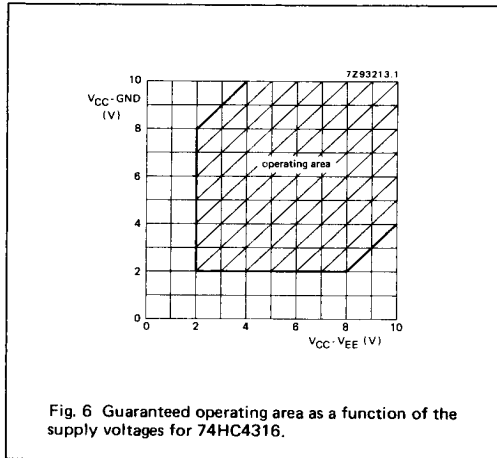


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4316.

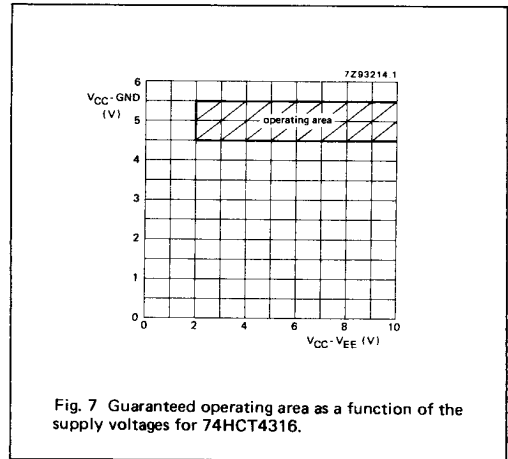


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4316.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

For 74HCT: $V_{CC} - GND = 4.5$ and 5.5 V; $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS					
		74HC/HCT							V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I	
		+25		-40 to +85		-40 to +125								
		min.	typ.	max.	min.	max.	min.		max.					
RON	ON resistance (peak)		160	320		400		480	Ω	2.0	0	100	V_{CC} to V_{EE}	V_{IH} or V_{IL}
			120	240		300		360	Ω	4.5	0	1000		
			85	170		215		255	Ω	6.0	0	1000		
RON	ON resistance (rail)		160	-		-		-	Ω	2.0	0	100	V_{EE}	V_{IH} or V_{IL}
			80	160		200		240	Ω	4.5	0	1000		
			70	140		175		210	Ω	6.0	0	1000		
RON	ON resistance (rail)		170	-		-		-	Ω	2.0	0	100	V_{CC}	V_{IH} or V_{IL}
			90	180		225		270	Ω	4.5	0	1000		
			80	160		200		240	Ω	6.0	0	1000		
ΔR_{ON}	maximum ΔR_{ON} resistance between any two channels		-						Ω	2.0	0		V_{CC} to V_{EE}	V_{IH} or V_{IL}
			16						Ω	4.5	0			
			9						Ω	6.0	0			
		6						Ω	4.5	-4.5				

Notes to DC characteristics

- At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig. 8.

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DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS				
		74HC							V _{CC} V	V _{EE} V	V _I	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	V	2.0 4.5 6.0 9.0				
V _{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
±I _I	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V _{CC} or GND	
±I _S	analog switch OFF-state current			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 10)
±I _S	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 11)
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V_{CC} V	V_{EE} V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ t_{PLH}	propagation delay V_{is} to V_{os}		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ t_{PZL}	turn "ON" time \bar{E} to V_{os}		61 22 18 19	205 41 35 37		255 51 43 47		310 62 53 56	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PZH}/$ t_{PZL}	turn "ON" time nS to V_{os}		52 19 15 17	175 35 30 34		220 44 37 43		265 53 45 51	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/$ t_{PLZ}	turn "OFF" time \bar{E} to V_{os}		63 23 18 21	220 44 37 39		275 55 47 49		330 66 56 59	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/$ t_{PLZ}	turn "OFF" time nS to V_{os}		55 20 16 18	175 35 30 36		220 44 37 45		265 53 45 54	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)

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DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

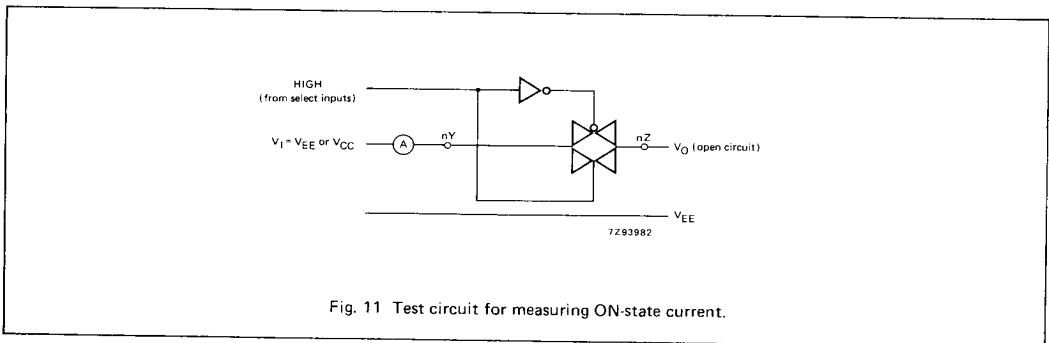
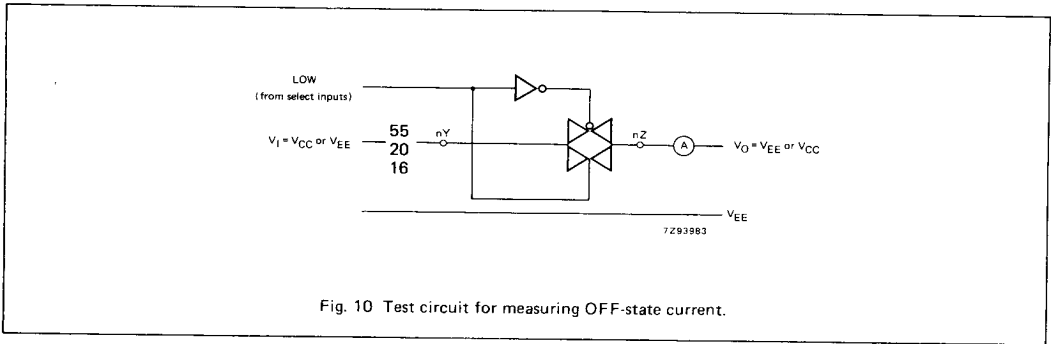
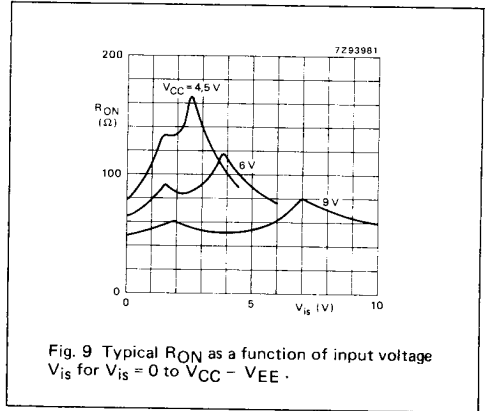
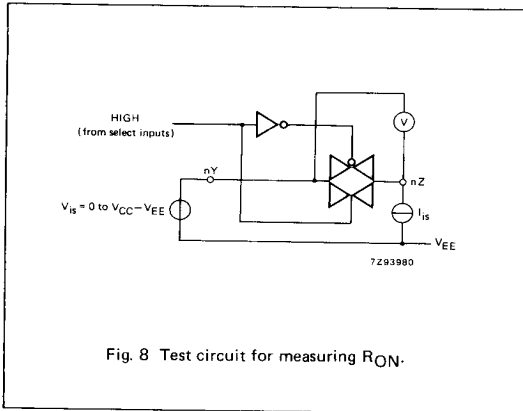
SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS				
		74HCT							V _{CC} V	V _{EE} V	V _I	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I _I	input leakage current			0.1		1.0		1.0	μA	5.5	0	V _{CC} or GND	
±I _S	analog switch OFF-state current			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 10)
±I _S	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 11)
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V _{CC} -2.1V	other inputs at V _{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nS	0.50
E	0.50

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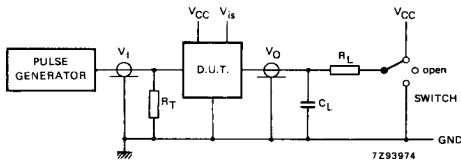
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V_{CC} V	V_{EE} V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ t_{PLH}	propagation delay V_{is} to V_{os}		6 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig. 18)
t_{PZH}	turn "ON" time \bar{E} to V_{os}		22 21	44 42		55 53		66 63	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
t_{PZL}	turn "ON" time \bar{E} to V_{os}		28 21	56 42		70 53		84 63	ns	4.5 4.5	0 -4.5	
t_{PZH}	turn "ON" time nS to V_{os}		20 17	40 34		53 43		60 51	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
t_{PZL}	turn "ON" time nS to V_{os}		25 17	50 34		63 43		75 51	ns	4.5 4.5	0 -4.5	
$t_{PHZ}/$ t_{PLZ}	turn "OFF" time \bar{E} to V_{os}		25 23	50 46		63 58		75 69	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/$ t_{PLZ}	turn "OFF" time nS to V_{os}		22 20	44 40		55 50		66 60	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)

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TEST CIRCUIT AND WAVEFORMS



Conditions

TEST	SWITCH	V _{is}
t _{PZH}	GND	V _{CC}
t _{PZL}	V _{CC}	GND
t _{PHZ}	GND	V _{CC}
t _{PLZ}	V _{CC}	GND
others	open	pulse

Fig. 18 Test circuit for measuring AC performance.

Definitions for Figs 18 and 19:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

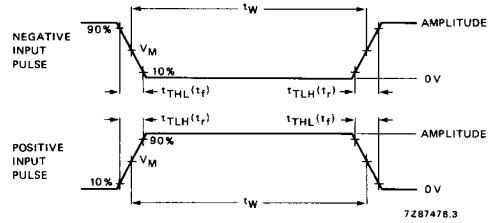
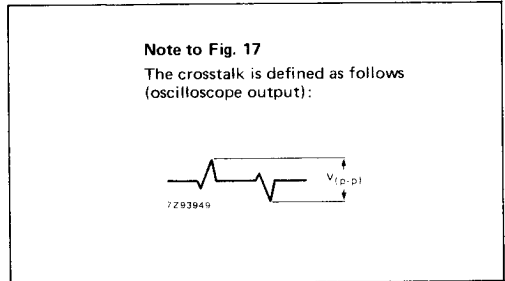
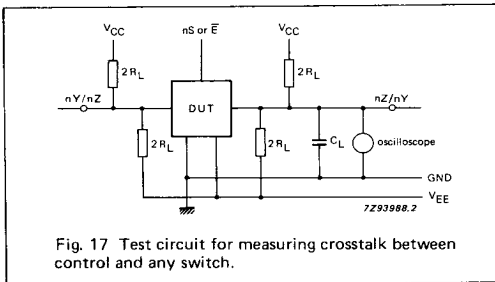
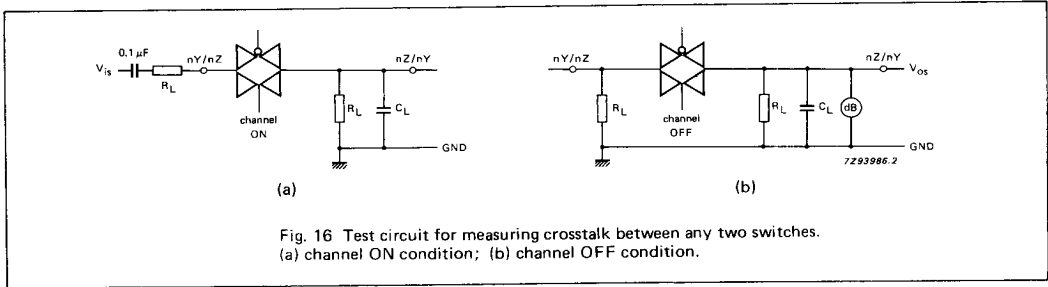
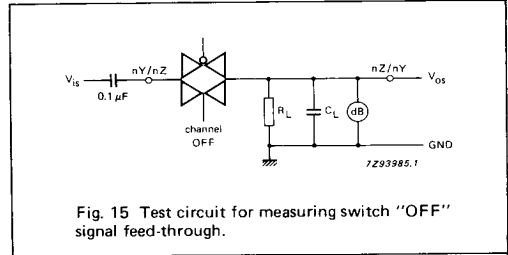
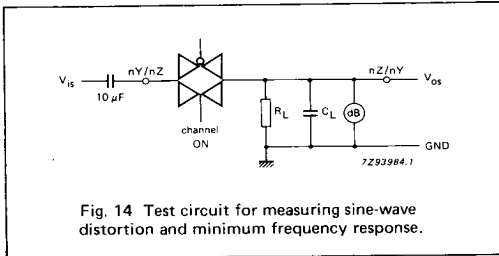
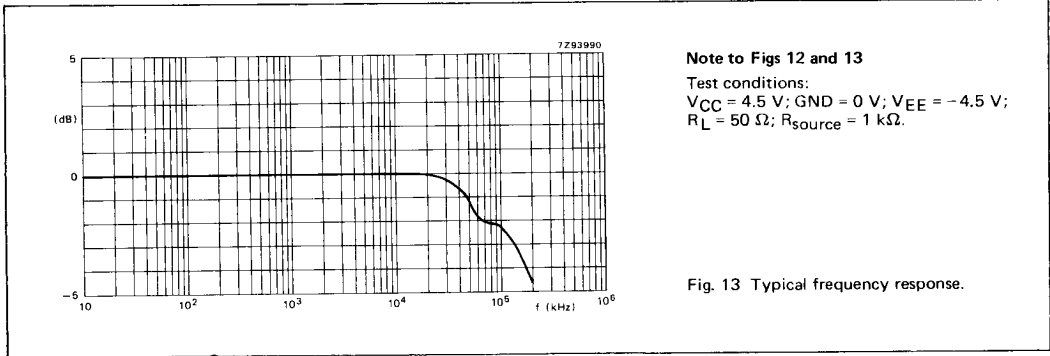


Fig. 19 Input pulse definitions.

FAMILY	AMPLITUDE	V _M	t _r ; t _f	
			f _{max} ; PULSE WIDTH	OTHER
74HC	V _{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

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AC WAVEFORMS

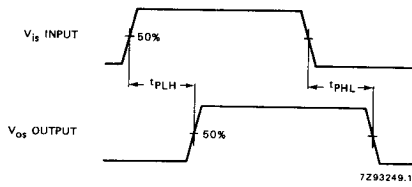


Fig. 18 Waveforms showing the input (V_{1S}) to output (V_{Os}) propagation delays.

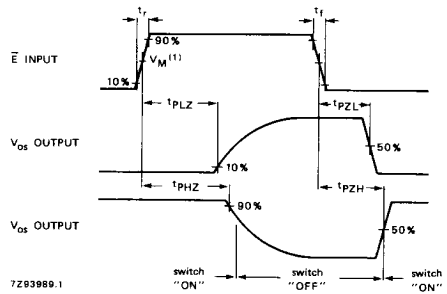
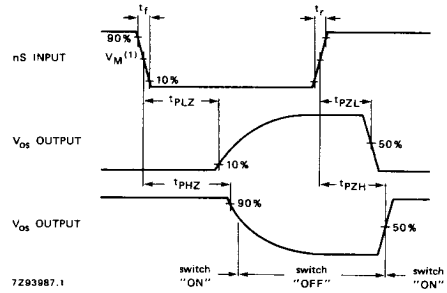


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Notes to Fig. 19

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

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TEST CIRCUIT AND WAVEFORMS

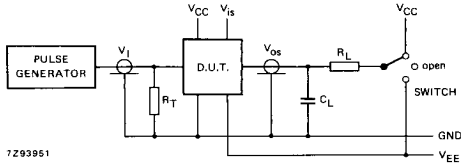


Fig. 20 Test circuit for measuring AC performance.

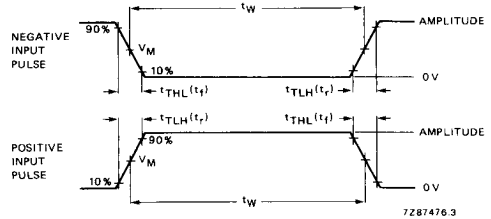


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V _{is}
t _{PZH}	VEE	V _{CC}
t _{PZL}	V _{CC}	VEE
t _{PHZ}	VEE	V _{CC}
t _{PLZ}	V _{CC}	VEE
others	open	pulse

FAMILY	AMPLITUDE	V _M	t _r ; t _f	
			f _{max} ; PULSE WIDTH	OTHER
74HC	V _{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.