查询"2SK2544<u>10S</u>曲应商eld Effect Transistor Silicon N Channel MOS Type (π-MOSV)

2SK2544

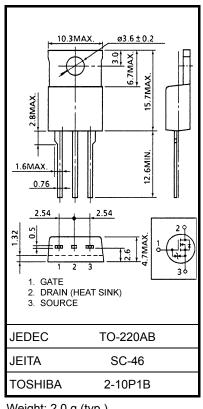
Switching Regulator Applications

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- Low drain-source ON resistance $: RDS (ON) = 0.9 \Omega(typ.)$
- High forward transfer admittance $|Y_{fs}| = 5.5 \text{ S (typ.)}$
- Low leakage current : $I_{DSS} = 100 \ \mu A \ (max) \ (V_{DS} = 600 \ V)$
- Enhancement mode $: V_{th} = 2.0 \sim 4.0 V (V_{DS} = 10 V, I_{D} = 1 mA)$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V _{DSS}	600	V
Drain-gate voltage (R _{GS} = 20 kΩ)		V _{DGR}	600	V
Gate-source voltage	_	V _{GSS}	±30	V
Drain current	DC (Note 1)	۱ _D	6	А
	Pulse (Note 1)	I _{DP}	24	А
Drain power dissipation	n (Tc = 25°C)	PD	80	W
Single pulse avalanche energy (Note 2)		E _{AS}	345	mJ
Avalanche current		I _{AR}	6	А
Repetitive avalanche e	nergy (Note 3)	E _{AR}	8	mJ
Channel temperature		T _{ch}	150	°C
Storage temperature ra	ange	T _{stg}	-55~150	°C



Weight: 2.0 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch−c)}	1.56	°C / W
Thermal resistance, channel to ambient	R _{th (ch−a)}	83.3	°C / W

Note 1: Ensure that the channel temperature does not exceed 150°C..

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 16.8 mH, R_G = 25 Ω , I_{AR} = 6 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Please handle with caution.

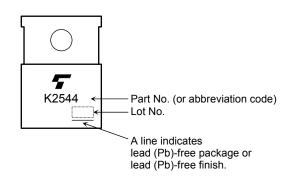
Eterrica for analdter stics (Ta = 25°C)

Charao	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cu	urrent	I _{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	_		±10	μA
Gate-source br	eakdown voltage	V _(BR) GSS	I _G = ±10 μA, V _{GS} = 0 V	±30	_	_	V
Drain cut-off cu	rrent	I _{DSS}	V _{DS} = 600 V, V _{DS} = 0 V	_	_	100	μA
Drain-source br	reakdown voltage	V (BR) DSS	I _D = 10 mA, V _{GS} = 0 V	600	_	_	V
Gate threshold	voltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.0	_	4.0	V
Drain-source O	N resistance	R _{DS (ON)}	V _{GS} = 10 V, I _D = 3 A		0.9	1.25	Ω
Forward transfe	r admittance	Y _{fs}	V _{DS} = 10 V, I _D = 3 A	2.0	5.5	_	S
Input capacitance	ce C _{iss}				1300		pF
Reverse transfer capacitance		C _{rss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		130		
Output capacitance		C _{oss}			400		
Switching time	Rise time	tr	$V_{GS} \stackrel{10V}{}_{0V} \stackrel{I_{D}=3A}{}_{R_{L}} \stackrel{V_{out}}{=} 100\Omega$ $V_{DD} \stackrel{=}{=} 300V$	_	25	_	- ns
	Turn-on time	t _{on}		_	45	_	
	Fall time	t _f		_	40	_	
	Turn-off time	t _{off}	Duty $\leq 1\%$, t _w =10µs		150		
Total gate charge (Gate-source plus gate-drain)		Qg		_	30	_	
Gate-source charge		Q _{gs}	V _{DD} ≈ 400 V, V _{GS} = 10 V, I _D = 6 A		18	_	nC
Gate-drain ("miller") charge		Q _{gd}			12	_	

Source–Drain Ratings and Characteristics (Ta = 25°C)

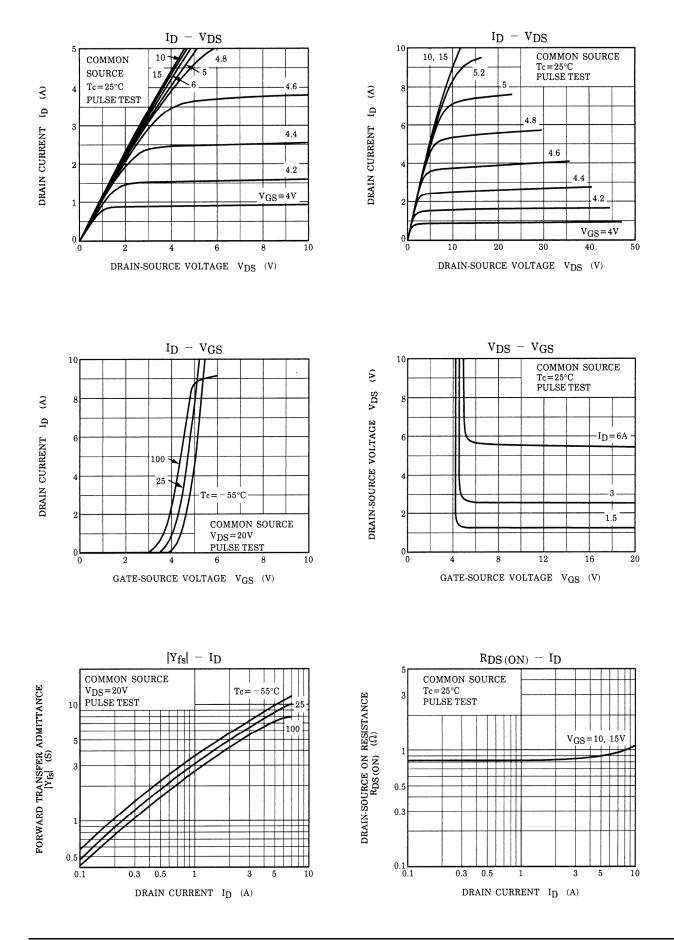
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	—		_	6	А
Pulse drain reverse current (Note 1)	I _{DRP}	_	Ι		24	А
Forward voltage (diode)	V _{DSF}	I _{DR} = 6 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 6 A, V _{GS} = 0 V	_	1000		ns
Reverse recovery charge	Qrr	dI _{DR} / dt = 100 A / μs	_	7		μC

Marking



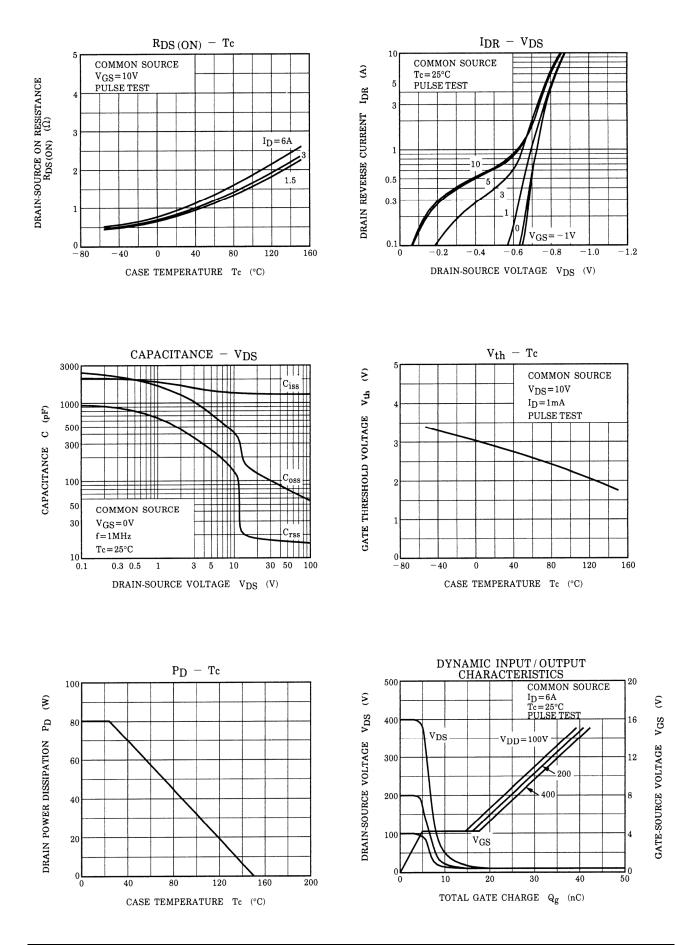
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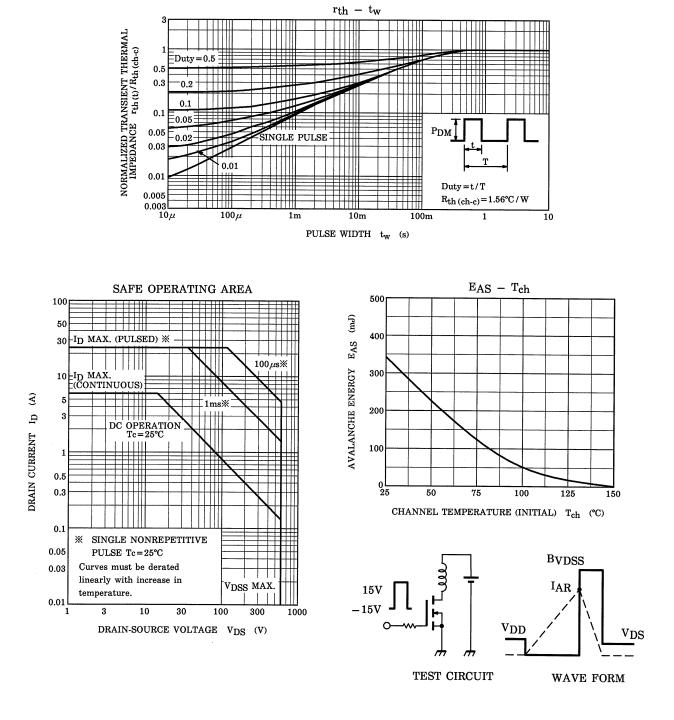
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$$\begin{array}{l} \text{R}_{\text{G}} = 25 \ \Omega \\ \text{V}_{\text{DD}} = 90 \ \text{V}, \ \text{L} = 16.8 \ \text{mH} \end{array} \qquad \qquad \text{EAS} = \frac{1}{2} \cdot \text{L} \cdot \text{I}^2 \cdot \left(\frac{\text{BVDSS}}{\text{BVDSS} - \text{VDD}} \right)$$

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