Dual 12 V Protection / Blocking Controller

Check for Samples: TPS2456

FEATURES

- **Dual 12 V Protection and Blocking Control**
- **Independent Current Limit and Fast Trip**
- **Blocking Permits ORing of Multiple Inputs**
- **Power Good and Fault Outputs**
- **Analog Current Monitor Outputs**
- **-40°C to 125°C Operating Junction Temperature**
- **QFN36 Package**

APPLICATIONS

- **ATCA Carrier Boards**
- **AdvancedMC™ Slots**
- **Blade Servers**
- **Base Stations**
- **Configurable for**
  - **1 Source, 2 Loads**
  - **2 Sources, 1 Load**
  - **2 Sources, 2 Loads**

DESCRIPTION

The TPS2456 is a dual, 12 V, channel protection (hotswap) and blocking (ORing) controller that provides inrush control, current limiting, overload protection, and reverse current blocking. The current sense topology provides both accurate current limits and independent setting of current limit and fast trip thresholds.

The ORing control uses an external MOSFET to block reverse current when an input is shorted. Systems with closely matched supply voltages and feed networks can supply current from both supplies simultaneously.

The MONx output provides an accurate analog indication of load current.

The protection circuits may be used without blocking, and the blocking may be used without protection. Internal connections prevent implementation of these as four fully-independent functions.

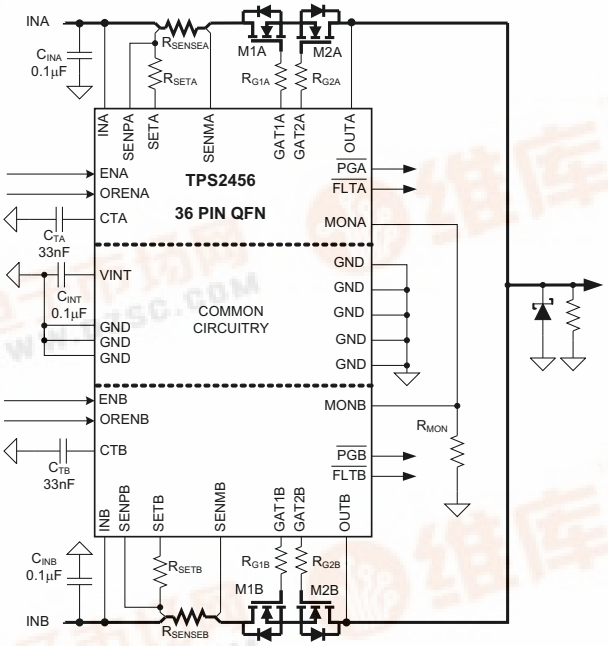


Figure 1. Two Sources, One Load Application Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PRODUCT INFORMATION(1)

DEVICE	TEMPERATURE	PACKAGE	MARKING
TPS2456RHH	–40°C to 85°C	QFN36 (6mm × 6mm)	TPS2456

(1) For package and ordering information see the Package Option Addendum at the end of this document or see the TI Web site at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2456 RHH 36 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	32	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	23	
θ_{JB}	Junction-to-board thermal resistance (4)	11	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter (6)	10	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	2.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ABSOLUTE MAXIMUM RATINGS(1)

Over recommended junction temperature range and all voltages referenced to GND, unless otherwise noted.

PINS OR PIN GROUPS		VALUE	UNITS
GAT1x, GAT2x		–0.3 to 30	V
INx, OUTx, SENPx, SENMx, SETx, ENx, $\overline{FLTx}$, $\overline{PGx}$, ORENx		–0.3 to 17	V
CTx, MONx		–0.3 to 5	V
$\overline{FLTx}$, $\overline{PGx}$ current sinking		5	mA
MONx current sourcing		5	mA
VINT current		–1 to 1	mA
ESD	Human Body Model	2	kV
	Charged Device Model	0.5	kV
Junction Temperature		Internally Limited	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over recommended junction temperature range and all voltages referenced to GND, unless otherwise noted.

	MIN	TYP	MAX	UNIT
V_{INx}	8.5	12	15	V
I_{MONx}		100	1000	µA
GAT1x, GAT2x board leakage current(1)	–1		1	µA
VINT bypass capacitance	1	100	250	nF
Operating junction temperature range, T_J	–40		125	°C

(1) This condition applies to the PCB and is not a limit on the TPS2456.

ELECTRICAL CHARACTERISTICS

Common conditions (unless otherwise noted) are: INA = INB = SENPA = SENPB = SENMA = SENMB = SETPA = SETPB = 12 V, ENA = ENB = ORENA = ORENB = 3 V, CTA = CTB = GND, $R_{MONA} = R_{MONB} = 6.81k\Omega$, all other pins open, $–40°C \le T_J \le 125°C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Enable Input – ENx, ORENx					
Threshold voltage	V_{INx} ↑	1.25	1.35	1.45	V
Hysteresis		20	50	80	mV
Pullup current	ENx = ORENx = 0 V, current sourcing	5	8	15	µA
Input bias current	ENx = ORENx = 17 V, current sinking		6	15	µA
Turn off time(1) (2)	ENx deasserts to V_{OUTx} < 1 V, C_{OUT} = 0 µF, Q_{GAT1x} = 33 nF			20	µs
Power Good Output – $\overline{PGx}$					
Output low voltage	$I_{\overline{PGx}}$ = 2 mA sinking		0.14	0.25	V
Leakage current	$\overline{PGx}$ = 17 V (sinking)			1	µA
Threshold voltage	$\overline{PGx}$, V_{OUTx} ↓	10.2	10.5	10.8	V
Hysteresis	$\overline{PGx}$, V_{OUTx} ↑		130(2)		mV
Deglitch time	$\overline{PGx}$ falling	50	100	150	µs
Fault Output – $\overline{FLTx}$					
Output low voltage	$I_{\overline{FLTx}}$ = 2 mA sinking		0.14	0.25	V
Leakage current	$V_{\overline{FLTx}}$ = 17 V (sinking)			1	µA
Bias Supply – VINT					
Output voltage	$0 < I_{VINT} < 50$ µA	2	2.3	2.8	V
Fault Timer – CTx					
Sourcing current	V_{CTx} = 0 V, during fault	7	10	13	µA
Upper threshold voltage		1.30	1.35	1.40	V
Discharge pulldown(2)			200		Ω
Timer start threshold	($V_{GAT1x} – V_{INx}$) when timer starts, with V_{GAT1x} falling due to over current	5	6	7	V
Channel Current Monitor – MONx					
Input referred offset	10.8 V ≤ V_{SENMx} ≤ 13.2 V, $V_{SENPx} = V_{SENMx}$ + 50 mV, measure $V_{SETx} – V_{SENMx}$	–1.5		1.5	mV
MONx threshold	V_{GAT1x} = 15 V	0.66	0.675	0.69	V
Leakage current	$V_{SETx} = (V_{SENMx} – 10$ mV)			1	µA

(1) Tested with HAT2156 MOSFET.
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS (continued)

Common conditions (unless otherwise noted) are: INA = INB = SENPA = SENPB = SENMA = SENMB = SETPA = SETPB = 12 V, ENA = ENB = ORENA = ORENB = 3 V, CTA = CTB = GND, R_{MONA} = R_{MONB} = 6.81kΩ, all other pins open, –40°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current limit					
Current limit threshold	R_{SETx} = 500 Ω, R_{MONx} = 6800 Ω, measure V_{SENPx} – V_{SENMx} when V_{GAT1x} = 15 V	47.5	50	52.5	mV
Sink current in current limit	V_{MONx} = 1 V, V_{GAT1x} = 12 V, measure I_{GAT1x}	20		40	µA
Fast trip threshold	Measure V_{SENPx} – V_{SENMx}	80	100	120	mV
Fast turn-off delay	(V_{SENP} – V_{SENM}): 0 V → 120 mV, t_{P50-50} (3)		200	300	ns
Channel UVLO					
UVLO	V_{INx} ↑	8.1	8.5	8.9	V
UVLO hysteresis	V_{INx} ↓	0.44	0.5	0.59	V
Blocking Comparator					
Turn-on threshold	Measure (V_{SENPx} – V_{OUTx})	5	10	20	mV
Turn-off threshold	Measure (V_{SENPx} – V_{OUTx})	–6	–3	0	mV
Turn-off delay	20 mV overdrive, t_{p50-50}		200	300	ns
Gate Drivers – GAT1x, GAT2x					
Output voltage	V_{INx} = V_{OUTx} = 10 V	21.5	23	24.5	V
Sourcing current	V_{INx} = V_{OUTx} = 10 V, V_{GAT1x} = V_{GAT2x} = 17 V	20	30	40	µA
Sinking current	Fast turnoff, V_{GAT1x} = V_{GAT2x} = 14 V, pulsed measurement	0.5	1		A
	Sustained, 4 V ≤ (V_{GAT1x} = V_{GAT2x}) ≤ 25 V	10	14	20	mA
Pulldown resistance	In thermal shutdown	14	20	26	kΩ
Fast turn-off duration		5	10	15	µs
Disable delay	ENx pin to V_{GATx1} and V_{GAT2x}, t_{P50-90} (4)			1	µs
Startup Time	INx rising to GAT1x or GAT2x sourcing current (ENx and ORENx high)			0.25	ms
Supply Current (I_{INx}+ I_{SENPx}+ I_{SENMx}+ I_{SETx}+ I_{OUTx})					
Both channels enabled			3.1	4	mA
Both channels disabled			2	2.8	mA
Thermal Shutdown					
Shutdown temperature	T_J rising	140	150		°C
Hysteresis			10 (5)		°C

(3) See Figure 3 for timing definition.
(4) See Figure 2 for timing definition.
(5) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

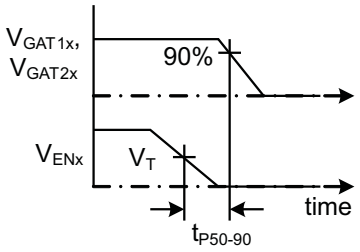


Figure 2. t_{P50-90}Definition

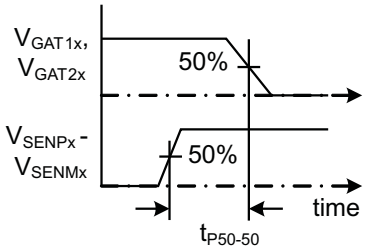


Figure 3. t_{P50-50} Definition

FUNCTIONAL BLOCK DIAGRAM

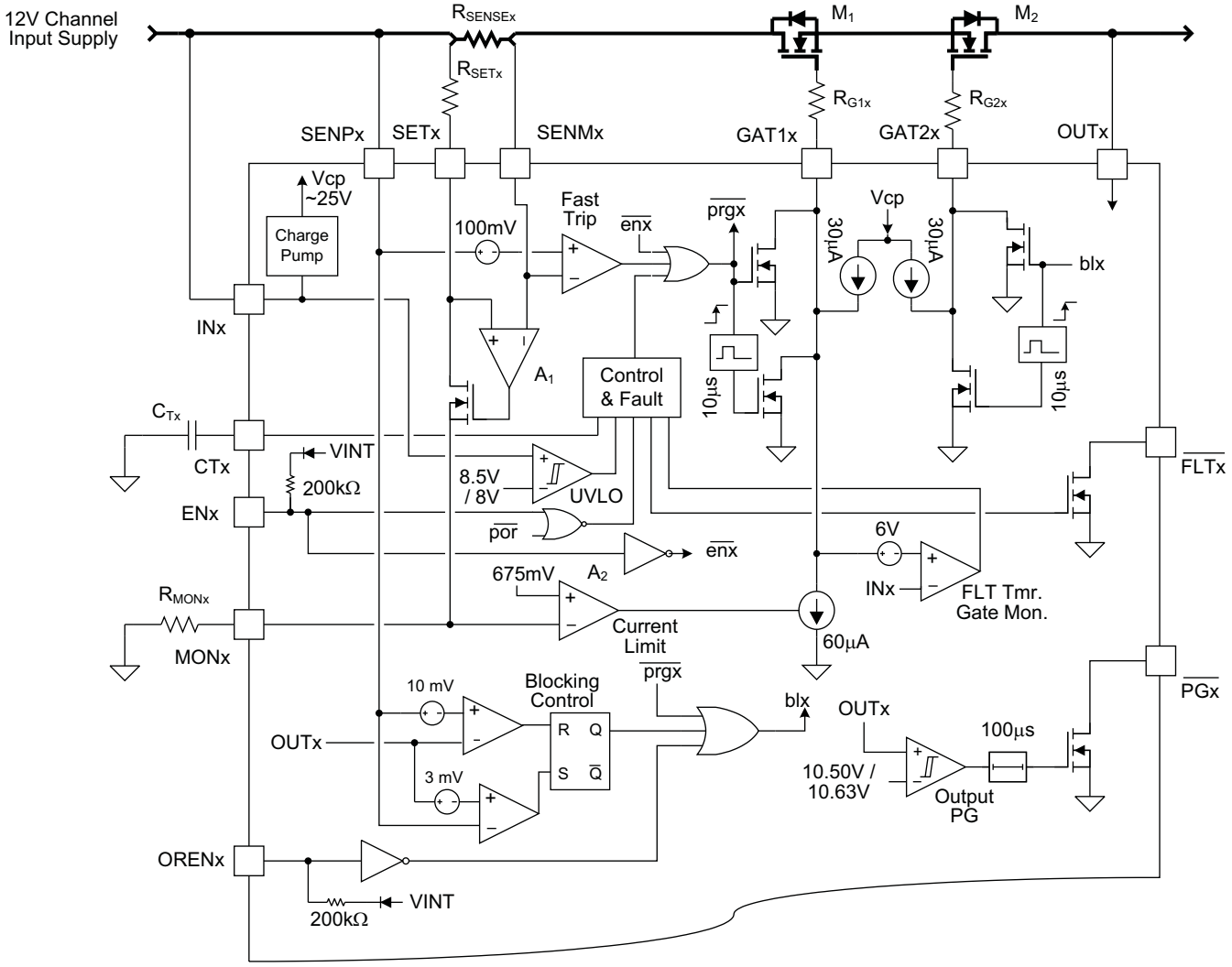


Figure 4. TPS2456 Channel (2 channels per device)

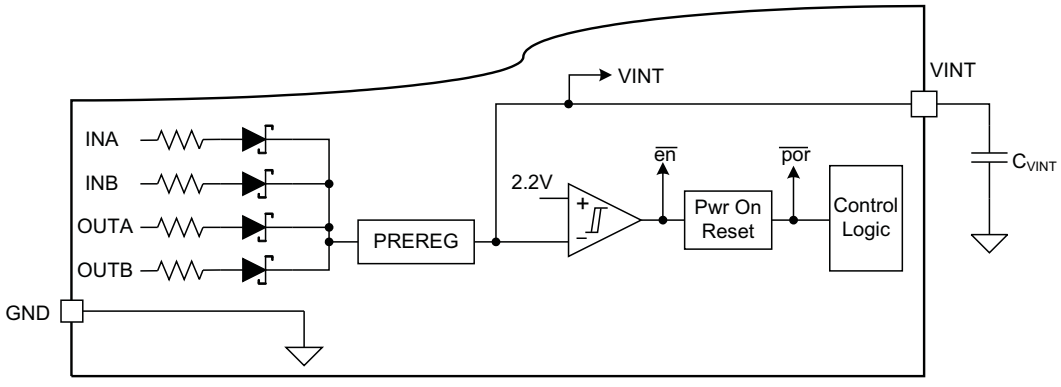


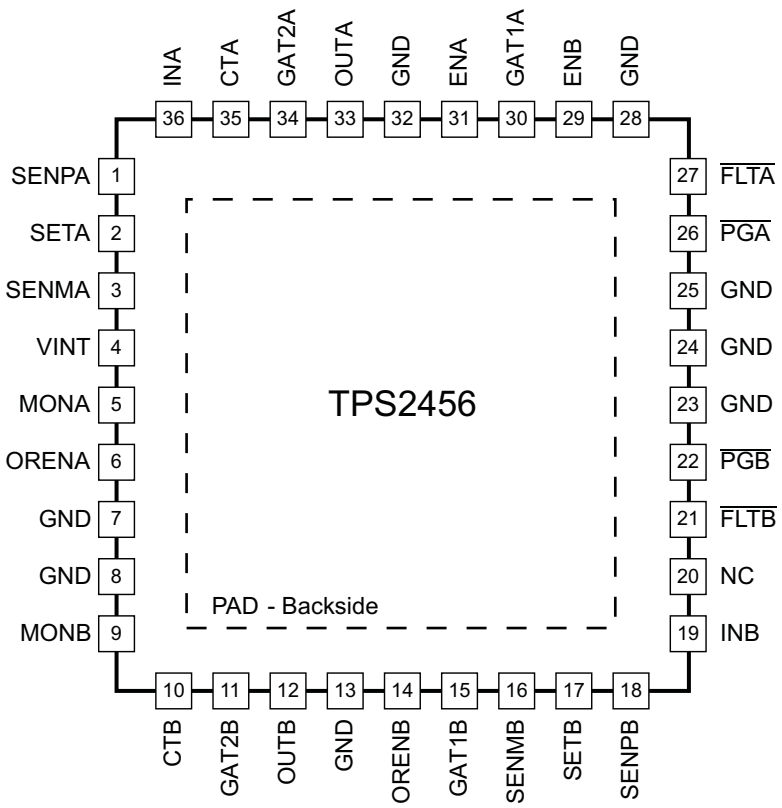
Figure 5. Common Control Circuits

PIN FUNCTIONS

PIN		TYPE	A/B[1]	DESCRIPTION
NAME	NO.			
SENPA	1	I	A	Input voltage sense – connect to input supply. Connect to the source side of R_{SENSEA}.
SETA	2	I	A	Connect R_{SETA} from the input supply to SETA to program the current limit in conjunction with R_{SENSEA} and R_{MONA} (see text).
SENMA	3	I	A	Connect this pin to the load side of the R_{SENSEA}. The fast-trip threshold equals 100 mV / R_{SENSEA}.
VINT	4	I/O	–	Connect a bypass capacitor (e.g., 0.01µF) to GND for this internal supply.
MONA	5	I/O	A	Connect R_{MONA} from MONA to GND to set the current limit in conjunction with R_{SENSEA} and R_{SETA} (see text).
ORENA	6	I	A	Blocking transistor enable, active high.
GND	7	GND	–	Connect pin to ground.
GND	8	GND	–	Connect pin to ground
MONB	9	I/O	B	Connect R_{MONB} from MONB to GND to set the current limit in conjunction with R_{SENSEB} and R_{SETB} (see text).
CTB	10	I/O	B	Connect C_{TB} from CTB to GND to set the fault timer period (see text).
GAT2B	11	O	B	Blocking transistor gate drive.
OUTB	12	I/O	B	Output voltage monitor and bias input.
GND	13	GND	B	Connect pin to ground.
ORENB	14	I	B	Blocking transistor enable, active high.
GAT1B	15	O	B	Protection transistor gate drive.
SENMB	16	I	B	Connect this pin to the load side of the R_{SENSEB}. The fast-trip threshold equals 100 mV / R_{SENSEB}.
SETB	17	I	B	Connect R_{SETB} from input supply to SETB to program the current limit program the current limit in conjunction with R_{SENSEB} and R_{MONB} (see text).
SENPB	18	I	B	Input voltage sense – connect to input supply. Connect to the source side of R_{SENSEB}.
INB	19	PWR	B	Control power input – connect to input supply.
–	20	–	–	No connection.
$\overline{FLTB}$	21	O	B	Fault output, active low, asserted when B fault timer runs out.
$\overline{PGB}$	22	O	B	Power good output, active low, asserts when V_{OUTB} > 10.63 V.
GND	23	GND	–	Connect pin to ground.
GND	24	GND	–	Connect pin to ground.
GND	25	GND	–	Connect pin to ground.
$\overline{PGA}$	26	O	A	Power good output, active low, asserts when V_{OUTA} > 10.63 V.
$\overline{FLTA}$	27	O	A	Fault output, active low, asserted when A fault timer runs out.
GND	28	GND	–	Connect pin to ground.
ENB	29	I	B	Enable, (active high).
GAT1A	30	O	A	Protection transistor gate drive.
ENA	31	I	A	Enable, (active high).
GND	32	GND	A	Connect pin to ground.
OUTA	33	I/O	A	Output voltage monitor and bias input.
GAT2A	34	O	A	Blocking transistor gate drive.
CTA	35	I/O	A	Connect C_{TA} from CTA to GND to set the fault timer period (see text).
INA	36	PWR	A	Control power input – connect to input supply.
PAD	–	–	–	Solder pad to GND.

(1) Specifies whether this pin is part of A channel, B channel, or is common to both (-).

DEVICE PINOUT
(TOP VIEW)



DETAILED PIN DESCRIPTIONS

The TPS2456 supports two 12-V protection (hotswap) and blocking (ORing) channels designated A and B. Where there are separate pins for both A and B channels, the pin name is shown with an x in place of A or B to describe the function. For example, references to CTx would be the same as CTA or CTB. Programming components are referred to in the text by reference designators used in Figure 1.

CTx – A capacitor from CTx to GND sets the period V_{GAT1x} can be low ($V_{GAT1x} < V_{INx} + 6$ V) before it shuts the channel down and declares a fault. V_{GAT1x} will be low during startup and current limit. Low V_{GAT1x} causes this pin to source 10 µA into the external capacitor (C_{Tx}). When V_{CTx} reaches 1.35 V, the TPS2456 shuts the channel off by pulling the GAT1x and GAT2x pins low, declares a fault by pulling the $\overline{\text{FLT}}$x pin low, and latching off. A 200 Ω internal pull down keeps this pin low during normal operation when not in current limit. It is normal to see a sawtooth on this pin when the channel is latched off by a fault.

ENx – Active high enable input. A low on ENx turns off the channel by pulling GAT1x and GAT2x low. An internal 200 kΩ resistor pulls this pin up to VINT. ENx may be left floating when the channel is to be permanently enabled.

$\overline{\text{FLT}}$x – Active low open-drain output indicating that V_{GAT1x} has been low ($V_{GAT1x} < V_{INx} + 6$ V) long enough trip the fault timer and shut the channel down. FLTx may be left open if not used.

GAT1x – Gate drive output for the protection MOSFET. This pin sources 30 µA to turn the MOSFET on. An internal clamp prevents this pin from rising more than 14.5 V above INx.

Up to 30µA may be sunk while current limit is active. A fast trip (overcurrent), disable (from ENx), or fault timeout enables a 10 µs, 1 A, discharge current and 14 mA pulldown. The pulldown will be released after 10 µs if only a fast trip had occurred.

Setting ENx low holds GAT1x low. GAT1x may be left open if not used.

GAT2x – Gate drive output for the blocking MOSFET. The blocking MOSFET prevents reverse channel current when OUTx is higher than INx. This is often used when two input sources are ORed together. GAT2x sources 30 µA to turn the MOSFET on. GAT2x is low when ENx is low, ORENx is low, $\overline{FLT}$x is low, a fast trip is active, or a voltage reversal has occurred. A 10 µs, 1 A, discharge and 14 mA pulldown are applied when this occurs.

An internal clamp prevents this pin from rising more than 14.5 V above OUTx. Setting the ORENx or ENx pins low holds the GAT2x pin low.

GAT2x may be left open if not used.

INx - Supply pin for the internal circuitry. A small bypass capacitor (e.g. 0.1 µF) is recommended for this pin.

MONx – A resistor connected from this pin to ground forms part of the current limit programming. As the current delivered to the load increases, so does the voltage on this pin. The current-limit circuit controls GAT1x to limit channel current at a V_{MONx} of 675 mV. The current limit circuit is inactive for lower values of V_{MONx}.

Equation 1 through Equation 4 define current limit and fast trip values using R_{MONx}, R_{SENSEx}, and R_{SETx}. V_{MONx} can by sampled with an external A/D converter to measure the channel current.

ORENx – Active high input. Pulling this pin low disables the blocking function by pulling the GAT2x pin low. Pulling this pin high (or allowing it to float high) allows the blocking function to operate normally. The M2x internal diode may carry the load current when GAT2x is low and $V_{INX} > V_{OUTX}$.

An internal 200 kΩ resistor pulls this pin to VINT. ORENx may be left open when blocking is not used, or does not require active control.

OUTx – Senses the output voltage of the channel. This voltage is used by the biasing, blocking, and power good circuits.

$\overline{PGx}$ – Active low open-drain output. A low on $\overline{PGx}$ indicates that V_{OUTx} has exceeded 10.63 V, and has not fallen below 10.50 V. These thresholds are internally set, and modifying the OUTx connection may effect blocking operation.

SENMx – Senses the voltage on the load side of R_{SENSEx} for use by the fast trip and current limiting circuits.

SENPx – Senses the voltage on the source side of R_{SENSEx} for use by the fast trip and blocking circuits. The fast trip overcurrent shutdown is activated at a $V_{SENP-SENM}$ of 0.1 V.

SETx – A resistor connected from this pin to SENPx sets the current limit level in conjunction with R_{SENSEx} and R_{MONx} as described in Equation 1 through Equation 4.

VINT – This pin connects to the internal 2.35 V rail. A 0.1 µF capacitor must be connected from this pin to ground. VINT is not designed to be a general-purpose bias rail.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs TEMPERATURE

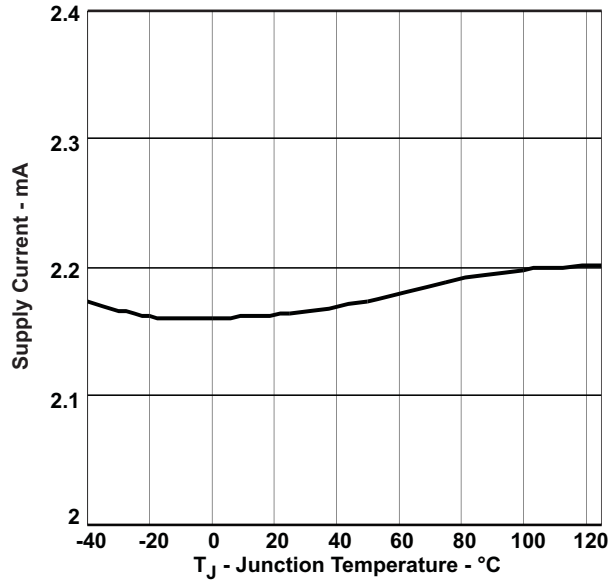


Figure 6.

SUPPLY CURRENT vs INPUT VOLTAGE

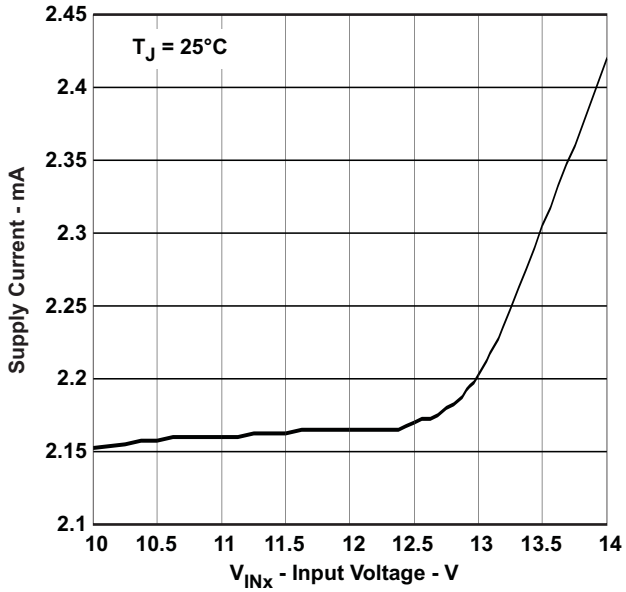


Figure 7.

CURRENT LIMIT THRESHOLD vs TEMPERATURE

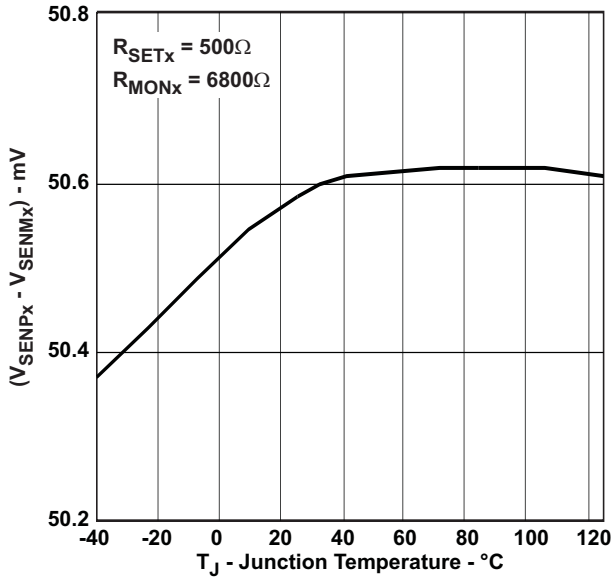


Figure 8.

BLOCKING TURNOFF THRESHOLD vs TEMPERATURE

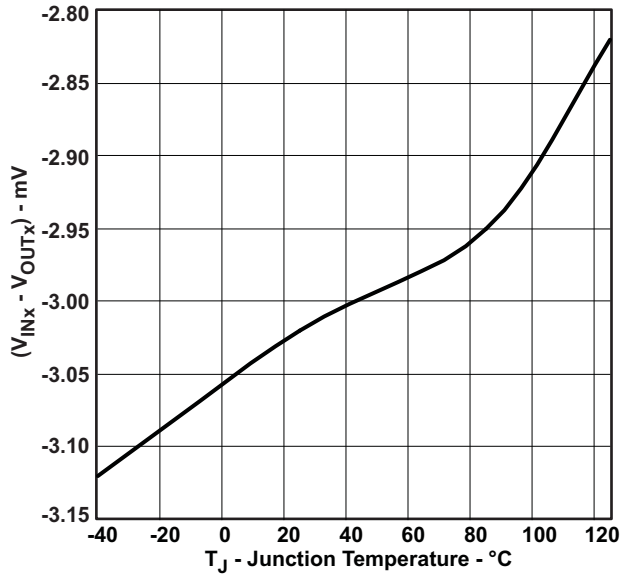


Figure 9.

TYPICAL CHARACTERISTICS (continued)

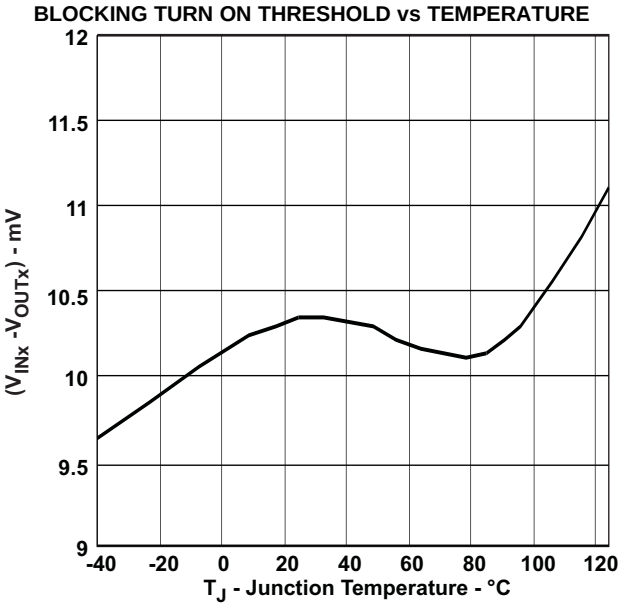


Figure 10.

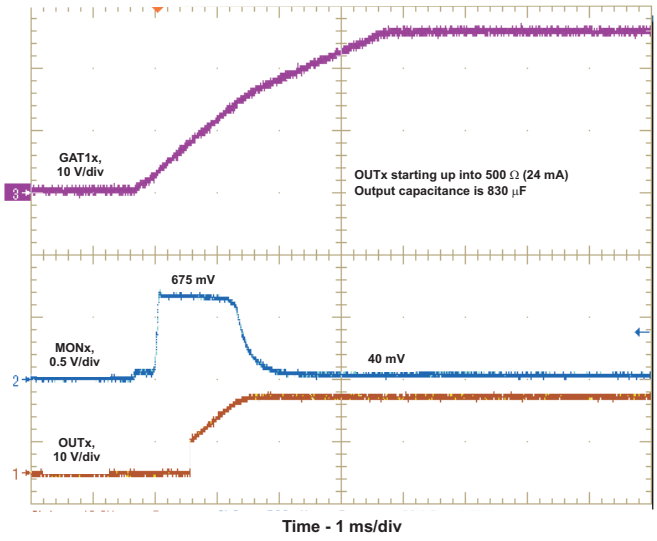


Figure 11. Startup into 500 Ω, 830 µF Load

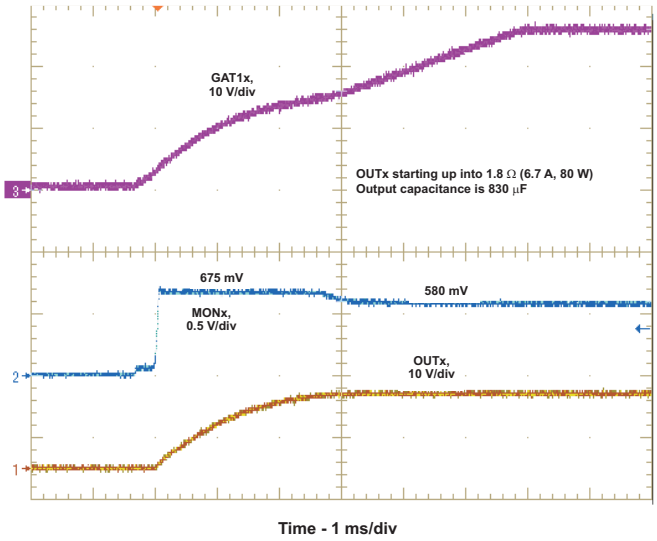


Figure 12. Startup into 80 Watt, 830 µF Load

TYPICAL CHARACTERISTICS (continued)

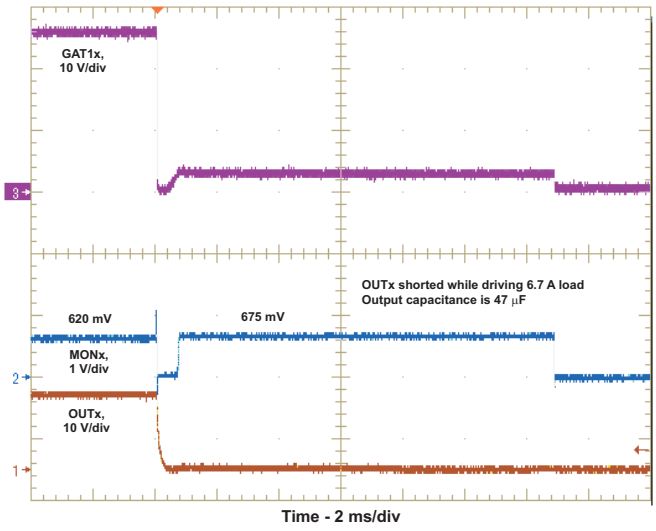


Figure 13. Short Circuit Under Full Load (6.7 A) Wide

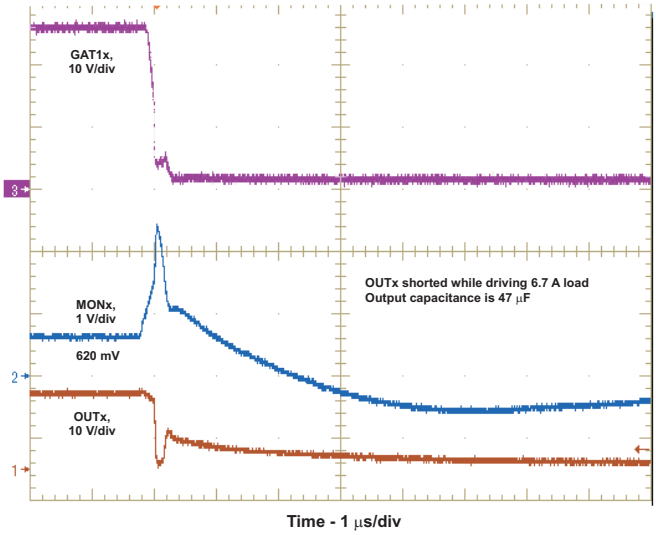


Figure 14. Short Circuit Under Full Load (6.7 A) Zoom View

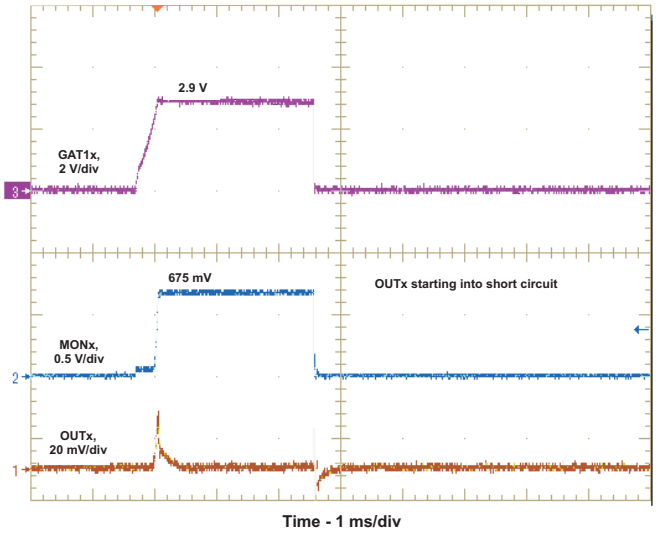


Figure 15. Startup into Short Circuit

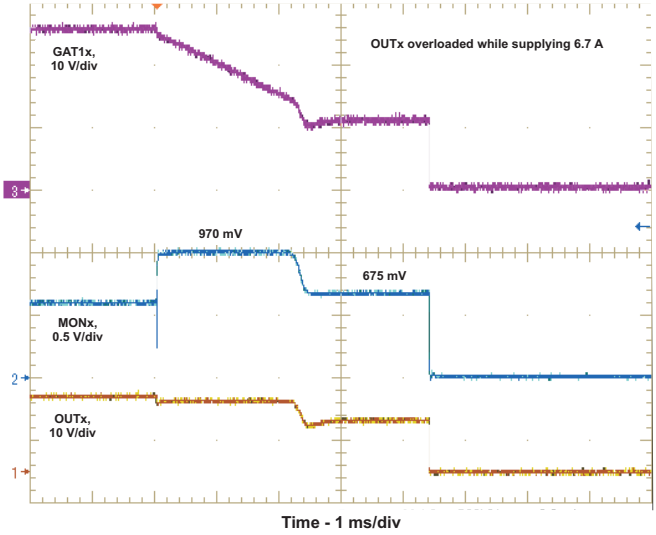


Figure 16. Overloaded while Supplying 6.7 A

SYSTEM OPERATION

INTRODUCTION

The TPS2456 controls two 12-V channels, or power paths. The channels can draw from a single common supply, or from two independent supplies. The following sections describe the TPS2456 operation and provide guidance for designing systems around this device.

CONTROL LOGIC AND POWER-ON RESET

The TPS2456 circuitry draws bias power from any of the INx or OUTx pins through an internal preregulator that generates VINT. A bypass capacitor from VINT to ground provides decoupling and output filtering for the internal circuits. Bias supply ORing allows the internal circuitry to function regardless of which channels receive power or are in a faulted state. The four external MOSFET drive pins (GAT1A, GAT1B, GAT2A, and GAT2B) are held low during startup to ensure that the channels remain off. When the voltage on the internal VINT rail exceeds approximately 1 V, the power-on reset (POR) circuit initializes the TPS2456 and allows normal operation.

ENABLE FUNCTIONS

The TPS2456 has two external enable pins for each of the channels.

The GAT1x and GAT2x pins are held low when the ENx pin is low. A high on ENx enables GAT1x for normal control by the startup and protection features. Toggling ENx low, then high, clears a latch-off condition after a fault has occurred on the channel.

The GAT2x pin is held low when the ORENx or ENx pins are low. The reverse blocking comparator-driven state machine controls GAT2x when ORENx and ENx pins are high.

ENx	ORENx	PROTECTION (M1x, GAT1x)	BLOCKING (M2x, GAT2x)
0	0	Disabled (low)	Disabled (low)
0	1	Disabled (low)	Disabled (low)
1	0	Enabled	Disabled (low)
1	1	Enabled	Enabled

Each of the four enable pins has an internal 200 kΩ pullup resistor to VINT.

POWER GOOD ($\overline{PGx}$) OUTPUTS

The TPS2456 provides an active-low open-drain Power Good ($\overline{PGx}$) output for each channel. $\overline{PGx}$ goes low (output good indication) for rising V_{OUTx} exceeding 10.63 V and $\overline{PGx}$ goes high for falling V_{OUTx} below 10.5 V. A 100 µs deglitch filter aids in avoiding false indications due to noise.

FAULT ($\overline{FLTx}$) OUTPUTS

The TPS2456 provides an active-low open-drain fault output for each channel. The $\overline{FLTx}$ output pulls low when the channel has remained in current limit long enough for the fault timer to expire (V_{CTx} > 1.35 V). A channel experiencing a fault timeout shuts down and latches off. Toggle the faulted channel's ENx low and high to clear the fault and re-enable the channel.

CURRENT LIMIT AND FAST TRIP THRESHOLDS

Load current is monitored by sensing the voltage across R_{SENSEx}, whose values typically lie in the range of 4 mΩ to 10 mΩ. Each channel features two distinct thresholds, a current-limit threshold and a fast-trip threshold.

The current limit threshold sets the regulation point of a feedback loop. If the current flowing through the channel exceeds the current limit threshold, V_{GAT1x} is reduced, forcing the MOSFET into linear operation. This causes the current flowing through the channel to settle to the value determined by the current limit threshold. For example, when a module first powers up, it draws an inrush current to charge its load capacitance. The current-limit loop ensures that this inrush current does not exceed the current limit threshold. M1 will dissipate much more power in current limit than during normal operation. The fault timer circuit limits the interval M1 operates in this condition.

There is a delay before channel current is regulated following the onset of an overload during normal operation. The current limit circuit is able to sink 30 µA from the protection MOSFET gate. The delay is the result of the MOSFET's C_{ISS} discharge from (V_{INx} + 13 V) to (V_{INx} + V_{T_M1x}) where V_{T_M1x} is the protection MOSFET's threshold voltage. Overloads between the current limit and the fast trip threshold will be permitted for this period. This is demonstrated by Figure 16. Currents above the fast trip threshold are handled by rapidly turning the protection MOSFET off with a strong gate pulldown that is driven by a 10 µs oneshot. The fault timer starts and the gate is allowed to rise after the oneshot completes in what resembles a normal startup.

The fast trip threshold protects the MOSFET and channel components against a severe short that creates a high current faster than the current-limit loop can control. If (V_{SENPx} – V_{SENMx}) exceeds the 100 mV fast trip threshold, GAT1x and GAT2x are immediately pulled to GND for a minimum of 10µs. The channel turns back on slowly, allowing the current limit feedback loop time to take over. The fault timer period limits the duration the MOSFET will see this stress. This is demonstrated by Figure 13 and Figure 14.

When the TPS2456 protects a supply output in configurations that allow the loads to hotplug, pay special attention to coordinating load surges (due to input capacitance) and the fast trip threshold. The fast trip threshold may need to be set 2–5 times higher than the current limit to accommodate this. Care must also be taken if the INx voltages can have fast rising transients. The resulting charge current to capacitors on OUTx can potentially exceed the fast trip threshold.

FAST TRIP AND CURRENT LIMITING

Figure 17 shows a simplified block diagram of the fast trip and current limit circuitry. Each channel requires an external N-channel protection MOSFET and three external resistors. These resistors allow the user to independently set the fast trip threshold and the current limit threshold, as described below.

The fast trip function is designed to protect the channel against short-circuit events. If the voltage across R_{SENSEx} exceeds 100 mV, the TPS2456 immediately turns off the protection MOSFET, M1x. The nominal fast trip limit I_{FTx} is defined in Equation 1.

$$I_{FTx} = \frac{100\ mV}{R_{SENSEx}} \tag{1}$$

The current limit circuit regulates V_{GAT1x} to control the channel current from exceeding I_{LIMITx}. The current limit circuitry includes two amplifiers, A_1 and A_2, as shown in Figure 17 and Figure 4. Amplifier A_1 forces the voltage across external resistor R_{SETx} to equal the voltage across external resistor R_{SENSEx}. The current that flows through R_{SETx} also flows through external resistor R_{MONx}, generating a voltage on the MONx pin per Equation 2.

$$V_{MONx} = \left(\frac{R_{SENSEx} \times I_{SENSEx}}{R_{SETx}} \right) \times R_{MONx} \tag{2}$$

Amplifier A_2 implements a slow-reacting current limit. As long as V_{MONx} is less than 0.675 V, GAT1x operates normally. When V_{MONx} exceeds 0.675 V, amplifier A_2 causes a small current to be drawn from GAT1x. The gate-to-source voltage of M1x drops until load current is reduced and the two inputs of amplifier A_2 balance. The current flowing through the channel then equals I_{LIMITx} per Equation 3.

$$I_{LIMITx} = \left(\frac{R_{SETx}}{R_{MONx} \times R_{SENSEx}} \right) \times 0.675\ V \tag{3}$$

$$R_{SETx} = \frac{I_{LIMITx} \times R_{MONx} \times R_{SENSEx}}{0.675\ V} \tag{4}$$

The recommended value of R_{MONx} is 6.81 kΩ. This resistor should be greater than 675 Ω to prevent excessive currents from flowing through the internal circuitry.

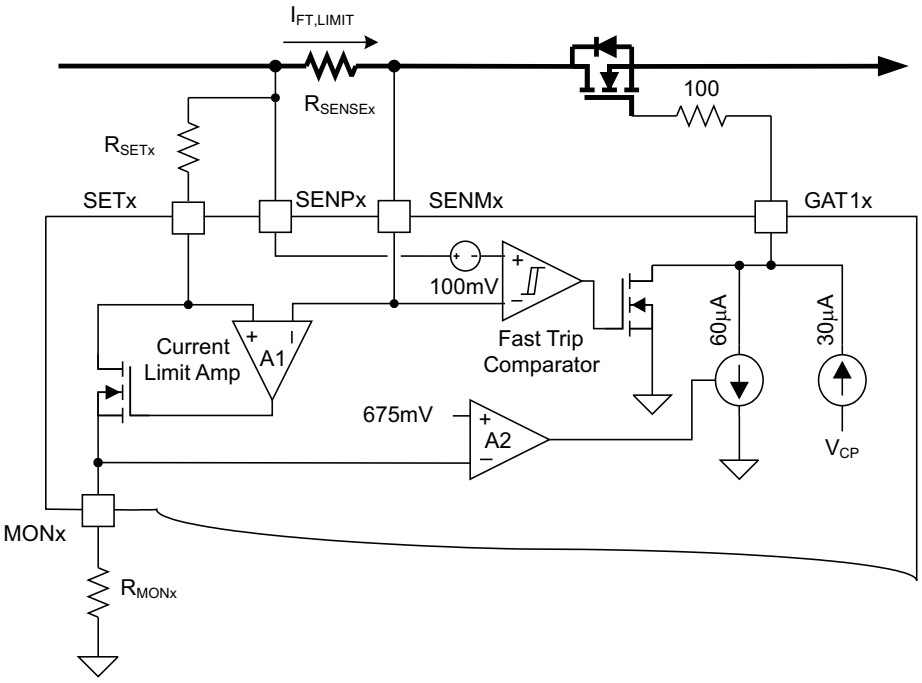


Figure 17. Over-Current Protection Circuitry

TURN ON AND INRUSH SLEW RATE CONTROL

One of the main functions of a protection device is to provide a method of hot-plugging and starting up a unit in a low-stress and controlled manner. Starting includes the ability to charge the output capacitance (on OUTx) without overburdening the input power bus while minimizing the stress on the protection MOSFET. Two possible charge-rate control methods are possible with the TPS2456, current limited and gate dv/dt controlled.

As normally configured, the gate dv/dt turn-on slew rate is described by Equation 5.

$$\frac{dV_{GAT1x}}{dt} \cong \frac{I_{GAT1x(sourcing)}}{C_{Gate\text{-}M1x}} \tag{5}$$

where $I_{GAT1x(sourcing)}$ equals the current sourced by the GAT1x pin (nominally 30 µA) and $C_{Gate\text{-}M1x}$ is the reverse transfer capacitance, C_{RSS}. Average C_{RSS} may be approximated using the MOSFET V_{GATE} vs. Q_g graph as $C_{RSS} = \Delta Q_g / V_T$ where ΔQ_g is the width of the plateau region and V_T is the gate plateau voltage. To simplify the calculation, the MOSFET gate capacitances are assumed to be fixed, while in reality, there is a voltage dependency. The output voltage tracks V_{GATE_M1x} once it has exceeded the MOSFET threshold voltage if current limit is not active. The inrush current is defined by the following equation for a purely capacitive load. Startup of a switching converter load during inrush should be avoided by use of PGx to control the converter.

$$I_{INx\_INRUSH} = \frac{dV_{OUTx}}{dt} \times C_{OUTx} = \frac{dV_{GAT1x}}{dt} \times C_{OUTx} \tag{6}$$

The actual inrush current is the lesser of the current limit (Equation 3) or dv/dt-limited inrush current.

To reduce the slew rate, increase $C_{Gate\text{-}M1x}$ by connecting additional capacitance from GAT1x to ground. Place a resistor of at least 1000 Ω in series with the additional capacitance to prevent it from interfering with the fast turn off of the MOSFET.

FAULT TIMER PROGRAMMING

Each channel requires an external capacitor C_{Tx} connected between the CTx pin and ground. The TPS2456 sources 10 µA into C_{Tx} when the gate voltage is low ((V_{GAT1x} – V_{INx}) < 6 V). The timer circuit interprets a low V_{GAT1x} as an indication that current limit is active. The TPS2456 pulls GAT1x and GAT2x to ground and latches the channel off if current limit persists long enough for V_{CTx} to reach 1.35 V. C_{Tx} is discharged through a nominal 200 Ω pull-down resistor when (V_{GAT1x} – V_{INx}) > 6 V) and $\overline{FLTx}$ is not active. The nominal fault time t_{fx} is defined by Equation 7.

$$t_{fx} = \frac{1.35\ V}{10\ \mu A} \times C_{Tx}$$

OR

$$C_{Tx} = \frac{t_{fx} \times 10\ \mu A}{1.35\ V} = t_{fx} \times 7.4 \times 10^{-6} \quad (7)$$

Converter startup typically sets the minimum t_{fx}. There are three important intervals to consider when calculating the time to set t_{fx}, initial charge of the MOSFET gate to the threshold voltage, the interval as V_{OUTx} rises to V_{INx}, and the interval for V_{GAT1x} to exceed V_{INx} by 6 V. Assume that a constant C_{ISS} is charged in the first and third periods since the MOSFET drain and source voltages do not change. The middle period may be controlled by either current limit or gate dv/dt limit as previously discussed. Let V_{TM1x} be the MOSFET gate voltage to sustain the inrush current.

Gate dv/dt Limited Inrush

$$t_{INRUSH} = \frac{C_{ISS\_M1x} \times V_{TM1x}}{I_{GAT1x}} + \frac{C_{RSS\_M1x} \times V_{IN1x}}{I_{GAT1x}} + \frac{C_{ISS\_M1x} \times \left(6\ V - V_{T\_M1x}\right)}{I_{GAT1x}}$$

Current Limited Inrush

$$t_{INRUSH} = \frac{C_{ISS\_M1x} \times V_{TM1x}}{I_{GAT1x}} + \frac{C_{OUTx} \times V_{IN1x}}{I_{LIMITx}} + \frac{C_{ISS\_M1x} \times \left(6\ V - V_{T\_M1x}\right)}{I_{GAT1x}} \quad (8)$$

Many of these parameters have wide tolerance, thus, the above approximation provides an initial estimate. Provide sufficient margin in the C_{Tx} selection to assure the channel starts reliably while not becoming overly long. Shorter fault times reduce the stresses imposed on the protection MOSFET under fault conditions, permitting the use of smaller, less expensive protection MOSFETs.

ENx RESET PERIOD

The TPS2456 will latch off after a current limit that persists long enough to trip the fault timer. The TPS2456 may be re-enabled by cycling the ENx false (low), then high. There is a minimum low period required to fully reset C_{CTx} that is determined by the R x C period where R is the internal discharge resistance. Calculate the minimum period as $t_{ENx\_LOW\_MIN}$ = C_{CTx_MAX} x 400 Ω x 3. Assuming C_{CTx_MAX} is 22 nF at 20% tolerance, $t_{ENx\_LOW\_MIN}$ = (22 nF x 1.2) x 400 x 3 = 31.7 µs. $t_{ENx\_LOW\_MIN}$ should always be greater than 100 ns.

BLOCKING OPERATION

Each channel may use an external MOSFET (M2x) to provide reverse blocking. This feature is often used where two inputs are ORed together to a common output for redundancy. Blocking protects the common output from being drawn down if an input is shorted, and maintains the independence of both inputs. Blocking may not be required in all system topologies. The TPS2456 pulls the GAT2x pin high when $V_{(INx–OUTx)}$ exceeds 10 mV, and it pulls the pin low when this differential falls below –3 mV (V_{OUTx} is greater than V_{INx}). These thresholds provide 13 mV of hysteresis to help prevent false triggering as shown in Figure 18. This technique will allow some reverse current to flow, but provides positive detection in the event of a real fault.

The blocking MOSFET is oriented so its body diode conducts forward current and blocks reverse current. The body diode does not normally conduct current because the MOSFET turns on when the voltage differential across it exceeds 10 mV.

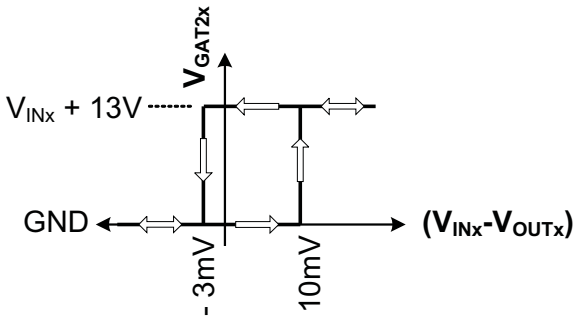


Figure 18. Blocking Thresholds

APPLICATION INFORMATION

SYSTEM DESIGN CONSIDERATIONS

The TPS2456 has two independent 12 V sections which provide protection and blocking (ORing). These sections may be used in multiple configurations.

- TPS2456 on the power input of a system
  - Two redundant input power rails to a single output (see Figure 1)
    - Blocking protects output when one of the inputs is shorted
  - Two independent loads powered by two separate or one common input rail
    - Blocking not required
  - Two redundant input rails ORed (no protection) to one common output
- TPS2456 on the power output of a system
  - Up to two output rails with protection
    - Protection isolates faulted output bus
    - Enable can be used to turn output on and off
  - Up to two output power rails with protection and blocking
    - Used where multiple outputs are tied together

The system power architecture drives the topology that best suits a particular design.

DESIGN EXAMPLE: CURRENT LIMITED START-UP

The following example is for a single channel protection circuit using current-limited inrush control. The design of the second channel would follow the same procedure and is not shown since it is redundant.

For this design example, a system board with 1000 µF of capacitance and a dc load of 1.6 Ω (or 7.5 A) must be able to be hot plugged into a 12 V main bus supply. The main bus supply has a peak fault current capability of 20 A. Operating above 20 A of current draw runs the risk of opening a circuit breaker and shutting the system down. The average current budgeted for the system board is 7.5 A under normal conditions. The main bus can supply up to 10.1 A peak for up to 10 ms during start-up or transient conditions. This procedure assumes that the inrush current is not limited by the gate charge rate. The basic system block diagram is shown in Figure 19.

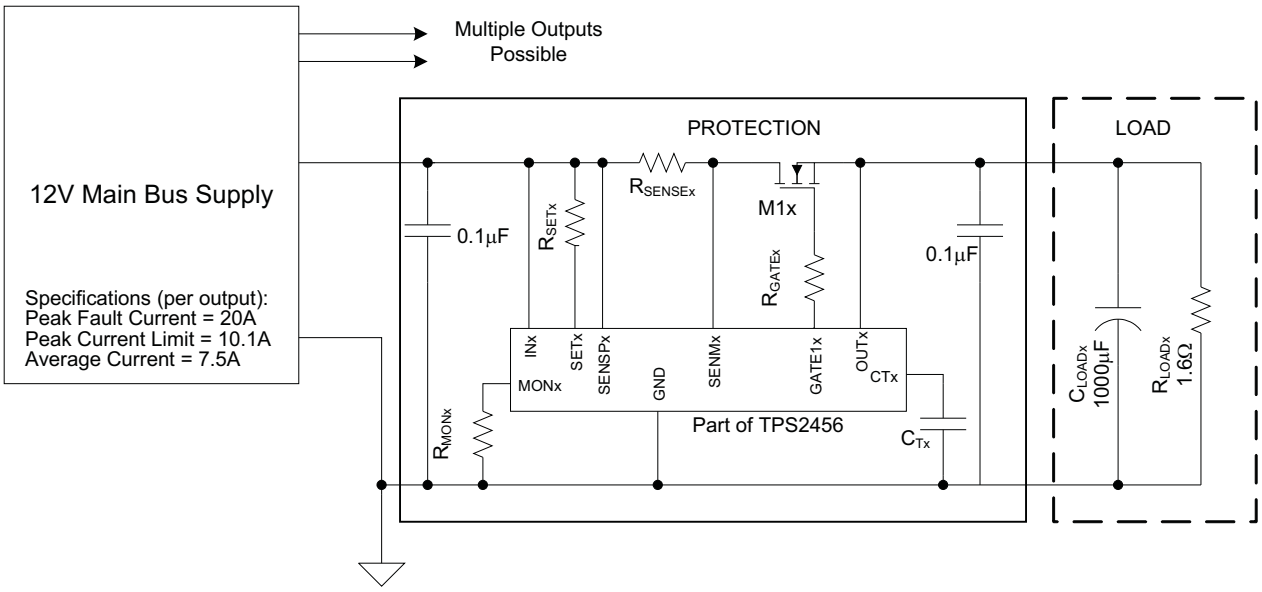


Figure 19. 12 V Main Bus

Select R_{SENSEx}

The first step is to calculate R_{SENSEx} which sets the fast current trip point, I_{FTx}. This is the maximum current that can pass through M1x and is meant to protect against short circuits. Calculate R_{SENSEx} using Equation 9 for a peak fault current (I_{FTx}) of 20 A.

$$R_{SENSEx} = \frac{100mV}{I_{FTx}} = \frac{100mV}{20A} = 5m\Omega \quad (9)$$

The R_{SENSEx} resistor is in series with the main power path and should have a power rating sufficient to support the full load current. The 12 V main bus has budgeted 10.1 A for this board, so this is the value of limit used for further calculations including the power dissipated in R_{SENSEx}. The power dissipated by R_{SENSE} is calculated using Equation 10. A higher wattage rating should be used based on local derating practice (for example 50%).

$$P_{RSENSEx} = I_{LIMITx}^2 \times R_{SENSEx} = 10.1^2 \times 5m\Omega = 0.51Watts \quad (10)$$

Select R_{SETx}

Next, R_{SETx} is calculated to set the channel current limit (I_{LIMITx}) to 10.1 A. R_{MONx} is also a variable in the calculation of R_{SETx}. Use the recommended 6.81kΩ for R_{MONx} (although other values can be used) and 10.1 A for I_{LIMITx} to calculate R_{SETx}.

$$R_{SETx} = \frac{I_{LIMITx} \times R_{MONx} \times R_{SENSEx}}{0.675V} = \frac{10.1A \times 6.81k\Omega \times 0.005\Omega}{0.675V} = 509\Omega \quad (11)$$

Choose R_{SETx} as the closest standard value, 511 Ω.

Estimate Output Charge Time

The system can provide 10.1 A of peak current for 10 ms. This current can be used for start-up of the system board as long as the output capacitance can be charged up to 12 V in less than 10 ms while also supplying current to the load resistance connected in parallel to the output capacitor. The charge time is estimated using Equation 12. For this equation, V_{OUTx} is the final nominal voltage for the board (12 V), R_{LOAD} is the dc load of the board (1.6 Ω), and there is a small amount of time for the pass transistor's gate capacitance to charge to the threshold voltage. This time, typically around 100 µs, is added to the end of the equation to provide a better estimate of the total start-up time.

$$t_{CHG} \approx -R_{LOADx} \times C_{LOADx} \times \ln\left(\frac{I_{LIMITx} \times R_{LOADx} - V_{OUTx}}{I_{LIMITx} \times R_{LOADx}}\right) + 100\mu s \quad (12)$$

$$t_{CHG} \approx -1.6\Omega \times 1000\mu F \times \ln\left(\frac{10.1A \times 1.6\Omega - 12V}{10.1A \times 1.6\Omega}\right) + 100\mu s \quad (13)$$

$$t_{CHG} \approx 2.27ms \quad (14)$$

The estimated time to charge the output is 2.27 ms. It is safe to allow the board to power up using the peak current limit because t_{CHG} is below the 10ms target.

Equation 12 assumes there is a resistive load on the output during the ramp up so the output voltage has an "RC" shape. The output capacitance charges linearly if the load is purely capacitive, simplifying the charge time equation to the following.

$$t_{CHG} = \frac{C_{LOADx} \times V_{OUTx}}{I_{LIMIT\_M1x}} + 100\mu s \quad (15)$$

Select M1x

The next design step is to select M1x. The TPS2456 is designed to use N channel MOSFETs as protection devices. The maximum MOSFET gate to source voltage rating, $V_{GS\text{-}MAX}$, must be high enough to support the highest of the gate drive (14.5 V) or input voltage.

The next factor to consider is the drain to source voltage rating, $V_{DS\text{-}MAX}$, of the MOSFET. From a dc perspective, the MOSFET needs to withstand the input power supply voltage of 12 V for this example. However; the MOSFET can be exposed to high voltage spikes during fault conditions. For this reason, a MOSFET with a substantially higher $V_{DS\text{-}MAX}$ rating improves the system reliability and provides voltage headroom for transient protection (snubber, TVS, diodes, etc.). Look for a $V_{DS\text{-}MAX}$ rating with a minimum of twice of the input power supply voltage.

Next, the dc power loss of the MOSFET must be considered. The power dissipation of the MOSFET is directly related to the $R_{DS(on)}$ of the MOSFET. The dc power dissipation for the MOSFET can be calculated using Equation 16.

$$P_{Dx} = R_{DS(on)\_M1x} \times I_{LIMITx}^2 \quad (16)$$

Taking these factors into consideration, the TI CSD16403Q5A was selected for this example. The CSD16403Q5A has a $V_{GS\text{-}MAX}$ rating of 16 V, $V_{DS\text{-}MAX}$ rating of 25 V, an $R_{DS(on)}$ of 2.2 mΩ, and an $R_{\theta JA\text{-}MAX}$ of 51 °C/W.

During normal circuit operation, the MOSFET can have up to 10.1 A flowing through, which equates to 0.22 W (I^2xR) and an 11°C rise in junction temperature (P x $R_{\theta JA\text{-}MAX}$). This is well within the data sheets limits for the MOSFET. The power dissipated during a fault (e.g. output short) is substantially larger than the steady-state power. The power handling capability of the MOSFET needs to be checked during fault conditions.

Most MOSFET data sheets provide a Safe Operating Area (SOA) plot. This plot can be used to check if the MOSFET can survive the power form a transient fault condition. Figure 20 shows the SOA curve for the QSD16403Q5A. The maximum fault current is set to 20 A for the 12 V input bus. This point can be located on Figure 20. The diagonal lines tell the length of time this transient can be safely applied to the QSD16403Q5A. The transistor can survive a 12 V, 20 A transient for approximately 9 ms.

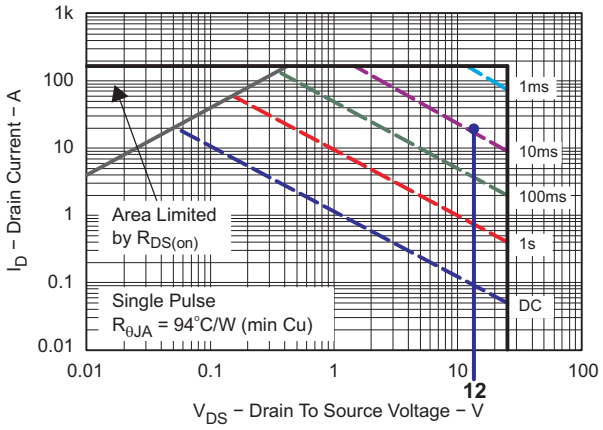


Figure 20. Drain To Source Voltage

The turn off time of the TPS2456 and MOSFET should be taken into account. The TPS2456 detects the fault condition as soon as the current through the sense resistor reaches 20 A. There is a 300 ns maximum propagation delay for the TPS2456 to start discharging the MOSFET gate. The MOSFET has an additional turn-off delay due to gate discharge (see Sinking current - Fast Discharge). The total delay for the TPS2456 and the CSD16403Q5A is approximately 310 ns. The fault current continues to rise above 20 A for this period. The rise of the fault current is determined by any inductance and resistance in the power path as well as the impedance of the input voltage source. Continuing to follow the 12 V line up on the SOA curve, it can be seen that the CSD16403Q5A could handle peak currents up to 180 A for 1 ms, giving substantial margin in this design. This makes this transistor a good choice for this application.

Output Charge Time Refinement

A more accurate charge time can be calculated using Equation 17, now that the MOSFET has been chosen. This is the same as Equation 15, but the 100 µs term is replaced with the variables that determine the time it takes to charge the gate of the MOSFET up to the threshold voltage. The threshold voltage used in this equation should be the voltage where the Mosfet starts to conduct higher currents. This can be found in the MOSFET data sheet from graphs showing I_D vs. V_{GS}. For the CSD16403Q5A, the V_{T_M1x} is 1.6 V, and C_{ISS} is 2040 pF. The term I_G in Equation 17 is the GAT1x sourcing current, typically 30 µA. Using these values, Equation 17 gives a charge time of 2.28 ms

$$t_{CHG} = -R_{LOADx} \times C_{LOADx} \times \ln\left(\frac{I_{LIMITx} \times R_{LOADx} - V_{OUTx}}{I_{LIMITx} \times R_{LOADx}}\right) + \frac{V_{T\_M1x} \times C_{ISS\_M1x}}{I_G} \quad (17)$$

Select C_{Tx}

The next step is to determine the minimum fault timer period. In the previous section, the change time calculation yielded 2.28 ms. This is the amount of time it takes to charge the output capacitor up to the final output voltage. However, the fault timer uses the difference between the input voltage and the gate voltage to determine if the TPS2456 is in current limit. The fault timer continues to run until V_{GATE_M1x} is 6 V above the input voltage. Some additional time must be added to the charge time to account for this additional gate voltage rise. The minimum fault timer time can be calculated using Equation 18.

$$t_{TMR\_MIN} = -R_{LOADx} \times C_{LOADx} \times \ln\left(\frac{I_{LIMITx} \times R_{LOADx} - V_{OUTx}}{I_{LIMITx} \times R_{LOAD}}\right) + \frac{(6\ V + V_{TM1x}) \times C_{ISS\_M1x}}{I_G} \quad (18)$$

Using the example numbers in the above equation leads to a minimum fault timer time of 2.688 ms. The fault timer must be set to a value higher than 2.688 ms to avoid turning off during start-up but lower than any maximum time limit. There is a maximum time limit set by the SOA curve of the MOSFET. Referring back to Figure 20, the CSD16403Q5A SOA curve, the MOSFET can tolerate 10.1 A with 12 V across it for approximately 20 ms. However; the input power supply can only supply the 10.1 A for 10 ms. Therefore, the fault timer should be set to between 2.688 ms and 10 ms. For this example, select 8 ms to allow for variation of system parameters such as temperature, load, component tolerance, and input voltage. The timing capacitor is calculated in Equation 19 as 59 nF. Select a the next highest standard value, 62 nF, yielding an 8.37 ms fault time.

$$C_{Tx} = \frac{t_{FAULT} \times 10\mu A}{1.35V} = \frac{0.008s \times 10\mu A}{1.35V} = 59nF \quad (19)$$

Blocking Device, M2x

Since this example uses a single channel, there is no need for the blocking MOSFET, and it can be left out of the circuit. No connection needs to be made to the GAT2x or ORENx pins.

DESIGN EXAMPLE: GATE RAMP LIMITED STARTUP

In the first example, the output capacitance is charged in current limit. In some applications, the current limit is the absolute maximum that the circuit should see, so charging the output up in current limit is not an option. In this case, it is necessary to slow down the output voltage ramp so that the current limit is not reached. This can be done by adding additional capacitance to M1x's gate.

The gate of the pass transistor is driven by a 30 µA (typical) current source. The current charges the gate to source and gate to drain (C_{rss}) capacitance, producing a voltage ramp at the gate. The time of the ramp can be lengthened by adding a capacitor, C_{ADD}, between the gate and ground. A 1 kΩ resistor should be placed in series with the additional capacitance as shown in Figure 21.

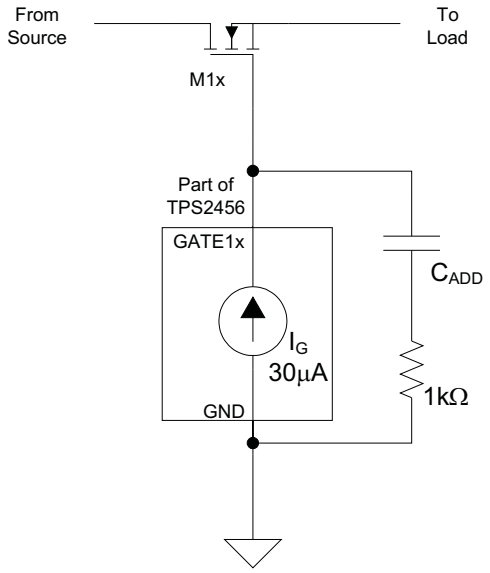


Figure 21.

With C_{ADD}, the output voltage ramp is equal to:

$$\frac{dV_{OUTx}}{dt} = \frac{dV_{GATE\_M1x}}{dt} = \frac{I_G}{C_{RSS\_M1x} + C_{ADD}} \quad (20)$$

The peak current, $I_{INX\text{-}PEAK}$, that is reached with the new ramp rate is:

$$I_{INx\_PEAK} = \frac{V_{OUTx}}{R_{LOADx}} + \frac{C_{OUTx} \times I_G}{(C_{RSS} + C_{ADD})} \quad (21)$$

C_{ADD} can be adjusted so that I_{INx_PEAK} is less than I_{LIMITx} avoiding current limit start-up. Using a controlled gate ramp requires lower peak current, but takes longer to charge the output capacitance. The length of the fault time needs to be selected to accomodate this longer ramp up time. The minimum time the fault timer should be set to is described by Equation 22.

$$t_{TMR\_MIN} = \frac{V_{T\_M1x}\left(C_{ISS} + C_{ADD}\right)}{I_G} + \frac{V_{OUTx} \times \left(C_{RSS} + C_{ADD}\right)}{I_G} + \frac{6 \times \left(C_{ISS} + C_{ADD}\right)}{I_G} \quad (22)$$

BYPASS CAPACITORS

It is a good practice to provide low-impedance ceramic capacitor bypassing of INx and OUTx. Values in the range of 10 nF to 1 µF are recommended. Some system topologies are insensitive to the values of these capacitors; however, some are not and prefer to minimize the value of the bypass capacitor.

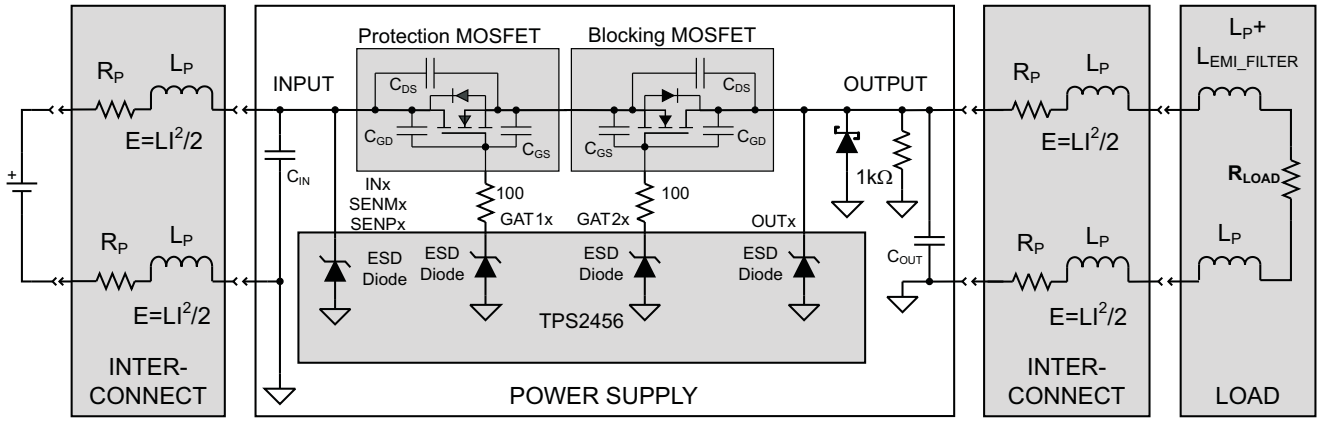
Input capacitance on a plug-in board may cause a large inrush current as the capacitor charges through the low impedance power bus when inserted. This stresses the connector contacts and causes a short voltage sag on the input bus. Small amounts of capacitance (e.g., 10 nF to 0.1 µF) are often tolerable in these systems.

Filter capacitors at the output of a redundant plug-in board are useful for controlling voltage transients, but they may can cause problems when the board is inserted into an active bus. If the output capacitor charge from an active bus is not limited, the inrush surge might engage the active supply's fast-trip shutdown. One possible solution is to put a few Ohms of resistance in series with the capacitor to limit inrush below the fast trip level.

TRANSIENT PROTECTION

If the TPS2456 is used in applications which have large input and output capacitors, voltage transients during load steps or short circuits are controlled and pose no problems.

TPS2456 devices are sometimes deployed systems that may have long, inductive feed or load interconnections. The effect of the inductance, with little local capacitance, gives rise to potential voltage transient issues. A simplified model of this is shown in Figure 22. Channel current transients may be caused by events such as hot-plug, output shorts with fast turnoff, or abrupt load changes. The combination of input inductance and an abrupt load decrease causes a positive voltage spike on the TPS2354 INPUT pins. The combination of output inductance and an abrupt load decrease will cause a negative voltage spike on the TPS2354 OUTPUT. These transients have the potential to exceed the Absolute Maximum Ratings, either damaging the TPS23754 or causing undesired operation.



NOTE: L_P = Parasitic Inductance (not all instances equal)
R_P = Parasitic Resistance (not all instances equal)

Figure 22. System Transient Model

An analysis must be performed to determine the need for transient protection. Equation 23 allows the designer to estimate the voltage spike due to current interruptions.

$$V_{SPIKE} = V_{INIT} + I_{LOAD}\sqrt{L/C} \quad (23)$$

Where:

V_{INIT} = initial voltage at terminal being analyzed before the current is interrupted
L = combined inductance of feed and RTN lines in series with interrupted current
C = capacitance at point of computation
I_{LOAD} = current immediately before circuit is opened
An approximation for the inductance of a straight wire is:
L ≈ [0.2 × length_in_meters × (In(4 × length/diameter) – 0.75)] nH

The capacitance in Equation 23, at INPUT, consists of parasitic capacitance and any intentional bypass capacitance. This implies that the transients can be controlled by the addition of sufficient capacitance. Equation 24 can be used to calculate the capacitance required to limit the voltage spike to a desired level above the nominal voltage.

$$C = \frac{L \times I_{LOAD}^2}{(V_{SPIKE} - V_{NOM})^2} \quad (24)$$

TRANSIENT PROTECTION SOLUTIONS

Typical protection solutions involve capacitors, TVSs (Transient Voltage Suppressors) and/or a Schottky diode.

A TVS and small bypass capacitor at INPUT (see Figure 22) are the most likely solutions to solve input voltage overshoot. The TVS must be selected so that its clamping is below the Absolute Maximum Rating (17 V) at the anticipated fault current. For example, the SMCJ13A data sheet specifies a maximum clamping voltage of 21.5 V (which exceeds the Absolute Maximum voltage) at 69.7 A. The actual clamping voltage at the fault current (I_{FT}) may be within the Absolute Maximum; however, the clamp voltage at lower currents must be estimated to verify.

By modeling the TVS as a perfect voltage clamp in series with a resistor, the clamping voltage may be estimated at different currents per Equation 25.

$$R_{SERIES} = \frac{V_{CL\_MAX} - V_{BR\_MIN}}{I_{PEAK\_PULSE} - I_{TEST}} = \frac{21.5\ V - 14.4\ V}{69.7\ A - 1\ mA} = 0.102\ \Omega \quad (25)$$

The maximum permitted clamping current for this device is found in Equation 26. This is a worst case (low) number.

$$I_{CL\_MAX} = \frac{V_{ABS\_MAX} - V_{BR\_MAX}}{R_{SERIES}} = \frac{17\ V - 15.9\ V}{0.102} = 10.8\ A \quad (26)$$

A Schottky diode and capacitor across the OUTPUT (Figure 22) are the most likely solutions to clamp the transient energy and limit the negative voltage excursion. Although the Schottky diode absorbs most of the energy, the extremely fast di/dt at shutoff allows some of the leading edge energy to couple through the parasitic capacitances of the protection and blocking MOSFET (C_{DS}, C_{GS}, C_{GD}) to the GAT1x and GAT2x pins. Protection for these pins is provided by 100 Ω resistors which have little effect on normal operation but provide good isolation during transient events.

Equation 24 gives insight into selection of transient protection capacitors for both INPUT and OUTPUT; however, there are concerns with adding a lot of capacitance in some situations. See the BYPASS CAPACITORS section regarding considerations and limitations

PCB layout of the protection is critical to its performance. The layout should minimize the impedance between the TPS2456 and the protection in order to provide the best clamping.

OUTPUT BLEED RESISTANCE

The OUTx pin sources a small amount of current when the channel input is powered, but disabled in non-redundant configurations (output is unpowered). The leakage can be modeled as a 6 V source in series with a 280 kΩ resistor, allowing approximately 21.4 µA into a short. This leakage can charge a high-impedance load to approximately 6 V. If this is unacceptable, control the output voltage in this state by adding a load resistor from OUTx to GND. Select the resistor, R_{BLEED}, per Equation 27, where V_{BLEED} is the desired maximum output voltage. Since the model is nominal, use a 25% smaller resistor value.

$$R_{BLEED} = \frac{V_{BLEED}}{(6\ V\ -\ V_{BLEED})} \times 280\ k\Omega \quad (27)$$

CONTROLLING FAULT CURRENT in REDUNDANT POWER TOPOLOGIES

System topologies such as Figure 1 are often used to provide power source redundancy. This permits the load to run from either source, or potentially both in parallel. Blocking permits the load to operate uninterrupted in the event of either source failing open or shorting to GND. However, this topology permits the load to draw twice the channel fault current (I_{LIMITx}) for two closely matched sources.

The simple configuration of Figure 23 programs the total load fault current to a fixed value independent of the number of channel feeds to the load. The current limit thresholds now apply to the sum of the currents delivered by the redundant channels. When implementing this redundant mode, it is recommended that all of the channels use the same R_{SENSEx} and R_{SETx} values. This configuration does not foster sharing or smooth transitions between sources, it simply permits the power to flow from the higher source, but limits the maximum load current to a fixed value.

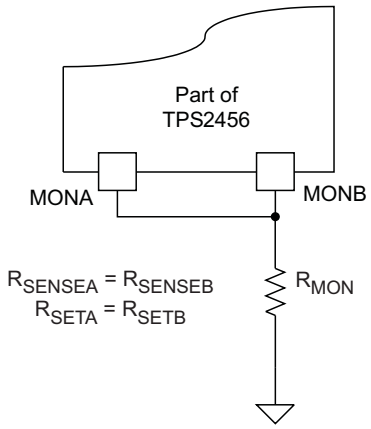


Figure 23. Fixed Fault Current Application

CURRENT FEEDBACK TO A SHELF CONTROLLER

A shelf controller can monitor channel currents by observing V_{MONx}, which is proportional to the current through R_{SENSEx}. The voltage on MONx can be directly sampled with an analog circuit (e.g. a comparator) or sampled with an Analog to Digital Converter (ADC) to provide a digital representation of the current. Figure 24 shows a typical system configuration using a multiplexer and ADC (analog to digital converter) to monitor the current in both channels of the TPS2456. It has been assumed that the normal 0 V to 0.675 V range of V_{MONx} is suitable for the ADC input. If this is not the case, operational amplifier circuits should be used to buffer and scale these signals. It is not advisable to add capacitance to the MONx pins as this effects the current-limit loop.

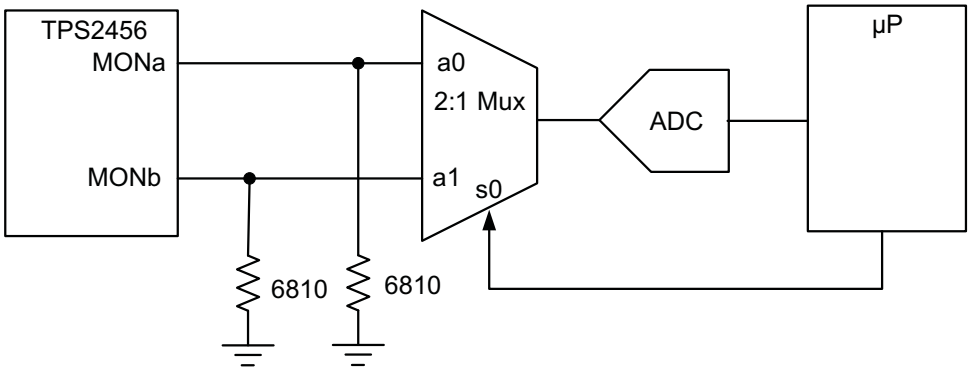


Figure 24.

The output of the MONx pin is a current proportional to the current passing through the pass transistor as defined in Equation 2. The current flowing out of the MONx pin is converted to a voltage by R_{MONx} which is typically 6.81 kΩ. Any circuitry connected to the MONx pin should either have an input impedance much higher that R_{MONx} to reduce measurement and limiting error, or the value of the parallel combination must be adjusted. The output of the MONx pin can also be buffered using a unity gain, non-inverting operational amplifier if necessary.

LAYOUT CONSIDERATIONS

TPS2456 applications require layout attention to ensure proper performance and minimize susceptibility to transients and noise. In general, all runs should be as short as possible, but the following list deserves first consideration.

1. Decoupling capacitors on INA and INB should have minimal length to the pin and to GND
2. SENMx and SENPx runs must be short and run side-by-side to maximize common mode rejection. Kelvin connections should be used at the points of contact with R_{SENSEx}. (See Figure 25)

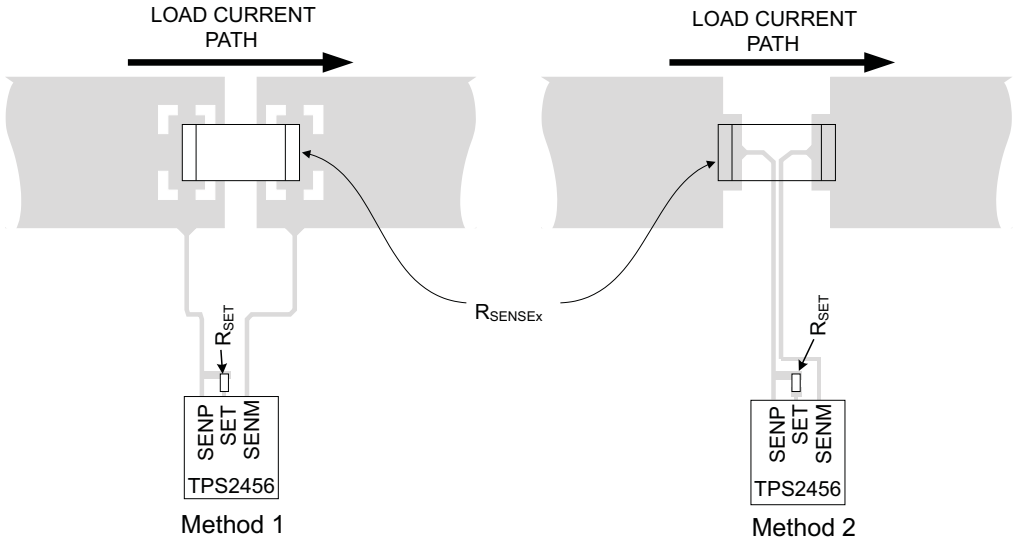


Figure 25. Recommended R_{SENSE} Layout

3. SETx runs need to be short on both sides of R_{SETx}.
4. Power path connections should be as short as possible and sized to carry at least twice the full load current, more if possible.
5. Connections to GND and MONx pins should be minimized after the connections above have been placed.
6. The device dissipates low power so soldering the powerpad to the board is not a requirement. However, doing so improves thermal performance and reduces susceptibility to noise.

7. The board should use a single point ground scheme. The current return path for both channels should be isolated from each other as much as possible and tie together at a single point. This helps to reduce ground bounce and false turn offs in one channel when there is a fault in the other channel. Also, sensitive analog grounds (such as the ground connections of $R_{MON}x$ and C_{Tx}) should be run separate from the power path grounds. This analog ground must also tie to the two power path grounds at a single point. Figure 26 shows the top layer routing of the TPS2456 EVM which uses a single point ground scheme. Each major power path, the analog ground, and the single point tying them together is highlighted in the figure.

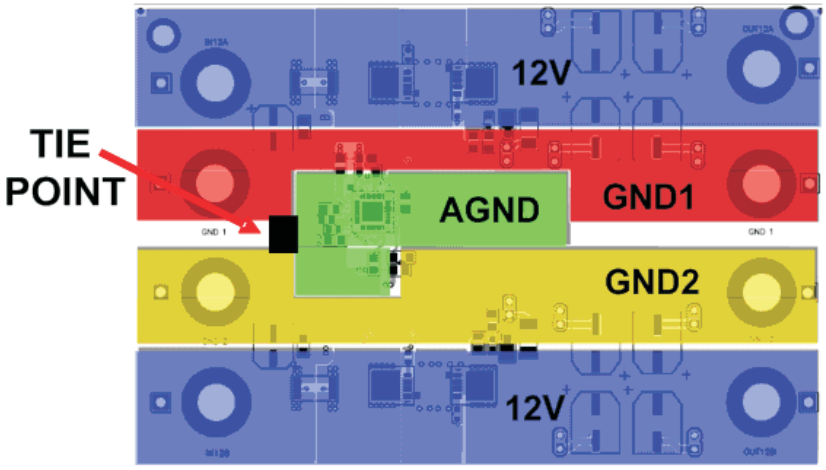


Figure 26.

8. Protection devices such as snubbers, TVS, capacitors or diodes should be placed physically close to the device they are intended to protect, and routed with short trances to reduce inductance. For example, the protection Schottky diode shown in Figure 1 should be physically close to the source of the pass transistor (or the drain of the blocking MOSFET if used).

REVISION HISTORY

Changes from Original (March 2010) to Revision A **Page**

- Changed data sheet status from Preview to Production 1
- Changed the second paragraph of the DESCRIPTION From: The ORing control uses an external MOSFET to prevent reverse current flow To: The ORing control uses an external MOSFET to block reverse current when an input is shorted. 1
- Deleted the Dissipation Rating table and added the Thermal Information table 2
- Added test to the SENPA pin of the PIN FUNCTIONS table - Connect to the source side of R_{SENSEA}. 6
- Changed PIN 32 From: GNDA To: GND and PIN 23 From: AGND To: GND in the DEVICE PINOUT illustration 7
- Changed the DETAILED PIN DESCRIPTIONS 7
- Changed Figure 8 Title From: FAST CURRENT LIMIT THRESHOLD vs TEMPERATURE To: CURRENT LIMIT THRESHOLD vs TEMPERATURE, and added R_{SETx} and R_{MONx} values 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2456RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2456RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

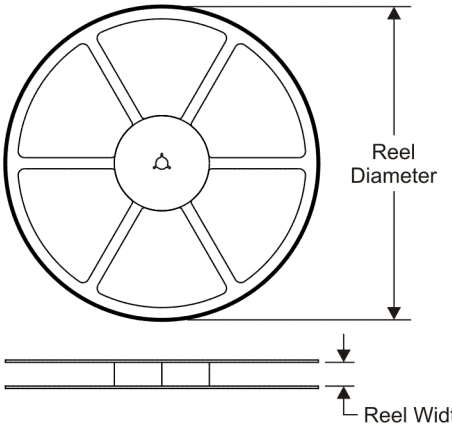
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

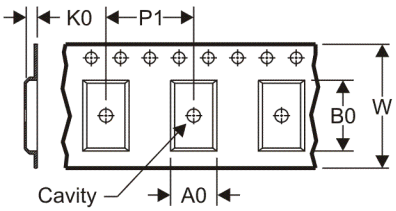
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

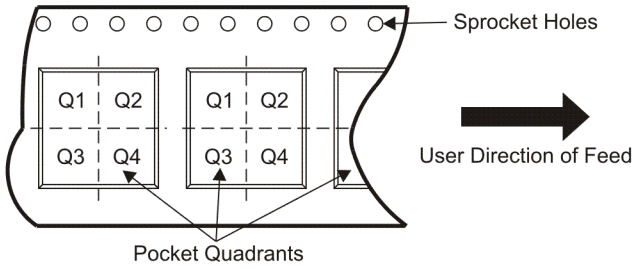


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



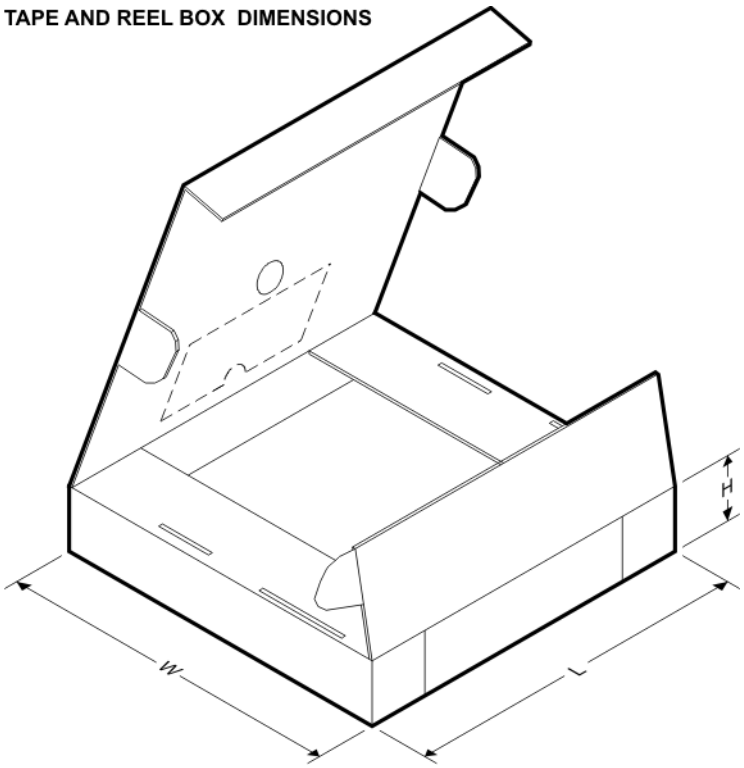
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2456RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TPS2456RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

PACKAGE MATERIALS INFORMATION

20-Jul-2010

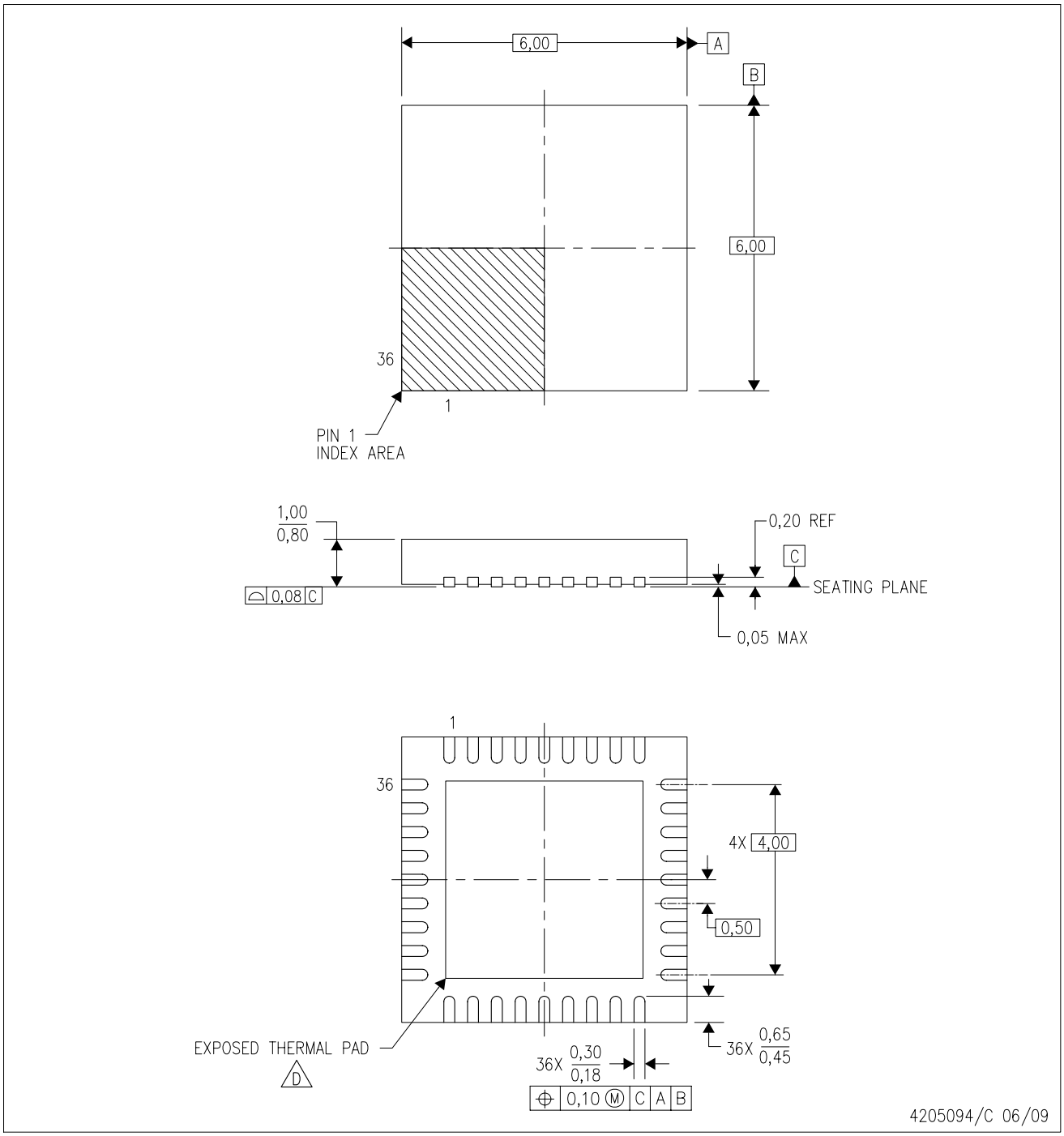
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2456RHHR	VQFN	RHH	36	2500	346.0	346.0	33.0
TPS2456RHHT	VQFN	RHH	36	250	190.5	212.7	31.8

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

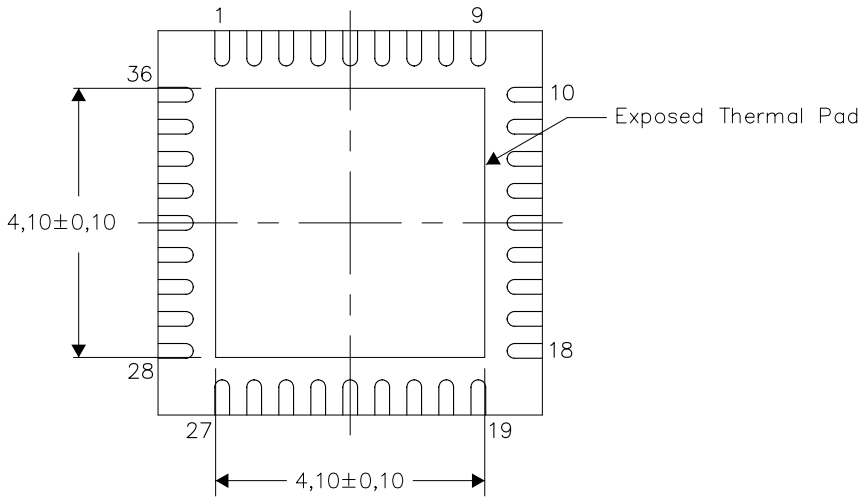
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



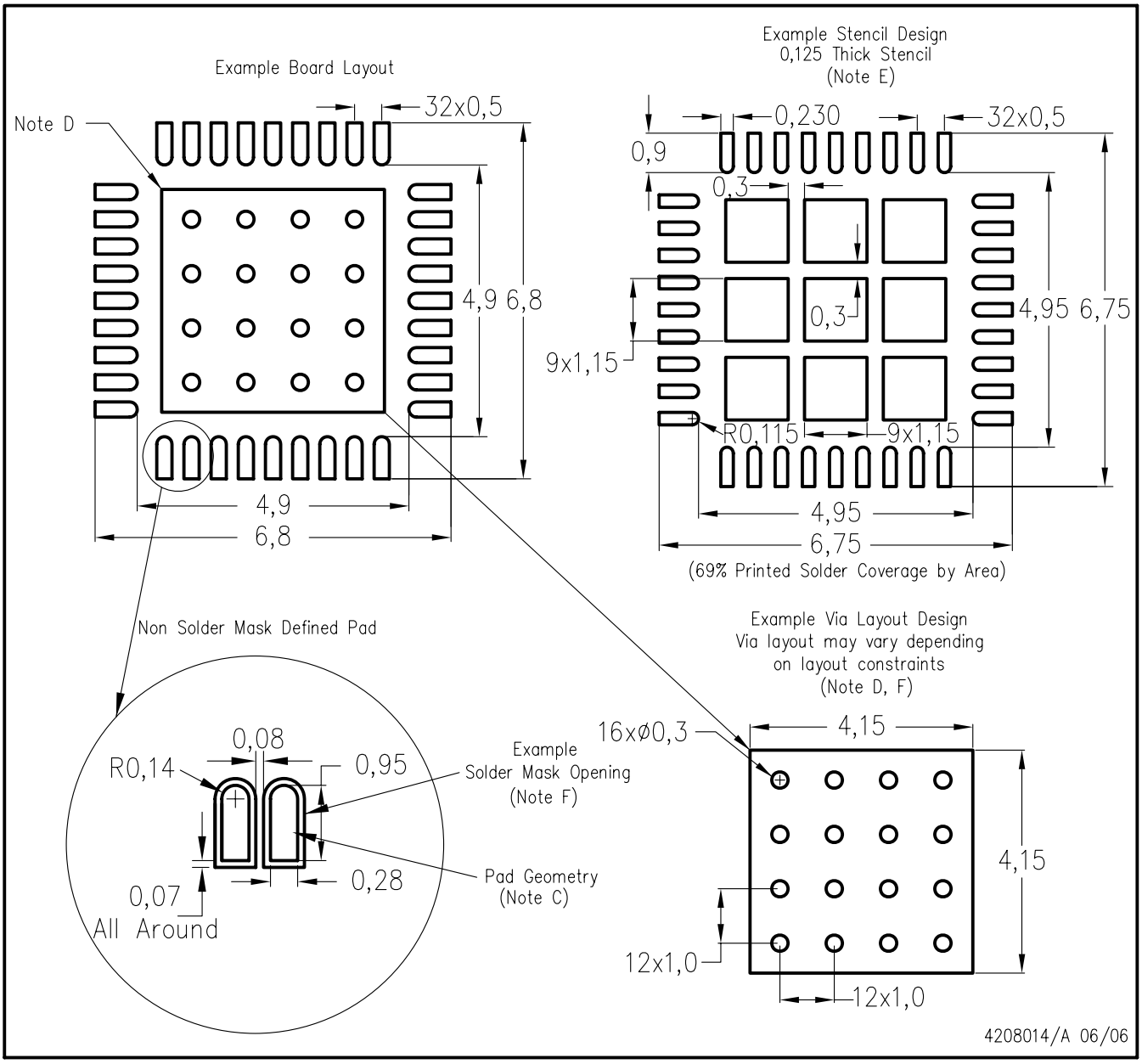
Bottom View

Exposed Thermal Pad Dimensions

4206362–3/H 09/10

NOTE: A. All linear dimensions are in millimeters

RHH (S–PQFP–N36)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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