

T-43-21

100307



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100307 Low Power Quint Exclusive OR/NOR Gate

General Description

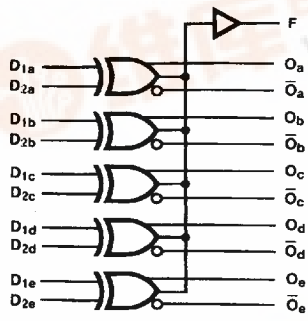
The 100307 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with 100107
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol



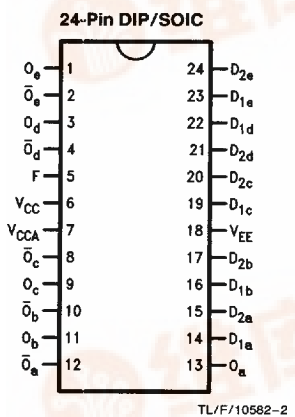
Logic Equation

$$F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$$

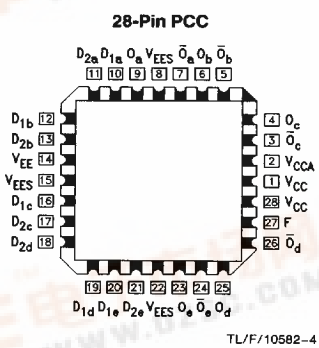
Pin Names	Description
D _{na} -D _{ne}	Data Inputs
F	Function Output
O _a -O _e	Data Outputs
O _a -O _e	Complementary Data Outputs

TL/F/10582-1

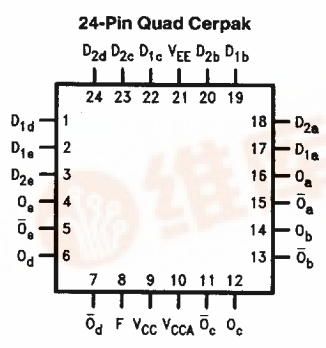
Connection Diagrams



TL/F/10582-2



TL/F/10582-4



TL/F/10582-3



106307

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG}) -65°C to +150°C

Maximum Junction Temperature (T_J):
 Ceramic +175°C
 Plastic +150°C

V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V

Input Voltage (DC) V_{EE} to +0.5V

Output Current (DC Output HIGH) -50 mA

ESD (Note 2) ≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)

Commercial 0°C to +85°C
 Industrial -40°C to +85°C
 Military -55°C to +125°C

Supply Voltage (V_{EE})

-5.7V to -4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V _{OH}	Output HIGH Voltage	-1025	-955	-870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1830	-1705	-1620	mV		
V _{OHC}	Output HIGH Voltage	-1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610	mV		
V _{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	
I _{IH}	Input HIGH Current D _{2a} -D _{2e} D _{1a} -D _{1e}			250 350	μA	V _{IN} = V _{IH} (Max)	
I _{EE}	Power Supply Current	-69	-43	-30	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T _C = 0°C		T _C = +25°C		T _C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay D _{2a} -D _{2e} to O, \bar{O}	0.55	1.90	0.55	1.80	0.55	1.90	ns	Figures 1 and 2
t _{PHL}		0.55	1.70	0.55	1.60	0.55	1.70		
t _{PLH}	Propagation Delay D _{1a} -D _{1e} to O, \bar{O}	1.15	2.75	1.15	2.75	1.15	3.00	ns	
t _{PHL}		0.35	1.20	0.35	1.20	0.35	1.20		
t _{TLH}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	
t _{THL}		0.35	1.20	0.35	1.20	0.35	1.20		

Commercial Version (Continued)

SOIC, PCC, and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O}	0.55	1.70	0.55	1.60	0.55	1.70	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O}	0.55	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Industrial Version

PCC DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$ (Note 1)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with 50Ω to $-2.0V$
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with 50Ω to $-2.0V$
V_{OLC}	Output LOW Voltage		-1565		-1610	mV		
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL}(\text{Min})$	
I_{IH}	Input HIGH Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$		250 350		250 350	μA	$V_{IN} = V_{IH}(\text{Max})$	
I_{EE}	Power Supply Current	-69	-30	-69	-30	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

100307

Industrial Version (Continued)

PCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O}	0.45	1.70	0.55	1.60	0.55	1.70	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O}	0.45	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.05	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Military Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50Ω to $-2.0V$	1, 2, 3
		-1085	-870	mV	$-55^\circ C$			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to $-2.0V$	1, 2, 3
		-1830	-1555	mV	$-55^\circ C$			
V_{OHC}	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to $-2.0V$	1, 2, 3
		-1085		mV	$-55^\circ C$			
V_{OLC}	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to $-2.0V$	1, 2, 3
			-1555	mV	$-55^\circ C$			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4	
V_{IL}	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4	
I_{IL}	Input LOW Current	0.50		μA	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$	1, 2, 3	
I_{IH}	Input High Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$		250	μA	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	1, 2, 3	
			350	μA	$-55^\circ C$			
I_{EE}	Power Supply Current	-75	-25	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open	1, 2, 3	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking to guarantee junction temperature equals $-55^\circ C$, then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version (Continued)

AC Electrical Characteristics

$V_{EE} = -4.25V$ 查询 100307 DCA 供应商

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O}	0.30	2.10	0.40	1.90	0.40	2.40	ns	Figures 1 and 2	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O}	0.30	1.90	0.40	1.80	0.40	2.20	ns		
t_{PLH} t_{PHL}	Propagation Delay Data to F	0.80	2.90	0.90	2.80	0.90	3.40	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.70	0.30	1.60	0.20	1.70	ns		4

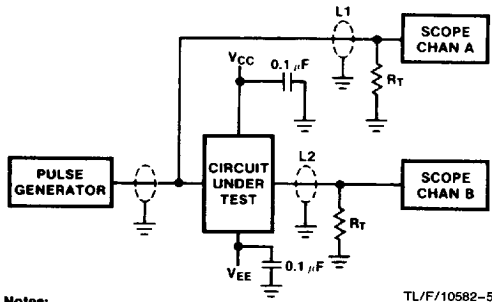
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $-25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Test Circuitry



TL/F/10582-5

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

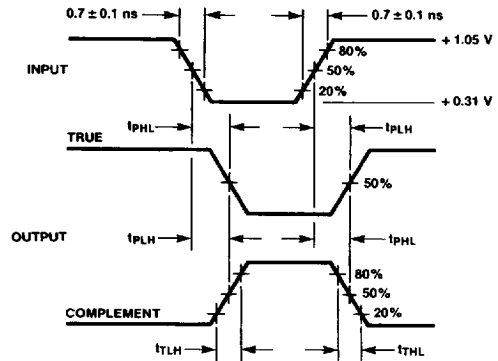
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance $\leq 3 pF$

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10582-6

FIGURE 2. Propagation Delay and Transition Times