SN74LVC1G06-EP SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

SCES669A-JULY 2006-REVISED MARCH 2007

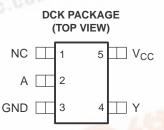
查询**"\$*******400**C1G06-EP"供应商

FEATURES

- Controlled Baseline
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- Extended Temperature Performance of –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Available in the Texas Instruments
 NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Input and Open-Drain Output Accept
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

Voltages up to 5.5 V

- Max t_{pd} of 4 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1G06 is a single inverter buffer/driver that is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G06 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

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SN74LVC1G06-EP SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

SCES(19)AS NUTX 12006 FIEV ISED MARCH 2007 1



ORDERING INFORMATION(1)

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
-55°C to 125°C	SOT (SC-70) - DCK	Reel of 3000	SN74LVC1G06MDCKREP ⁽⁴⁾	СВА

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
- Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- The actual top-side marking has one additional character that designates the assembly/test site.
- (4) Product Preview

FUNCTION TABLE

INPUT A	OUTPUT Y
Н	Г
L	Н

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V _I	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-	impedance or power-off state ⁽²⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the high	or low state ⁽²⁾⁽³⁾	-0.5	6.5	V
I _{IK}	Input clamp current	V _I < 0 V		-50	mA
I _{OK}	Output clamp current	V _O < 0 V		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			252	°C/W
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed. (3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
\/	Cupply voltage	Operating	1.65	5.5	V
V _{CC} Supply voltage		Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
\/	High lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
V _{IH} High-level input voltage	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

WITH OPEN-DRAIN OUTPUT

SCES669A-JULY 2006-REVISED MARCH 2007

Recommended Operating Conditions (continued)

			MIN	MAX	UNIT
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V	Low level input valtage	V _{CC} = 2.3 V to 2.7 V		0.7	V
V_{IL}	Low-level input voltage	w-level input voltage $V_{CC} = 3 \text{ V to 3.6 V}$		0.8	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		0.3 × V _{CC}		
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	5.5	V
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current	V 2 V		16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	
T _A	Operating free-air temperature		-55	125	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	R	TEST C	ONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
		I _{OL} = 100 μA	1.65 V to 5.5 V			0.1		
		I _{OL} = 4 mA	1.65 V			0.45		
		I _{OL} = 8 mA	2.3 V			0.3	.,	
V _{OL}		I _{OL} = 16 mA	0.1/			0.4	V	
		I _{OL} = 24 mA	3 V			0.55		
		I _{OL} = 32 mA	4.5 V			0.55		
I _I A inp	out	V _I = 5.5 V or GND		0 V to 5.5 V			±1	μA
I _{off}		V_I or $V_O = 5.5 \text{ V}$		0 V			±10	μA
I _{CC}		$V_I = 5.5 \text{ V or GND},$	I _O = 0	1.65 V to 5.5 V			10	μΑ
ΔI _{CC}		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 5.5 V			500	μΑ
Ci		$V_I = V_{CC}$ or GND		3.3 V		4		pF
Co		$V_O = V_{CC}$ or GND		3.3 V		5		pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	ARAMETER FROM (INPUT)		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = ± 0.2		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Y	2.2	8	1.1	6	1.2	6	1	5.5	ns

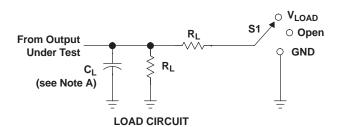
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	$V_{CC} = 3.3 \text{ V}$	V _{CC} = 5 V	UNIT
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	ONII
C_{pd}	Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF

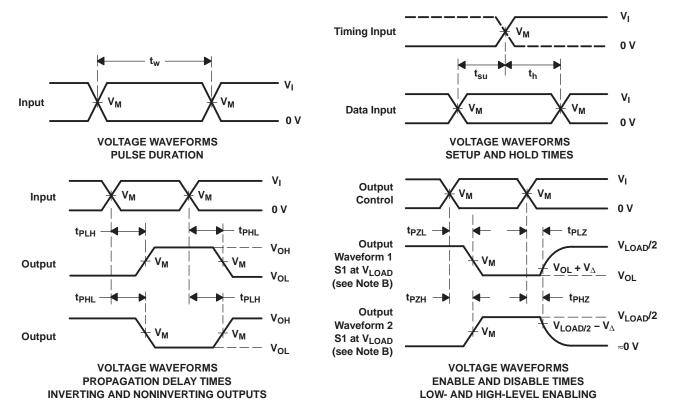


PARAMETER MEASUREMENT INFORMATION (Open Drain)



TEST	S1
t _{PZL} (see Notes E and F)	V _{LOAD}
t _{PLZ} (see Notes E and G)	V _{LOAD}
t _{PHZ} /t _{PZH}	V_{LOAD}

	IN	IPUT			_		
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_{\Delta}$
1.8 V \pm 0.15 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	V _{CC}	≤ 2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- F. t_{PZL} is measured at V_M.
- G. t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins F	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G06MDCKREP	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06655-01XE	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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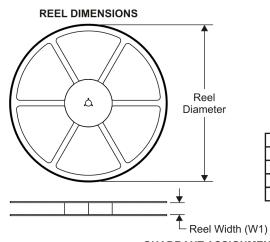
Catalog: SN74LVC1G06

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

16-Aug-2008

TAPE AND REEL INFORMATION





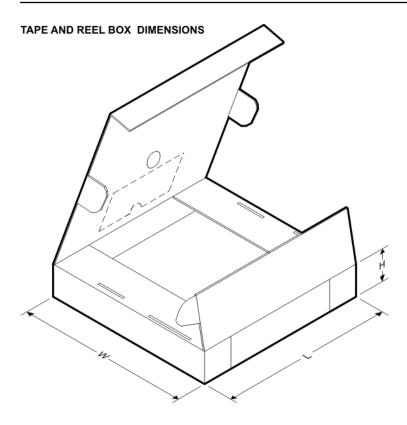
Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G06MDCKREP	SC70	DCK	5	3000	180.0	9.2	4.0	2.24	2.34	4.0	8.0	Q3

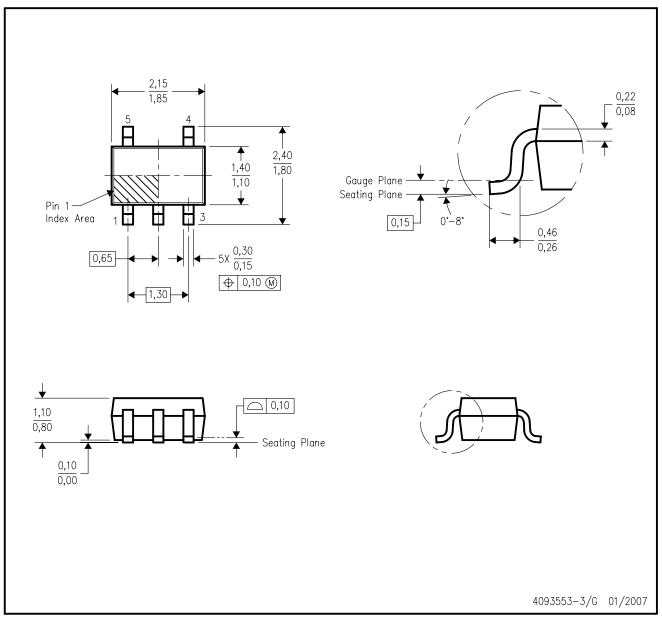


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G06MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



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