High-Voltage Switchmode Regulator

FEATURES

- 10- to 120-V Input Range
- Current-Mode Control
- On-Chip 200-V, 5-Ω MOSFET Switch
- $\overline{\text{SHUTDOWN}}$ and RESET
- High Efficiency Operation (>80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

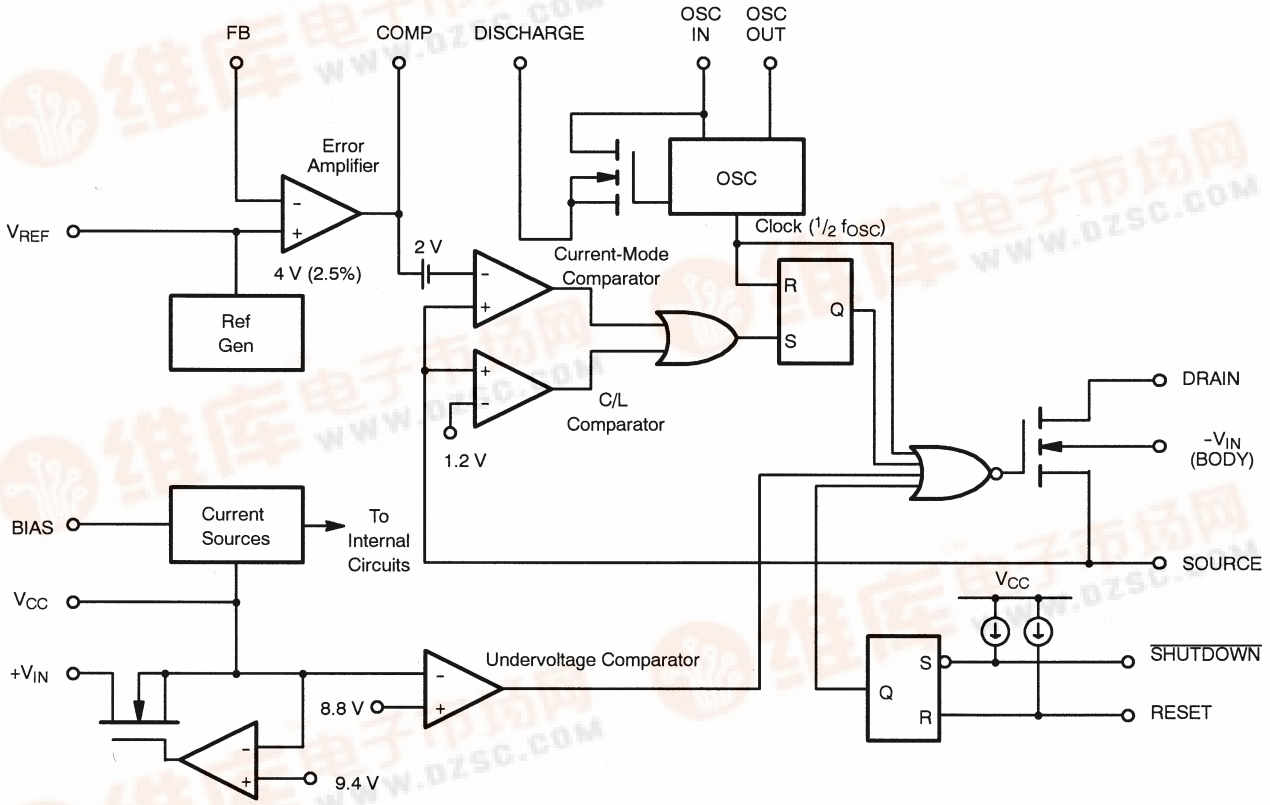
DESCRIPTION

The Si9104 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9104 is available in a 16-pin wide-body SOIC and is specified over the D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} . . . . . 15 V
$+V_{IN}$ . . . . . 120 V
V_{DS} . . . . . 200 V
I_D (Peak) (300 µs pulse, 2% duty cycle) . . . . . 2 A
I_D (rms) . . . . . 250 mA
Logic Inputs (RESET, SHUTDOWN, OSC IN) . . -0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) . . . . . -0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) . . . . . 3 mA
Storage Temperature . . . . . -65 to 125°C
Operating Temperature . . . . . -40 to 85°C
Junction Temperature (T_J) . . . . . 150°C
Power Dissipation (Package)[a]
16-Pin Plastic Wide-Body SOIC[b] . . . . . 900 mW
Thermal Impedance (Θ_{JA})
16-Pin Plastic Wide-Body SOIC . . . . . 140°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC} . . . . . 10 V to 13.5 V
$+V_{IN}$ . . . . . 10 V to 120 V
f_{OSC} . . . . . 40 kHz to 1 MHz
R_{OSC} . . . . . 25 kΩ to 1 MΩ
Linear Inputs . . . . . 0 to 7 V
Digital Inputs . . . . . 0 to V_{CC}

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	Limits D Suffix -40 to 85°C Temp[b]	Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = - V_{IN} (OSC Disabled) R_L = 10 MΩ	Room Full	3.92 3.85	4.0	4.08 4.15	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	V_{REF} = $-V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.25	1.0	mV/°C
Long Term Stability[e]		t = 1000 hrs., T_A = 125°C	Room		5	25	mV
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 kΩ[f]	Room	80	100	120	kHz
		R_{OSC} = 150 kΩ[f]	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) - f(10 V) / f(10 V)	Room	4	10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = - V_{IN} (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = - V_{IN}, V_{FB} = 4 V	Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = - V_{IN} (OSC Disabled)	Room		±15	±40	mV
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room	0.7	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		-2.0	-1.4	mA
		Sink (V_{FB} = 4.5 V)	Room	0.12	0.15		
Power Supply Rejection	PSRR	10 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB

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Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC}, V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1.	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room	120			V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq$ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	9.4	9.8	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.3	
V_{REG} - V_{UVLO}	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2.	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3.	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width[e] $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = V_{CC}	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	-35	-25		
MOSFET Switch							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On-Resistance[g]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 150 V	Room		5	10	µA
Drain Capacitance[e]	C_{DS}		Room		35		pF

Notes

a. Refer to PROCESS OPTION FLOWCHART for additional information.

b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

e. Guaranteed by design, not subject to production test.

f. C_{STRAY} @ OSC IN ≤ 5 pF.

g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

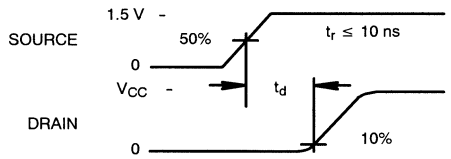


FIGURE 1.

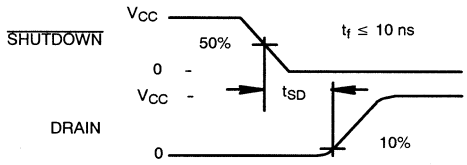


FIGURE 2.

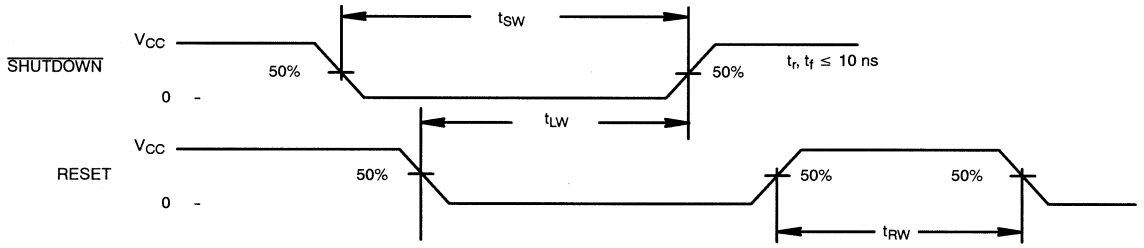


FIGURE 3.

TYPICAL CHARACTERISTICS

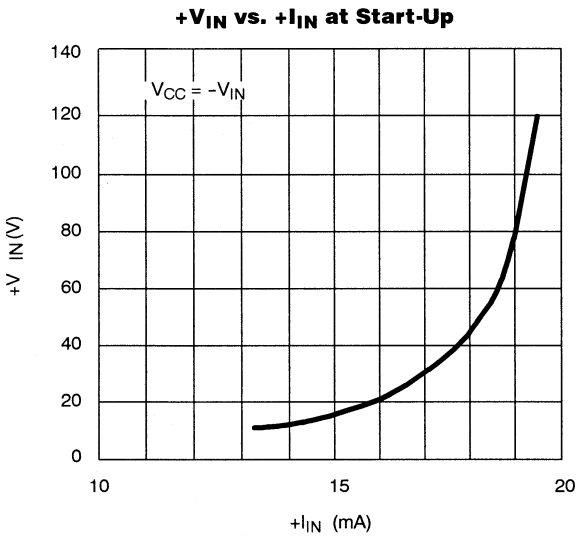


FIGURE 4.

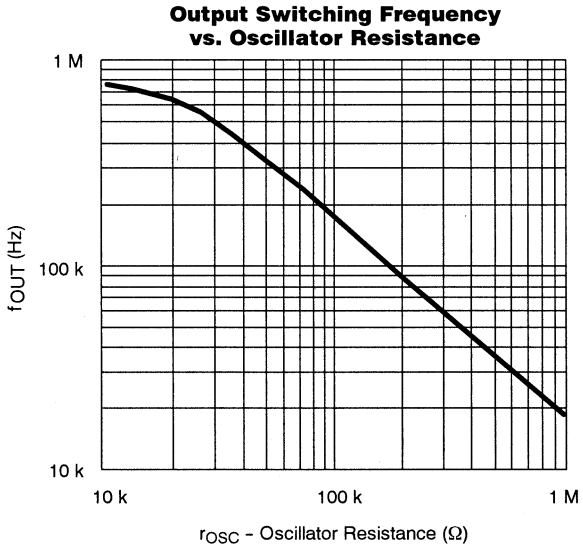
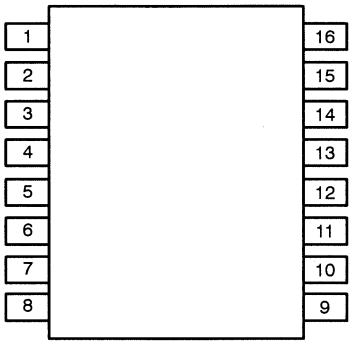


FIGURE 5.

PIN CONFIGURATIONS

SO-16
(Wide-Body)



Top View
Order Number: Si9104DW

PIN DESCRIPTION

Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
$-V_{IN}$	5	2	8
V_{CC}	6	4	9
OSC_{OUT}	7	5	10
OSC_{IN}	8	6	11
DISCHARGE	9	7	12
V_{REF}	10	8	14
$\overline{SHUTDOWN}$	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
$+V_{IN}$	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19

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