查询"DAC8832IBRGYTG4"供应商

16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converter

FEATURES

- 16-Bit Resolution
- 2.7 V to 5.5 V Single-Supply Operation
- Very Low Power: 15 μW for 3 V Power
- High Accuracy, INL: 1 LSB
- Low Glitch: 10 nV-s
- Low Noise: 18n V/√Hz
- Fast Settling: 1.0 μS
- Fast SPI™ Interface, up to 50 MHz
- Reset to Mid-Code
- Schmitt-Trigger Inputs for Direct Optocoupler Interface

APPLICATIONS

- Portable Equipment
- Automatic Test Equipment
- Industrial Process Control
- Data Acquisition Systems
- Optical Networking

DESCRIPTION

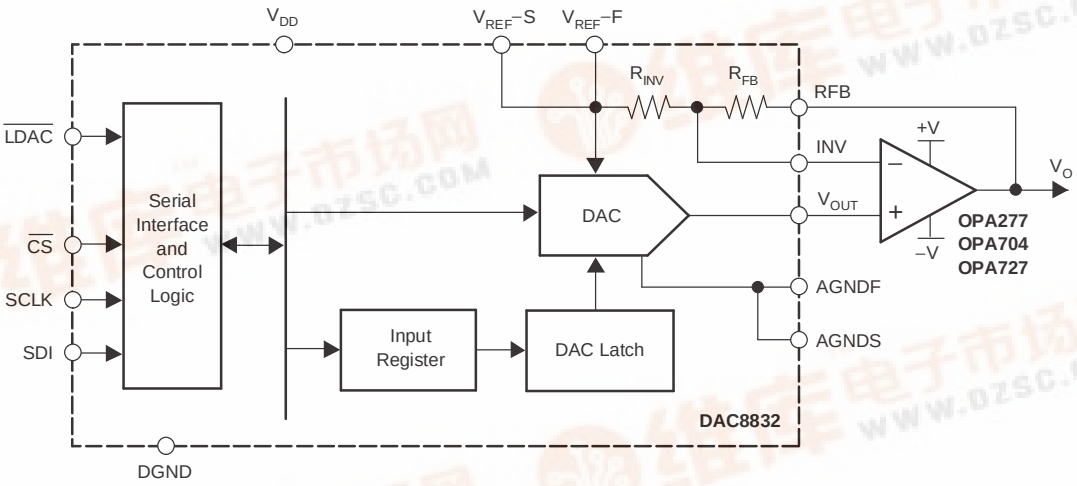
The DAC8832 is a single, 16-bit, serial-input, voltage-output digital-to-analog converter (DAC) operating from a single 3 V to 5 V power supply. The DAC8832 provides excellent linearity (1 LSB INL), low glitch, low noise, and fast settling (1.0 μS to 1/2 LSB of full-scale output) over the specified temperature range of –40°C to +85°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer.

This device features a standard high-speed (clock up to 50MHz), 3 V or 5 V SPI serial interface to communicate with the DSP or microprocessors.

The DAC8832 provides unipolar or bipolar output ($\pm V_{REF}$) when working with an external buffer, and is reset to mid-code after power-up. For optimum performance, a set of Kelvin connections to the external reference and the analog ground input are provided.

The DAC8832 is available in a QFN-14 package, and is pin-to-pin compatible with the DAC8831IRGY, which is reset to zero-code after power-up.

Functional Block Diagram



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	POWER-ON RESET VALUE	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8832IRGY	±4	±1	Mid-Code	–40°C to +85°C	8832I	QFN-14	RGY	DAC8832IRGYT	Tape and Reel, 250
								DAC8832IRGYR	Tape and Reel, 1000
DAC8832IBRGY	±2	±1	Mid-Code	–40°C to +85°C	8832I	QFN-14	RGY	DAC8832IBRGYT	Tape and Reel, 250
								DAC8832IBRGYR	Tape and Reel, 1000
DAC8832ICRGY	±1	±1	Mid-Code	–40°C to +85°C	8832I	QFN-14	RGY	DAC8832ICRGYT	Tape and Reel, 250
								DAC8832ICRGYR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	DAC8832	UNIT
V_{DD} to AGND	–0.3 to +7	V
Digital input voltage to DGND	–0.3 to +V_{DD} + 0.3	V
V_{OUT} to AGND	–0.3 to +V_{DD} + 0.3	V
AGND, AGNDF, AGNDS to DGND	–0.3 to +0.3	V
Operating temperature range	–40 to +85	°C
Storage temperature range	–65 to +150	°C
Junction temperature range (T_J max)	+150	°C
Power dissipation	(T_J max – T_A) / θ_{JA}	W
Thermal impedance, θ_{JA}	54.9	°C/W

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +3 V or V_{DD} = +5V, V_{REF} = +2.5 V unless otherwise noted; specifications subject to change without notice.

PARAMETER		CONDITIONS	DAC8832 MIN	DAC8832 TYP	DAC8832 MAX	UNIT
STATIC PERFORMANCE						
Resolution			16			bits
Linearity error	DAC8832ICRGY			±0.5	±1	LSB
	DAC8832IBRGY			±0.5	±2	
	DAC8832IRGY			±0.5	±4	
Differential linearity error		All grades		±0.5	±1	LSB
Gain error		T_A = +25°C		±1	±5	LSB
		T_A = –40°C to +85°C			±7	
Gain drift				±0.1		ppm/°C
Zero code error		T_A = +25°C		±0.25	±1	LSB
		T_A = –40°C to +85°C			±2	
Zero code drift				±0.05		ppm/°C
OUTPUT CHARACTERISTICS						
Voltage output (1)		Unipolar operation	0		$+V_{REF}$	V
		Bipolar operation	$-V_{REF}$		$+V_{REF}$	V
Output impedance				6.25		kΩ
Settling time		To 1/2 LSB of FS, C_L = 10 pF		1		µs
Slew rate (2)		C_L = 10 pF		25		V/µs
Digital-to-analog glitch		1 LSB change around major carry		10		nV-s
Digital feedthrough (3)				0.2		nV-s
Output noise		T_A = +25°C		18		nV/√Hz
Power-supply rejection		V_{DD} varies ±10%			±1	LSB
Bipolar resistor matching		R_{FB} / R_{INV}		1		Ω/Ω
		Ratio error		±0.0015	±0.0076	%
Bipolar zero error		T_A = +25°C		±0.25	±5	LSB
		T_A = –40°C to +85°C			±7	
Bipolar zero drift				±0.2		ppm/°C

(1) See the *Bipolar Output Operation* section for details.
(2) Slew Rate is measure from 10% to 90% of transition when the output changes from 0 to full-scale.
(3) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change; $\overline{CS}$ is held high, while SCLK and DIN signals are toggled.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +3 V or V_{DD} = +5V, V_{REF} = +2.5 V unless otherwise noted; specifications subject to change without notice.

PARAMETER		CONDITIONS	DAC8832			UNIT
			MIN	TYP	MAX	
REFERENCE INPUT						
	Reference input voltage range		1.25		V_{DD}	V
	Reference input impedance(4)	Unipolar mode	9			kΩ
		Bipolar mode	7.5			
	Reference –3 dB bandwidth, BW	Code = FFFFh		1.3		MHz
	Reference feedthrough	Code = 0000h, V_{REF} = 1 V_{PP} at 100 kHz		1		mV
	Signal-to-noise ratio, SNR			92		dB
	Reference input capacitance	Code = 0000h		75		pF
		Code = FFFFh		120		
DIGITAL INPUTS						
V_{IL}	Input low voltage	V_{DD} = 2.7 V			0.6	V
		V_{DD} = 5 V			0.8	
V_{IH}	Input high voltage	V_{DD} = 2.7 V	2.1			V
		V_{DD} = 5 V	2.4			
	Input current				±1	µA
	Input capacitance				10	pF
	Hysteresis voltage			0.4		V
POWER SUPPLY						
V_{DD}	Power-supply voltage		2.7		5.5	V
I_{DD}	Power-supply current	V_{DD} = 3 V		5	20	µA
		V_{DD} = 5 V		5	20	
	Power	V_{DD} = 3 V		15	60	µW
		V_{DD} = 5 V		25	100	
TEMPERATURE RANGE						
	Specified performance		–40		+85	°C

(4) Reference input resistance is code-dependent, minimum at 8555h.

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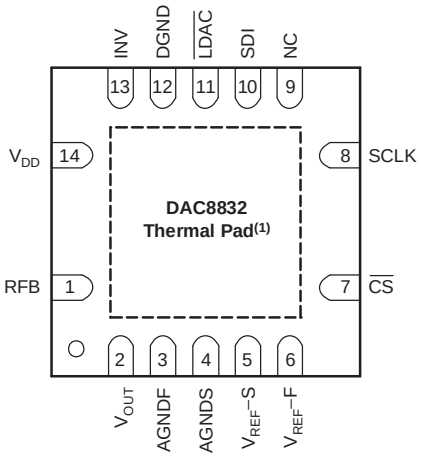
PIN CONFIGURATION (NOT TO SCALE)

RGY PACKAGE
QFN-14
(TOP VIEW)



NOTE: (1) Exposed thermal pad must be connected to analog ground.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
2	V_{OUT}	Analog output of DAC
3	AGNDF	Analog ground (Force)
4	AGNDS	Analog ground (Sense)
5	V_{REF}-S	Voltage reference input (Sense). Connect to external voltage reference
6	V_{REF}-F	Voltage reference input (Force). Connect to external voltage reference
7	$\overline{CS}$	Chip select input (active low). Data is not clocked into SDI unless $\overline{CS}$ is low.
8	SCLK	Serial clock input.
9	NC	No internal connection
10	SDI	Serial data input. Data is latched into input register on the rising edge of SCLK.
11	$\overline{LDAC}$	Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.
12	DGND	Digital ground
13	INV	Junction point of internal scaling resistors. Connect to external operational amplifier inverting input in bipolar mode.
14	V_{DD}	Analog power supply, +3 V to +5 V.

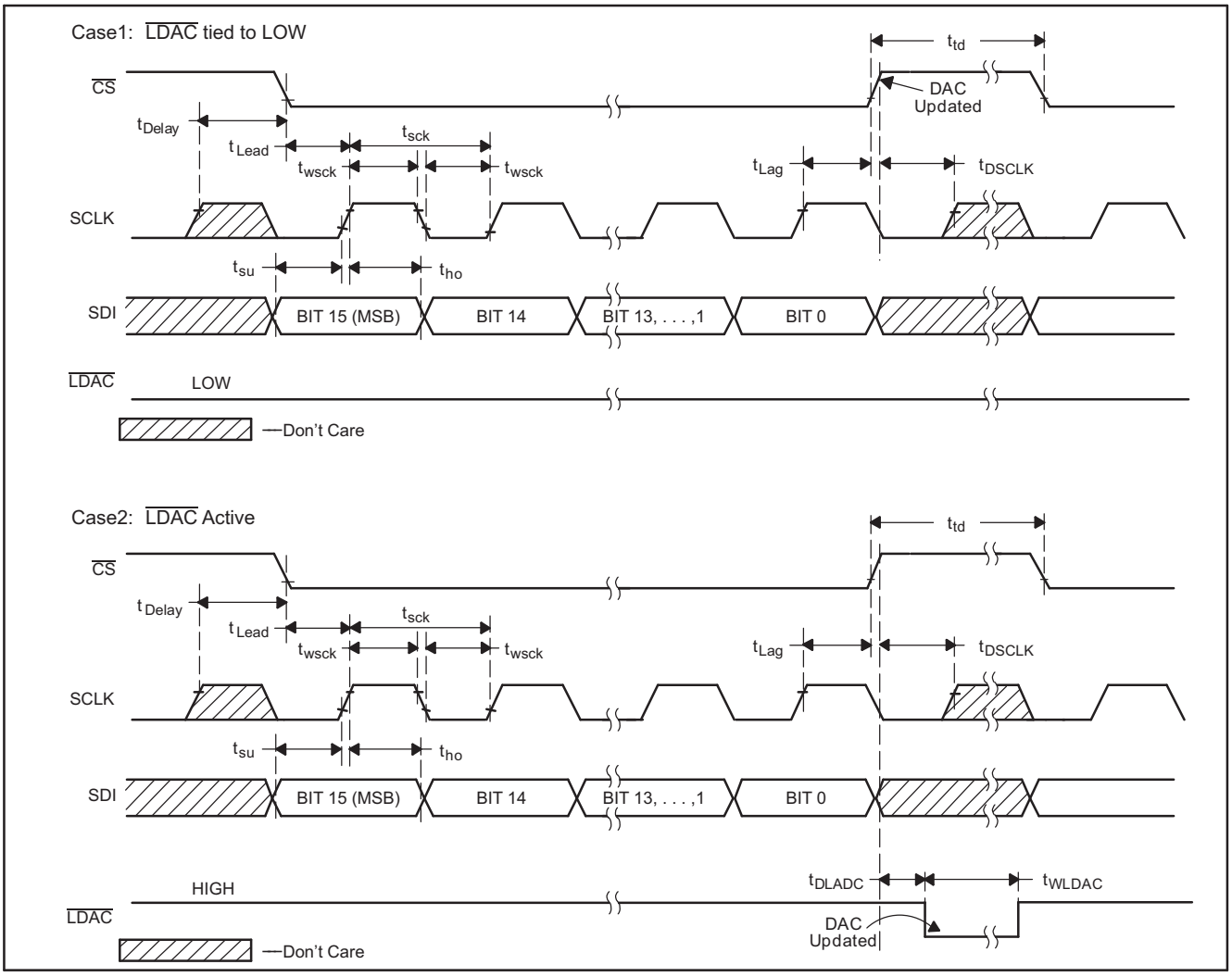


Figure 1. DAC8832 Timing Diagram

TIMING CHARACTERISTICS: V_{DD} = +5 V(1)(2)

At –40°C to +85°C, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	20		ns
t_{wsck}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{CS}$ low	10		ns
t_{Lead}	$\overline{CS}$ enable lead time	10		ns
t_{Lag}	$\overline{CS}$ enable lag time	10		ns
t_{DSCLK}	Delay from $\overline{CS}$ high to SCLK high	10		ns
t_{td}	$\overline{CS}$ high between active period	30		ns
t_{su}	Data setup time (input)	10		ns
t_{ho}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{LDAC}$ width	30		ns
t_{DLDAC}	Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	30		ns
	V_{DD} high to $\overline{CS}$ low (power-up delay)	10		µs

(1) Assured by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TIMING CHARACTERISTICS: V_{DD} = +3 V(1)(2)

At –40°C to +85°C, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	20		ns
t_{wsck}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{CS}$ low	10		ns
t_{Lead}	$\overline{CS}$ enable lead time	10		ns
t_{Lag}	$\overline{CS}$ enable lag time	10		ns
t_{DSCLK}	Delay from $\overline{CS}$ high to SCLK high	10		ns
t_{td}	$\overline{CS}$ high between active period	30		ns
t_{su}	Data setup time (input)	10		ns
t_{ho}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{LDAC}$ width	30		ns
t_{DLDAC}	Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	30		ns
	V_{DD} high to $\overline{CS}$ low (power-up delay)	10		µs

(1) Assured by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V

At T_A = +25°C, V_{REF} = +2.5 V unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

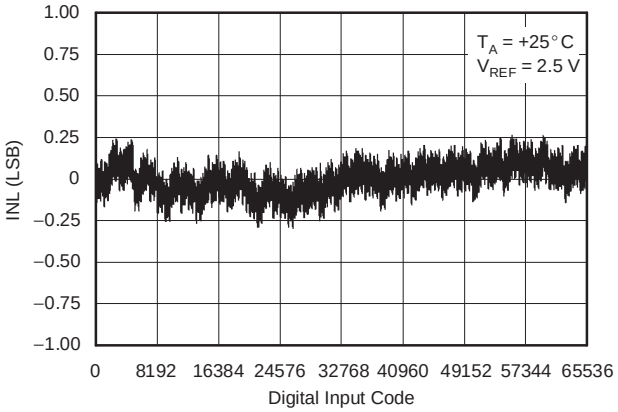


Figure 2.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

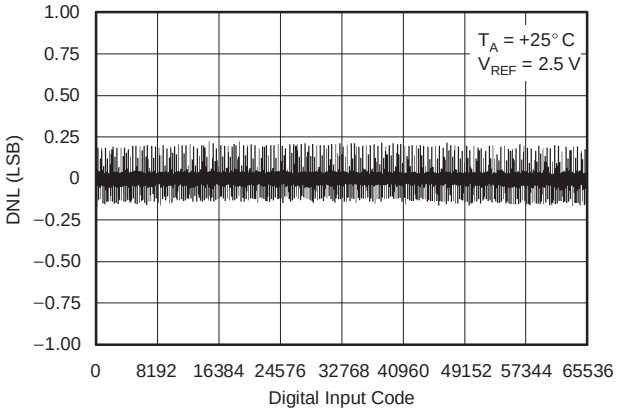


Figure 3.

LINEARITY ERROR vs DIGITAL INPUT CODE

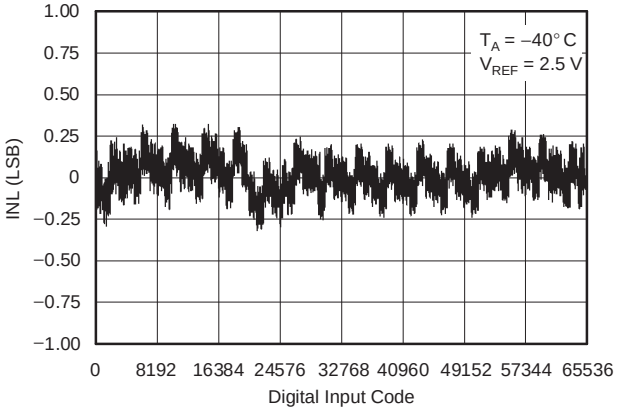


Figure 4.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

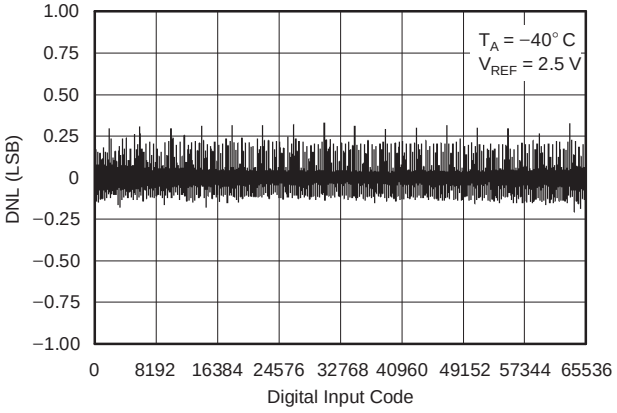


Figure 5.

LINEARITY ERROR vs DIGITAL INPUT CODE

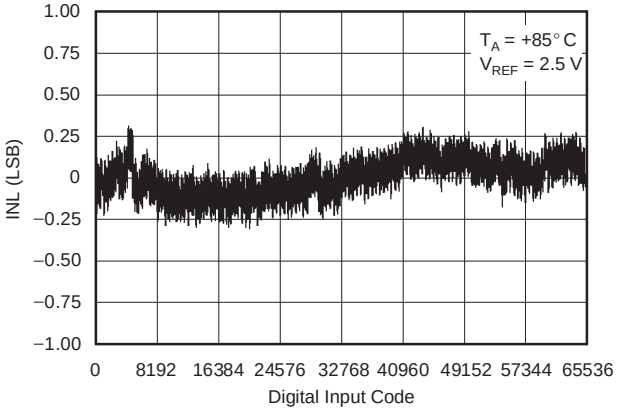


Figure 6.

DIFFERENTIAL LINEARY ERROR vs DIGITAL INPUT CODE

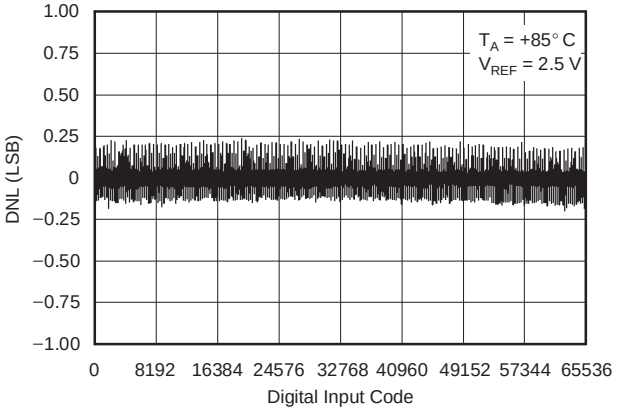


Figure 7.

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TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, V_{REF} = +2.5 V unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

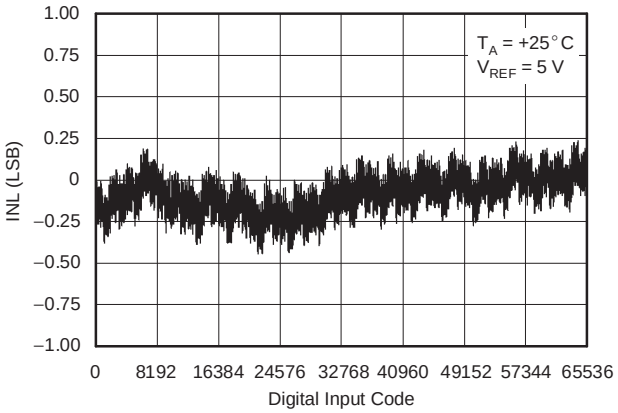

Figure 8.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

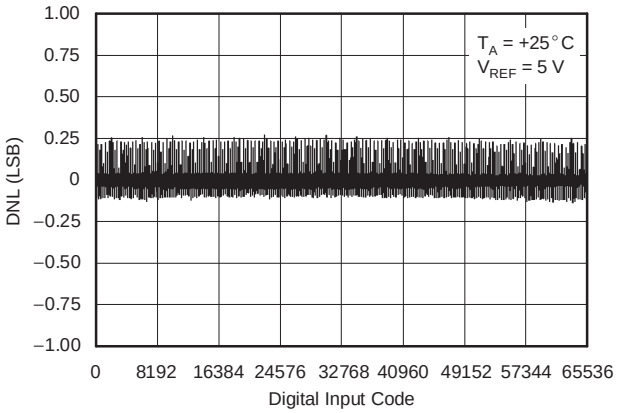

Figure 9.

LINEARITY ERROR vs REFERENCE VOLTAGE

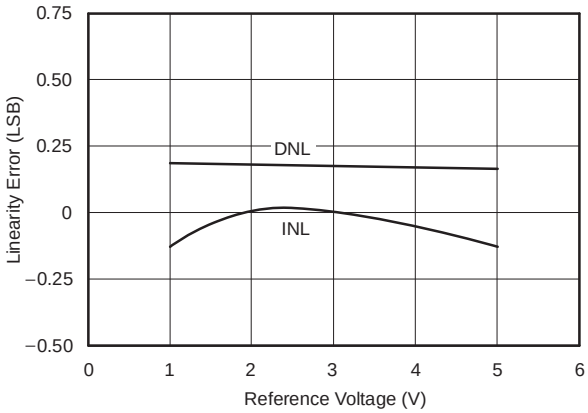

Figure 10.

LINEARITY ERROR vs SUPPLY VOLTAGE

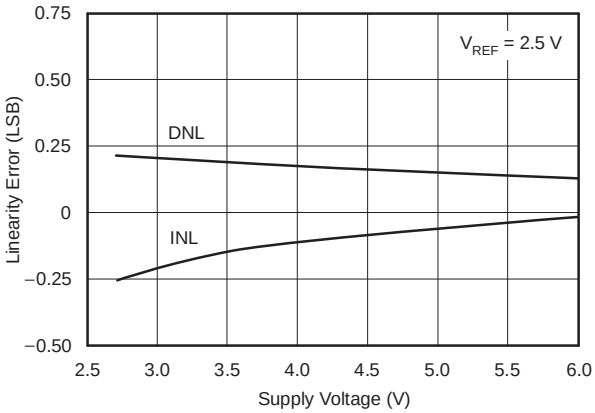

Figure 11.

GAIN ERROR vs TEMPERATURE

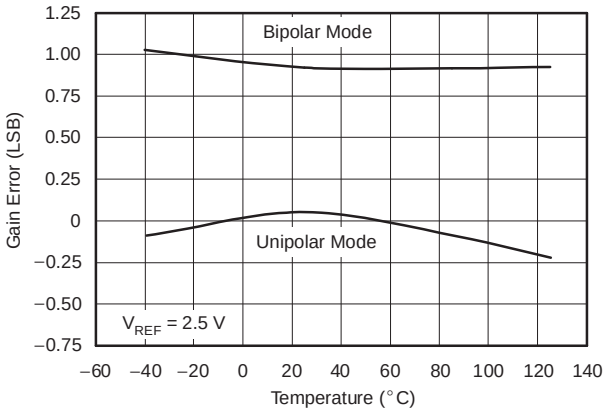

Figure 12.

ZERO-CODE ERROR vs TEMPERATURE

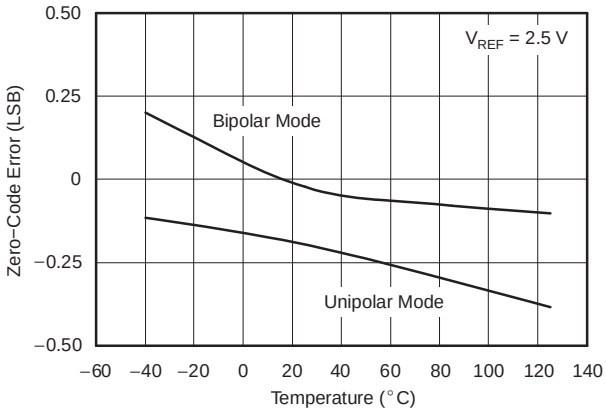

Figure 13.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, V_{REF} = +2.5 V unless otherwise noted.

REFERENCE CURRENT vs CODE (UNIPOLAR MODE)

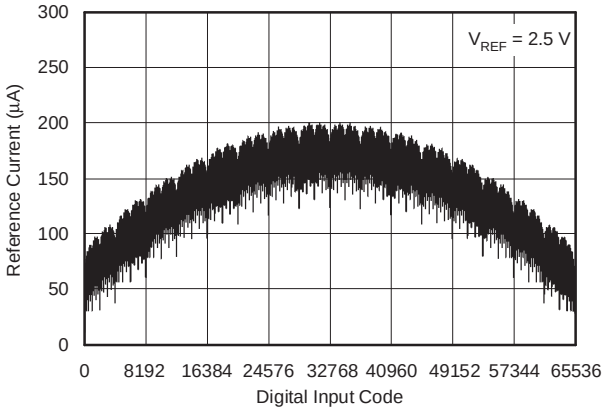

Figure 14.

REFERENCE CURRENT vs CODE (BIPOLAR MODE)

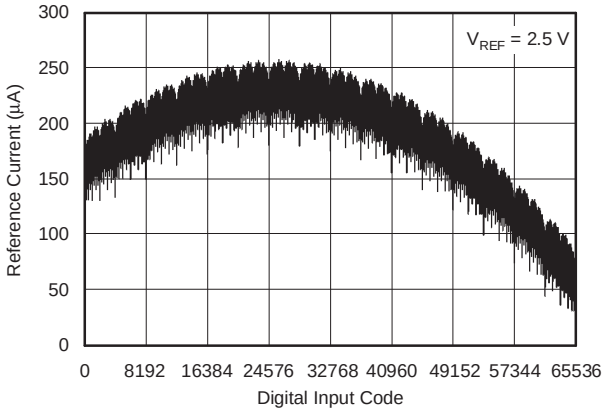

Figure 15.

SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE

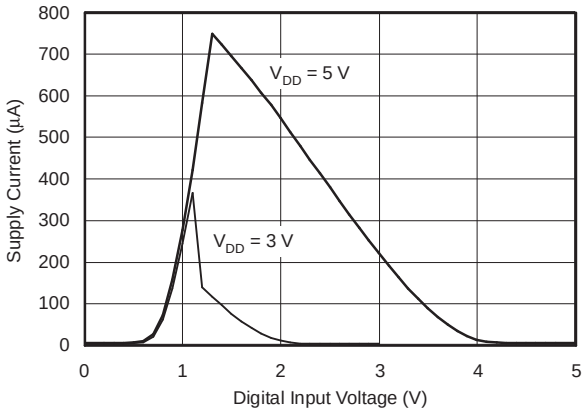

Figure 16.

SUPPLY CURRENT vs TEMPERATURE

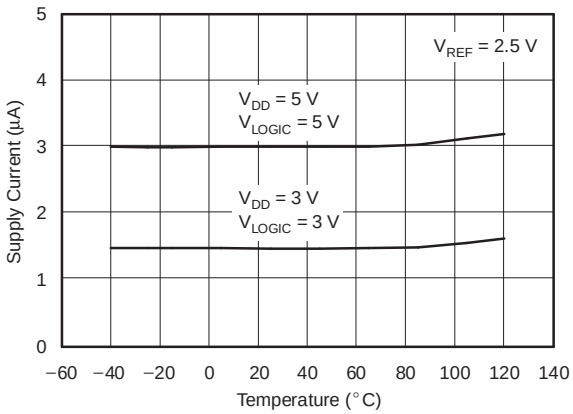

Figure 17.

SUPPLY CURRENT vs SUPPLY VOLTAGE

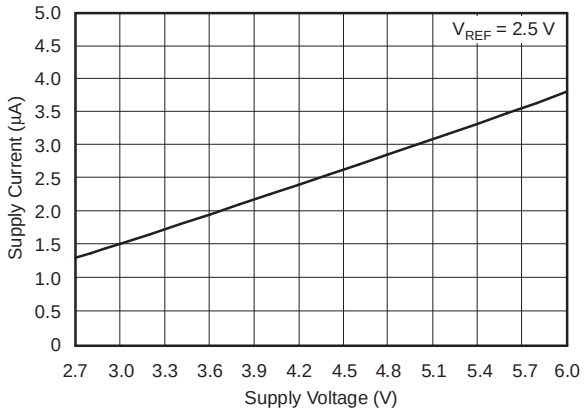

Figure 18.

SUPPLY CURRENT vs REFERENCE VOLTAGE

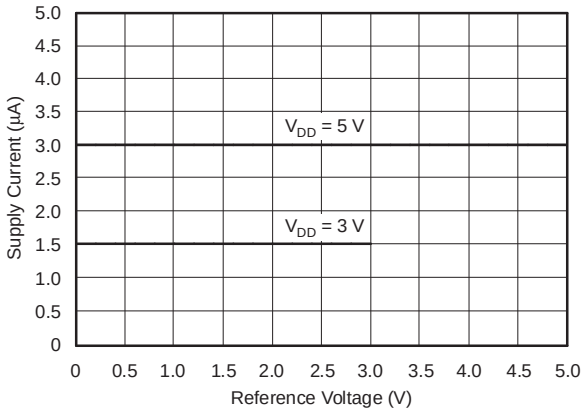

Figure 19.

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TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, V_{REF} = +2.5 V unless otherwise noted.

MAJOR-CARRY GLITCH (FALLING)

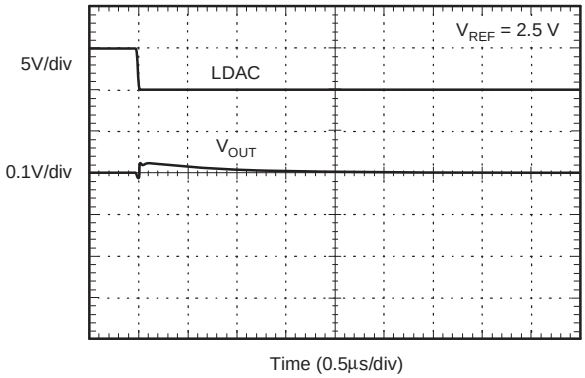

Figure 20.

MAJOR-CARRY GLITCH (RISING)

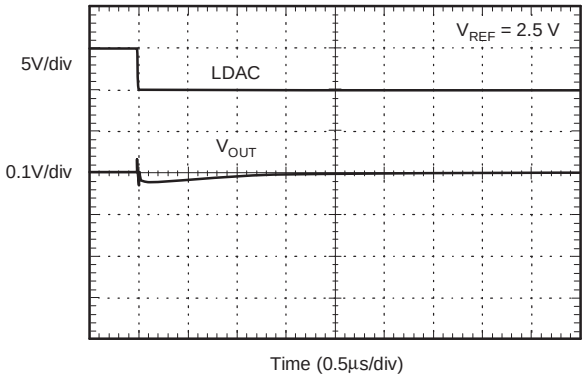

Figure 21.

DAC SETTLING TIME (FALLING)

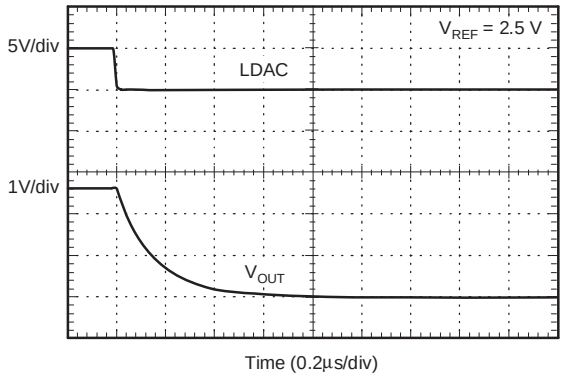

Figure 22.

DAC SETTLING TIME (RISING)

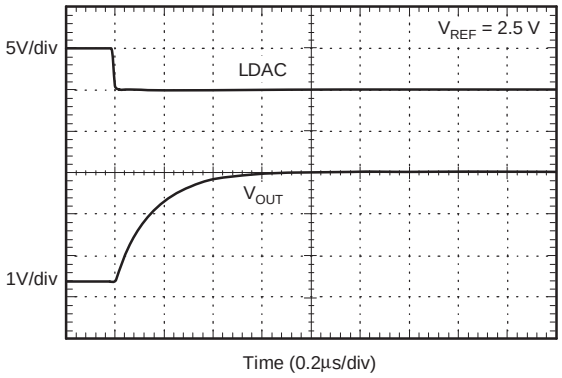

Figure 23.

DIGITAL FEEDTHROUGH

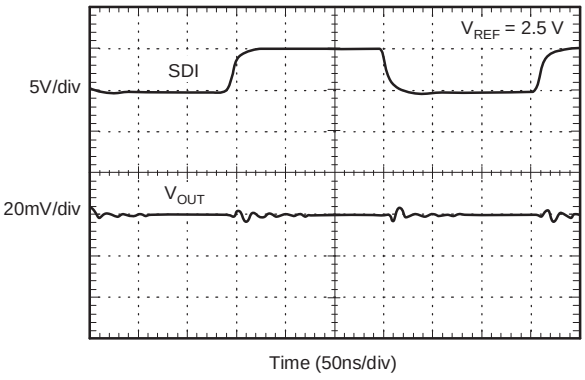

Figure 24.

TYPICAL CHARACTERISTICS: V_{DD} = +3 V

At T_A = +25°C, V_{REF} = +2.5 V unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

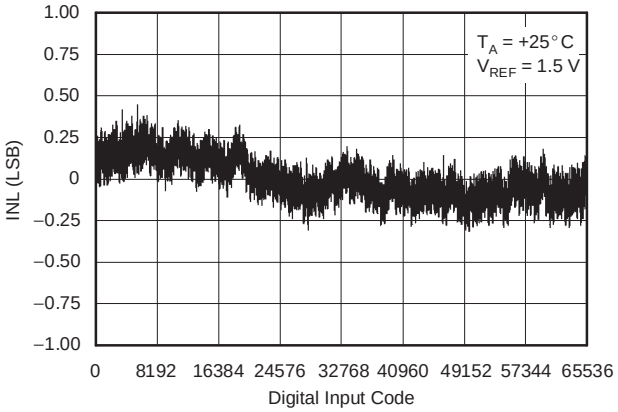

Figure 25.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

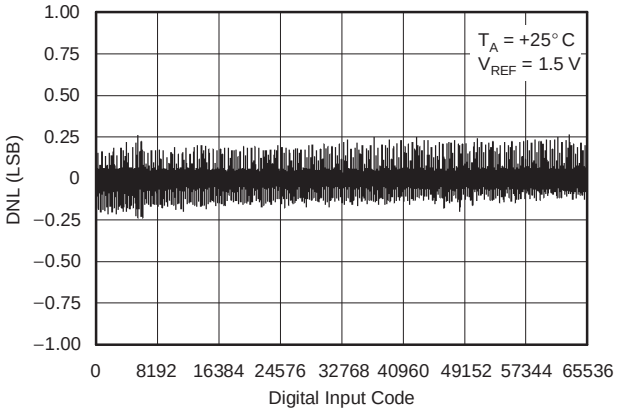

Figure 26.

LINEARITY ERROR vs DIGITAL INPUT CODE

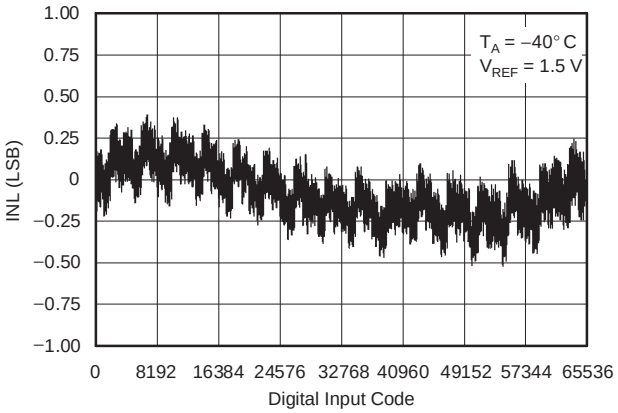

Figure 27.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

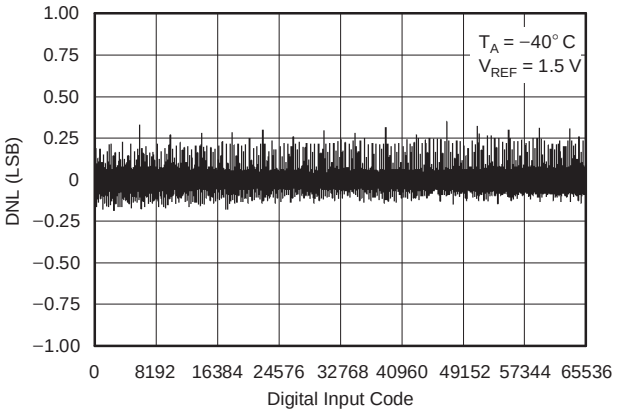

Figure 28.

LINEARITY ERROR vs DIGITAL INPUT CODE

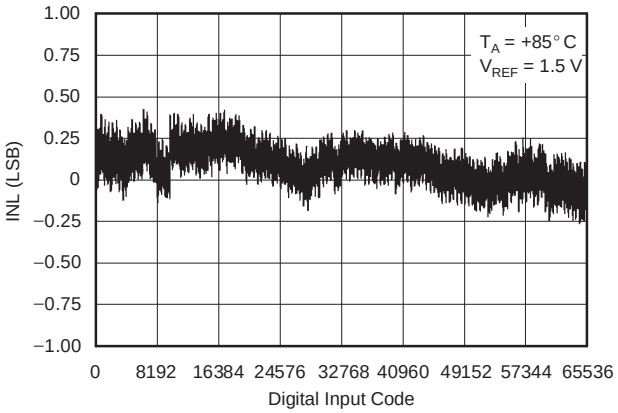

Figure 29.

DIFFERENTIAL LINEARY ERROR vs DIGITAL INPUT CODE

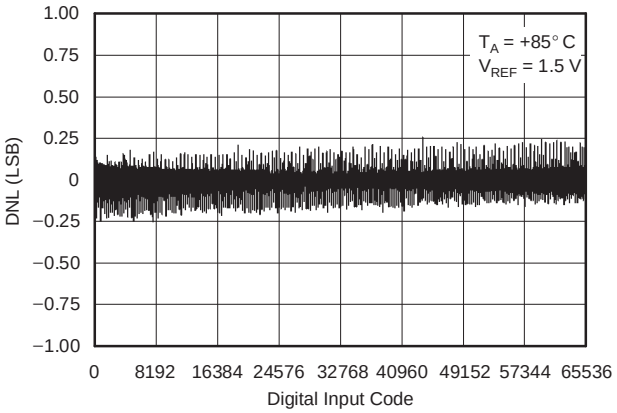

Figure 30.

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TYPICAL CHARACTERISTICS: V_{DD} = +3 V (continued)

At T_A = +25°C, V_{REF} = +2.5 V unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

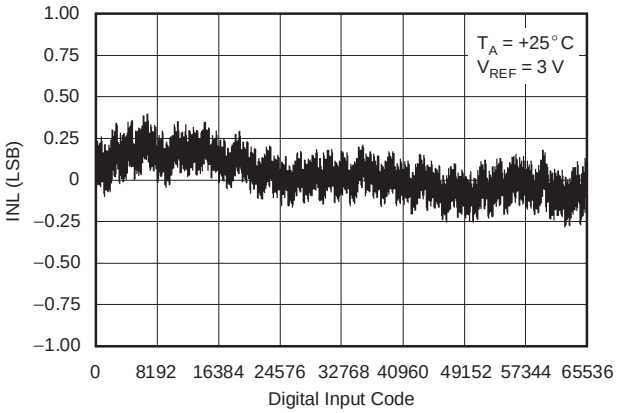

Figure 31.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

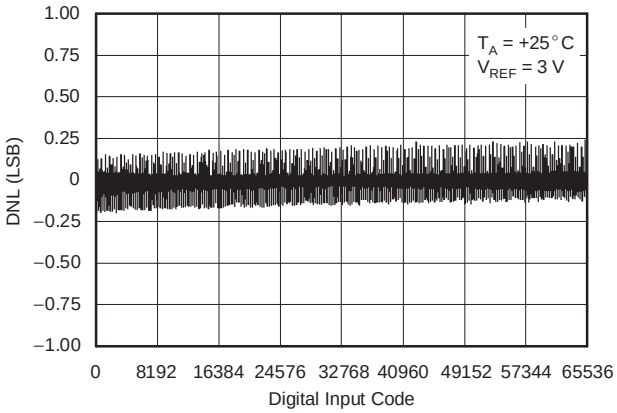

Figure 32.

LINEARITY ERROR vs REFERENCE VOLTAGE

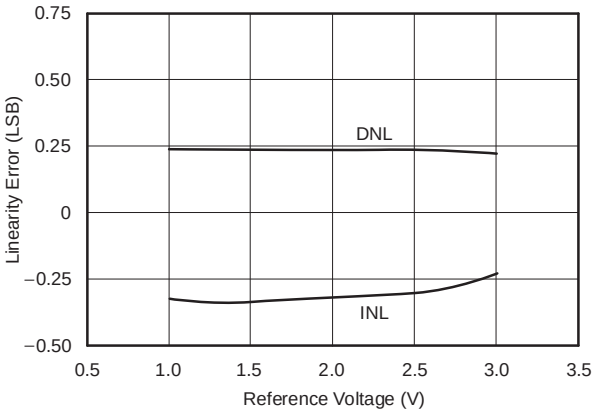

Figure 33.

GAIN ERROR vs TEMPERATURE

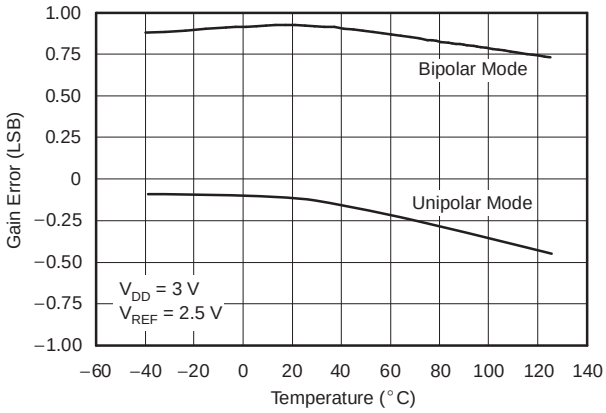

Figure 34.

ZERO-CODE ERROR vs TEMPERATURE

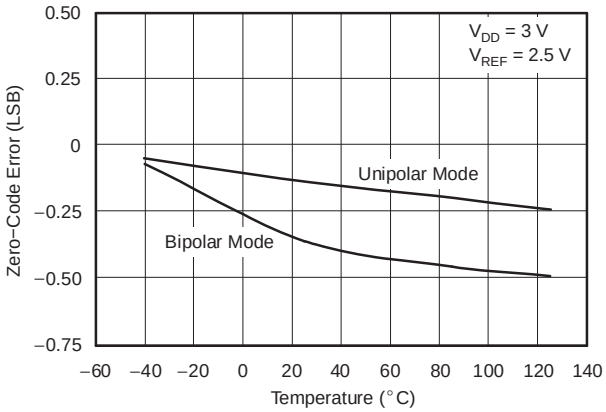

Figure 35.

REFERENCE CURRENT vs CODE (UNIPOLAR MODE)

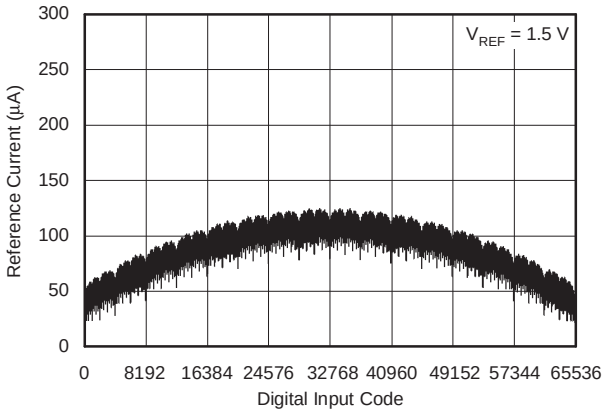

Figure 36.

TYPICAL CHARACTERISTICS: V_{DD} = +3 V (continued)

At T_A = +25°C, V_{REF} = +2.5 V unless otherwise noted.

REFERENCE CURRENT vs CODE (BIPOLAR MODE)

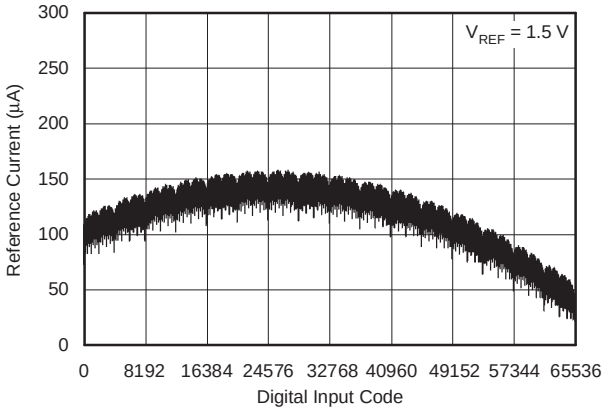

Figure 37.

DIGITAL FEEDTHROUGH

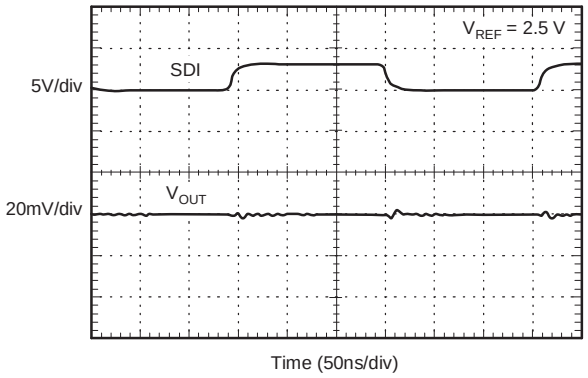

Figure 38.

MAJOR-CARRY GLITCH (FALLING)

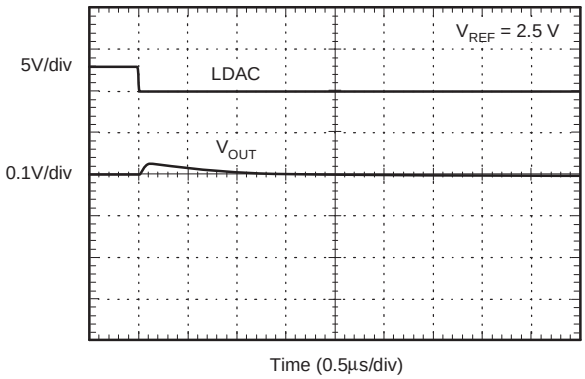

Figure 39.

MAJOR-CARRY GLITCH (RISING)

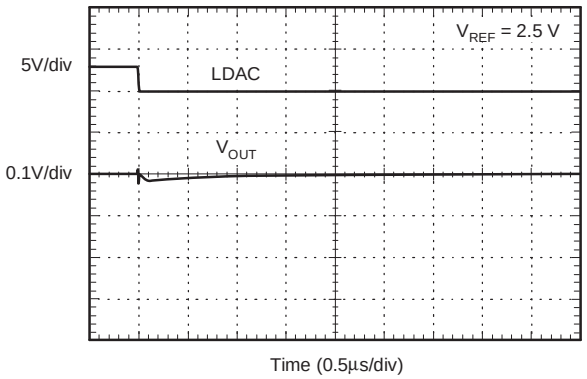

Figure 40.

DAC SETTLING TIME (FALLING)

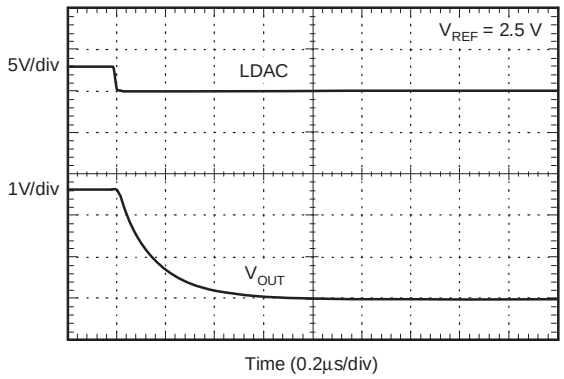

Figure 41.

DAC SETTLING TIME (RISING)

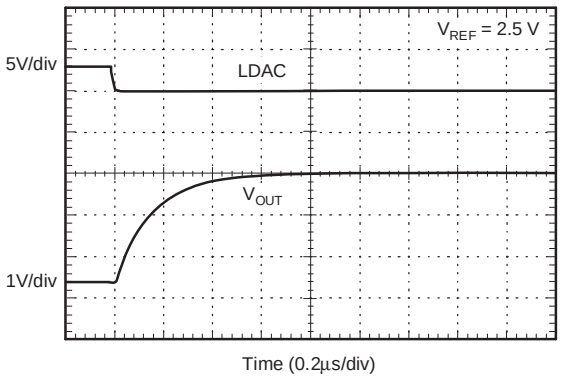

Figure 42.

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8832 is a single, 16-bit, serial-input, voltage-output DAC. It operates from a single supply ranging from 2.7 V to 5 V, and typically consumes 5 μA. Data are written to this device in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, the DAC8832 is designed with a power-on reset function. The DAC8832 is reset to mid-scale code. In unipolar mode, the DAC8832 is reset to 1/2 × V_{REF}, and in bipolar mode, is reset to 0 V. Kelvin sense connections for the reference and analog ground are also included.

DIGITAL-TO-ANALOG SECTIONS

The DAC architecture consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 43. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

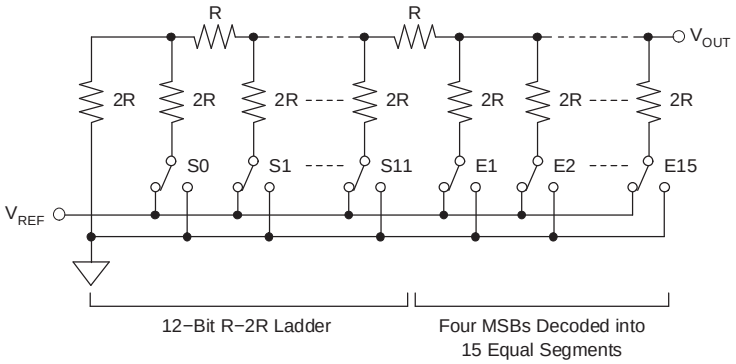

Figure 43. DAC Architecture

OUTPUT RANGE

The output of the DAC is:

$V_{OUT} = (V_{REF} \times Code)/65536$

Where *Code* is the decimal data word loaded to the DAC latch.

THEORY OF OPERATION (continued)

POWER-ON RESET

The DAC8832 has a power-on reset function to ensure the output is at a known state upon power-up. Upon power-up, the DAC latch and input register contain mid-scale code until new data is loaded from the input serial shift register. Therefore, after power-up, the output from pin V_{OUT} is $0.5 \times V_{REF}$ in unipolar mode, and 0V in bipolar mode.

However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the device, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept; if less than 16 are loaded, bits will remain from the previous word. If the device must be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

SERIAL INTERFACE

The digital interface is standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

The DAC8832 has an $\overline{LDAC}$ pin allowing the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. In this case, $\overline{LDAC}$ must be maintained high while $\overline{CS}$ is low. If $\overline{LDAC}$ is tied permanently low, the DAC latch is updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{CS}$).

APPLICATION INFORMATION

UNIPOLAR OUTPUT OPERATION

The DAC8832 is capable of driving unbuffered loads of 60kΩ. Unbuffered operation results in low supply current (typically 5µA) and a low offset error. The DAC8832 can be configured to output both unipolar and bipolar voltages. Figure 44 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 1.

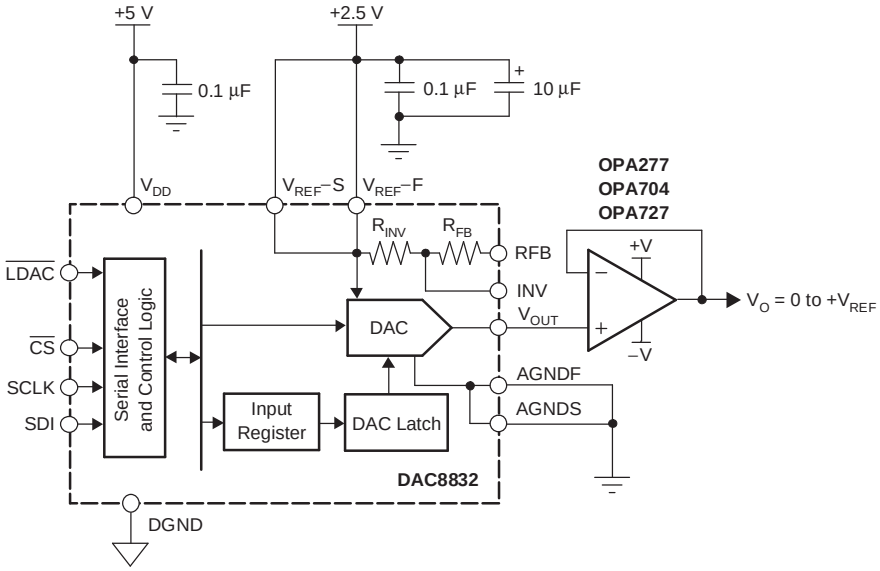

Figure 44. Unipolar Output Mode

Table 1. Unipolar Code

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111 1111	V_{REF} × (65,535/65,536)
1000 0000 0000 0000	V_{REF} × (32,768/65,536) = 1/2 V_{REF}
0000 0000 0000 0001	V_{REF} × (1/65,536)
0000 0000 0000 0000	0V

Assuming a perfect reference, the worst-case output voltage may be calculated in the following equation:

Unipolar Mode Worst-Case Output:

$$V_{OUT\_UNI} = \frac{D}{2^{16}} \times \left(V_{REF} + V_{GE}\right) + V_{ZSE} + INL$$

Where:

V_{OUT_UNI} = Unipolar mode worst-case output
D = Code loaded to DAC
V_{REF} = Reference voltage applied to part
V_{GE} = Gain error in volts
V_{ZSE} = Zero scale error in volts
INL = Integral nonlinearity in volts

BIPOLAR OUTPUT OPERATION

With the aid of an external operational amplifier, the DAC8832 may be configured to provide a bipolar voltage output. A typical circuit of such an operation is shown in Figure 45. The matched bipolar offset resistors R_{FB} and R_{INV} are connected to an external operational amplifier to achieve this bipolar output swing; typically, $R_{FB} = R_{INV} = 28\ k\Omega$.

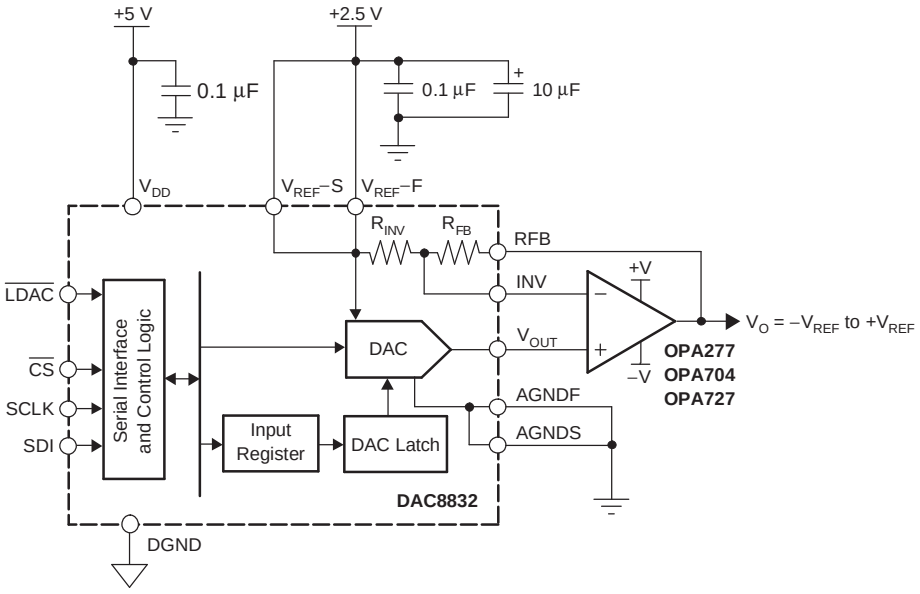

Figure 45. Bipolar Output Mode

Table 2 shows the transfer function for this output operating mode. The DAC8832 also provides a set of Kelvin connections to the analog ground and external reference inputs.

Table 2. Bipolar Code

DAC LATCH CONTENTS	
MSB LSB	ANALOG OUTPUT
1111 1111 1111 1111	$+V_{REF} \times (32{,}767/32{,}768)$
1000 0000 0000 0001	$+V_{REF} \times (1/32{,}768)$
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF} \times (1/32{,}768)$
0000 0000 0000 0000	$-V_{REF} \times (32{,}768/32{,}768) = -V_{REF}$

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation:

Bipolar Mode Worst-Case Output:

$$V_{OUT\_BIP} = \frac{\left[\left(V_{OUT\_UNI} + V_{OS}\right)(2 + RD) - V_{REF}(1 + RD)\right]}{1 + \left(\frac{2 + RD}{A}\right)}$$

Where:

V_{OS} = External operational amplifier input offset voltage
RD = R_{FB} and R_{IN} resistor matching error
A = Operational amplifier open-loop gain

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OUTPUT AMPLIFIER SELECTION

For bipolar mode, a precision amplifier should be used, supplied from a dual power supply. This provides the $\pm V_{REF}$ output.

In a single-supply application, selection of a suitable operational amplifier may be more difficult because the output swing of the amplifier does not usually include the negative rail; in this case, AGND. This output swing can result in some degradation of the specified performance unless the application does not use codes near 0.

The selected operational amplifier needs to have low-offset voltage (the DAC LSB is 38 μV with a 2.5 V reference), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25 kΩ) adds to the zero-code error.

Rail-to-rail input and output performance is required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but in order to minimize gain errors the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

REFERENCE AND GROUND

Since the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The DAC8832 operates with a voltage reference ranging from 1.25 V to V_{DD}. References below 1.25 V result in reduced accuracy.

The DAC full-scale output voltage is determined by the reference. Table 1 and Table 2 outline the analog output voltage for particular digital codes.

For optimum performance, Kelvin sense connections are provided. If the application does not require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die.

POWER SUPPLY AND REFERENCE BYPASSING

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original Revision (February 2006) to A Revision	Page
• Deleted Lead Temperature information from Absolute Maximum Ratings	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8832IBRGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832IBRGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832IBRGYT	ACTIVE	QFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832IBRGYTG4	ACTIVE	QFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832ICRGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832ICRGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832ICRGYT	ACTIVE	QFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832ICRGYTG4	ACTIVE	QFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832IRGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832IRGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832IRGYT	ACTIVE	QFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8832IRGYTG4	ACTIVE	QFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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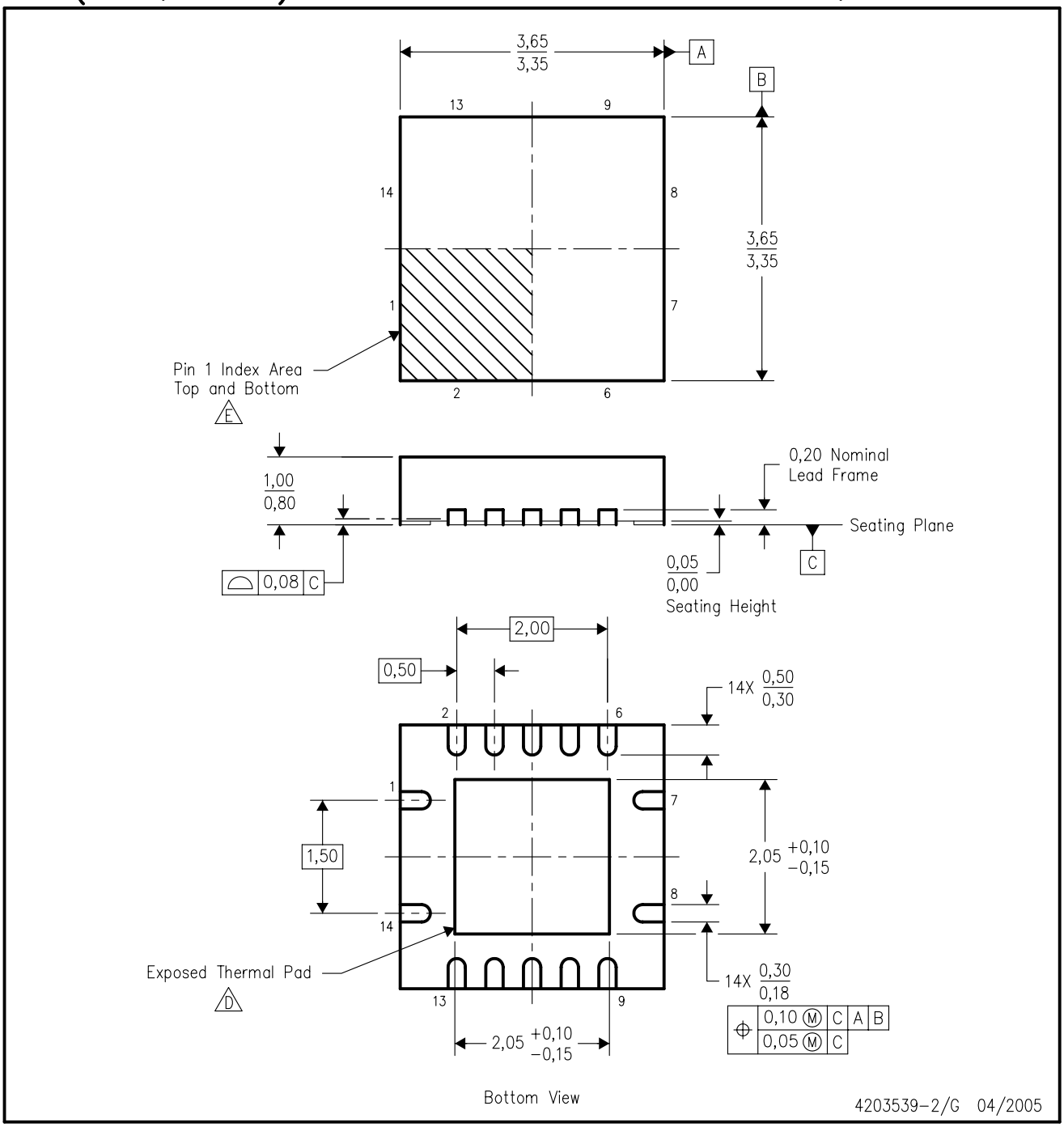
RGY (S–PQFP–N14) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BA.

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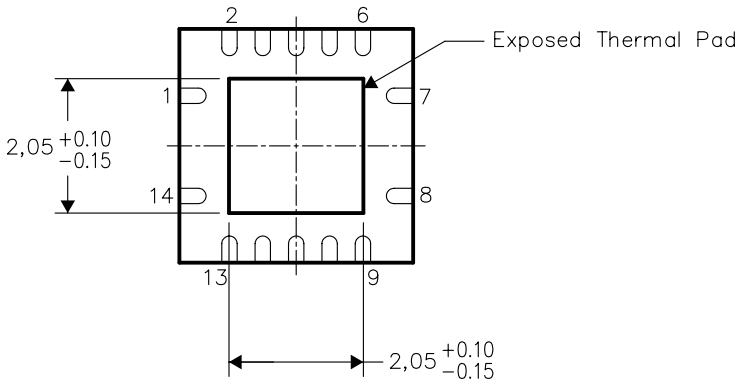
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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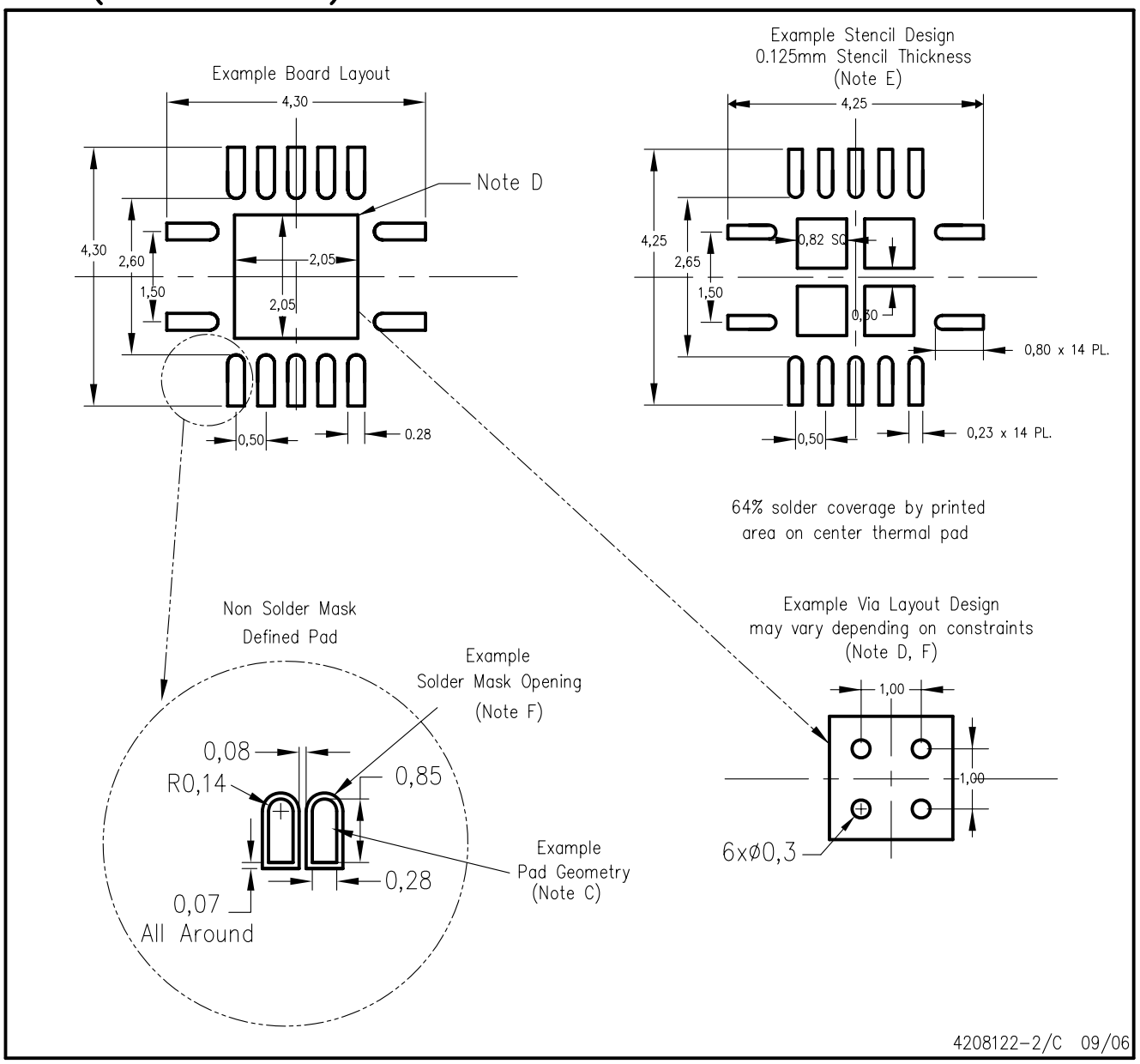
RGY (R–PQFP–N14)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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