REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change operating temperature range. Change table I limits for I_{X1L}, I_{X2H}, 7A, 14, 23, and 40A. Add footnote 8 to table I. Editorial changes throughout.	1988 DEC 20	M. A. Frye

REV																								
SHEET																								
REV																								
SHEET	22	23	24	25																				
REV STATUS OF SHEETS	REV	A	A		A	A	A	A	A	A												A		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Peltz

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APPROVED BY: M. A. Frye

DRAWING APPROVAL DATE: 4 MAY 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, NMOS DUAL UNIVERSAL SERIAL COMMUNICATIONS CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-86810

SHEET 1 OF 25

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86810	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68562	Dual universal serial communications controller (DUSCC)

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-14 (48-lead, 2.435" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

Storage temperature	-65°C to +150°C
All voltages with respect to ground	-0.5 V dc to 7.0 V dc
Maximum power dissipation (P_D)	1.8 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature	+175°C
Thermal resistance, junction-to-case (O_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH}):	
All except X1/CLK	2.0 V
X1/CLK	2.4 V
Low level input voltage (V_{IL}):	
All except X1/CLK	0.8 V
X1/CLK	0.4 V
Low level output current (I_{OL}):	
All except DONEN and IRQN	5.3 mA
DONEN and IRQN	8.8 mA
High level output current (I_{OH})	-400 µA
Case operating temperature range (T_C)	-55°C to +110°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1 .

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Power supply current	I_{CC}	V_{CC} = 5.5 V	1,2,3		325	mA
Output low voltage, except DONEN and IRQN	V_{OL}	V_{CC} = 4.5 V I_{OL} = 5.3 mA	1,2,3		0.5	V
Output voltage low DONEN and IRQN	V_{OL}	V_{CC} = 4.5 V I_{OL} = 8.8 mA	1,2,3		0.5	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -400 µA	1,2,3	2.4		V
Open collector output leakage current	I_{OC}	V_{CC} = 5.5 V V_O = 0 V to V_{CC}	1,2,3		10	µA
Input low voltage, all except X1/CLK	V_{IL1}		1,2,3		0.8	V
Input low voltage, X1/CLK	V_{IL2}		1,2,3		0.4	V
Input high voltage, all except X1/CLK	V_{IH1}		1,2,3	2.0		V
Input high voltage, X1/CLK	V_{IH2}		1,2,3	2.4		V
Three-state leakage current	I_{OZ}	V_O = 0 V to V_{CC} V_{CC} = 5.5 V	1,2,3	-10	10	µA
X1/CLK low input current	I_{X1L}	V_{CC} = 5.5 V 3/ V_{IN} = 0 V, X2/IDCN floated V_{IN} = 0 V, X2/IDCN grounded	1,2,3	-5.0 -2.0		mA mA
X1/CLK high input current	I_{X1H}	V_{CC} = 5.5 V 3/ V_{IN} = V_{CC}, X2/IDCN floated V_{IN} = V_{CC}, X2/IDCN grounded	1,2,3		36.0 1.0	mA mA
X2/IDCN low input current	I_{X2L}	V_{CC} = 5.5 V 3/ V_{IN} = 0 V, X1/CLK floated	1,2,3	-100		µA
X2/IDCN high input current	I_{X2H}	V_{CC} = 5.5 V 3/ V_{IN} = V_{CC}, X1/CLK floated	1,2,3		100	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V	1,2,3		10	µA
Input low current. all except DTCN, RTxDAKA/B, TxDAKA/B	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0 V	1,2,3	-100		µA
Input low current, remaining input pins	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0 V	1,2,3	-10		µA
Functional tests		see 4.3.1d	7,8			
RESETN pulse width	1	see figure 3	9,10,11	1.2		µs
A1-A6 setup time to CSN low	2	see figures 4 and 6	9,10,11	10		ns
A1-A6 hold time from CSN high	3		9,10,11	0		ns
R/WN setup time to CSN low	4		9,10,11	0		ns
R/WN hold time to CSN high	5		9,10,11	0		ns
CSN high pulse width 4/	6		9,10,11	160		ns
CSN or IACKN high from DTACKN low	7	see figures 4, 6, and 7	9,10,11	30		ns
IACKN high to DTACKN high	7A	see figure 7	9,10,11		200	ns
Data valid from CSN or IACKN low	8	see figures 4 and 7	9,10,11		300	ns

See footnotes at end of table

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Data bus floating from CSN high 5/	9	see figure 4	9,10,11		100	ns
Data hold time from DTACKN low 6/	10	see figure 6	9,10,11	0		ns
DTACKN low from read data ready	11	see figures 4 and 7	9,10,11	0		ns
DTACKN low from CSN low	12	see figures 4 and 6	9,10,11		560	ns
CSN low to write data valid	12A	see figure 6	9,10,11		50	ns
DTACKN high from CSN high	13	see figures 4 and 6	9,10,11		150	ns
DTACKN high impedance from CSN high	14		9,10,11		185	ns
DTACKN low from IACKN low	15	see figure 7	9,10,11		550	ns
GPI input setup time CSN low	16	see figure 8	9,10,11	20		ns
GPI input hold time from CSN low	17		9,10,11	100		ns
GPO output valid from DTACKN low	18		9,10,11		300	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
IRQN high from:						
Read RxFIFO (RxRDY interrupt)	19	see figure 9	9,10,11		450	ns
Write TxFIFO (TxRDY interrupt) 7/					450	ns
Write receive status register (Rx condition interrupt) 7/					400	ns
Write transmit/receive status register (Rx/Tx interrupt) 7/					400	ns
Write input counter/timer status register (port change and CT int.) 7/					400	ns
X1/CLK high or low time	20	see figure 10	9,10,11	25		ns
X1/CLK frequency				2.0	16	MHz
CTCLK high or low time				100		ns
CTCLK frequency				0	4	MHz
RxC high or low time				110		ns
RxC frequency (16x or 1x) 8/				0	4	MHz
TxC high or low time				110		ns
TxC frequency (16x or 1x)				0	4	MHz
TxD output from TxC input low (1x) (16x)	21	see figure 11	9,10,11		240 435	ns
TxD output from TxC output low	22		9,10,11		50	ns
RxD data setup time to RxC high	23	see figure 12	9,10,11	50		ns
RxD data hold time from RxC high	24		9,10,11	50		ns
IACKN low to IDCN low	25	see figure 13	9,10,11		200	ns
Data valid from received DMA acknowledge (RTxDAKN)	26	see figure 15	9,10,11		300	ns
DTCN width	27	see figures 14 and 15	9,10,11	100		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
DTACKN low to DTCN low	28	see figures 14 and 15	9,10,11	80		ns
Data bus float from DTCN low 5/	29	see figure 15	9,10,11		200	ns
DMA acknowledge (TxDAKN or RTxDAKN) low to DTACKN low	30	see figures 14 and 15	9,10,11		360	ns
DTACKN high from DTCN low	31		9,10,11		230	ns
DTACKN high impedance from DTCN low	32		9,10,11		250	ns
Receive DMA request (RTxDRQN) high from DMA acknowledge (RTxDAKN)	33	see figure 15	9,10,11		325	ns
Receive DMA acknowledge (RTxDAKN) width	34		9,10,11	150		ns
Receive DMA acknowledge (RTxDAKN) low to DONEN low	35		9,10,11		250	ns
Data setup to DTCN low	36	see figure 14	9,10,11	50		ns
Data hold from DTCN low 9/	37		9,10,11	50		ns
Transmit DMA request (TxDRQN) high from acknowledge (TxDAKN)	38		9,10,11		340	ns
Transmit DMA acknowledge (TxDAKN) width	39		9,10,11	150		ns
Transmit DMA acknowledge (TxDAKN) low to DONEN low output	40		9,10,11		250	ns
DTCN low DONEN output high	40A		9,10,11		260	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
CSN low to transmit DONEN low output	41	see figure 16	9,10,11		300	ns
CSN low to transmit DMA request negated (TxDRQN)	42		9,10,11		400	ns
CSN low to receive DONEN low	43		9,10,11		300	ns
CSN low to receive DMA request negated (RTxDRQN)	44		9,10,11		400	ns

1/ All voltage measurements are referenced to ground (GND). For d.c. and functional testing, all inputs except X1/CLK swing between 0.4 V and 2.4 V with a transition time of 20 ns maximum. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input voltages of 0.2 V and 2.4 V for all inputs.

2/ Test condition for outputs: C_L = 150 pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50 pF, R_L = 2.7 k ohm to V_{CC}.

3/ X1/CLK and X2/IDCN are not tested with a crystal installed.

4/ This specification will impose maximum 68000 CPU CLK to 6 MHz. Higher CPU CLK can be used if repeating bus cycles are not performed.

5/ These values were not explicitly tested, they are guaranteed by design and characterization data.

6/ Execution of the valid command (after it is latched) requires three falling edges of X1 (see figure 14).

7/ These timings are from the falling edge of DTACKN (not CSN rising).

8/ X1/CLK frequency must be at least 4 times the receiver serial data rate.

9/ In single address DMA mode write operation, data is latched by the falling edge of DTCN.

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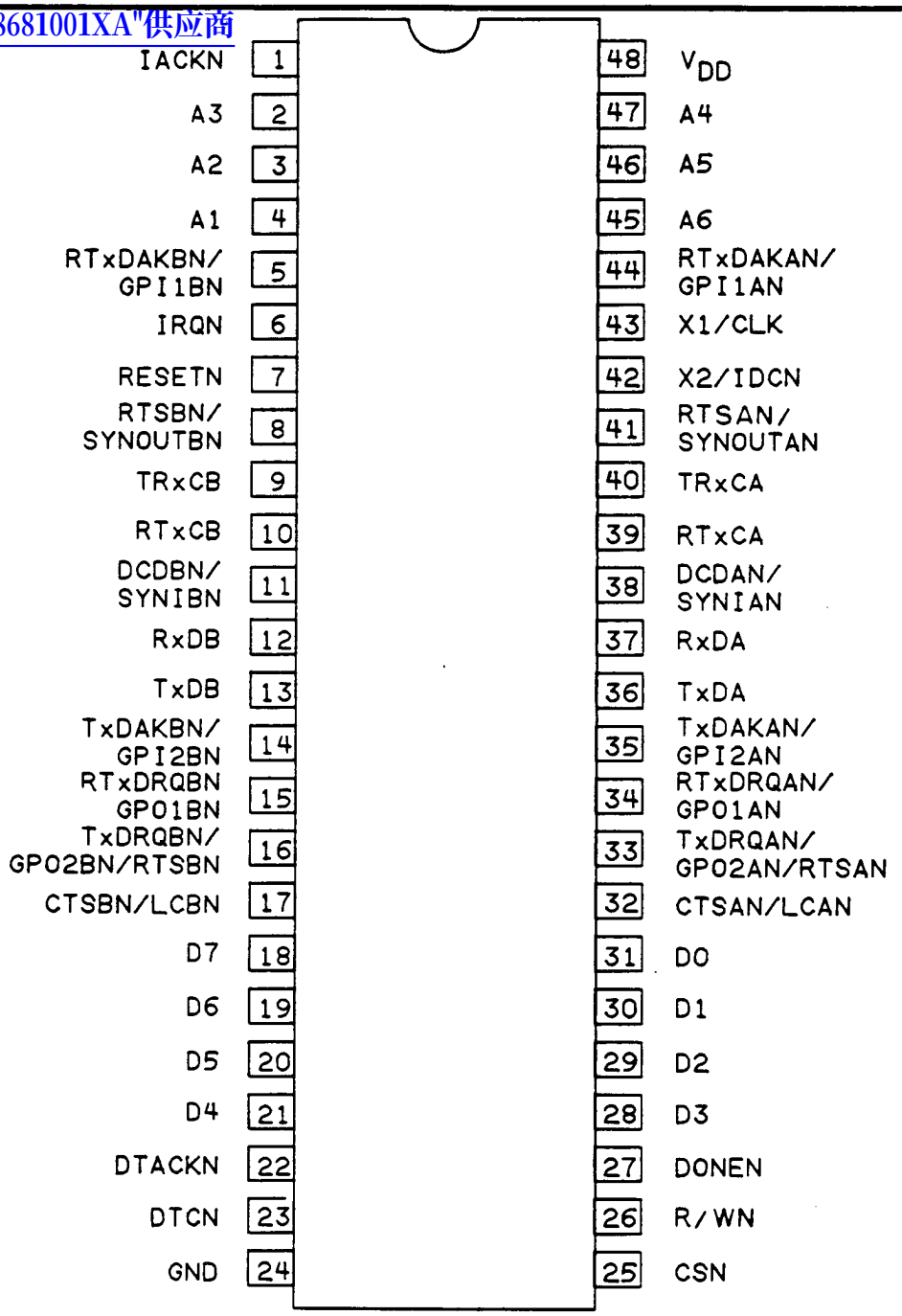

TOP VIEW

FIGURE 1. Terminal connections.

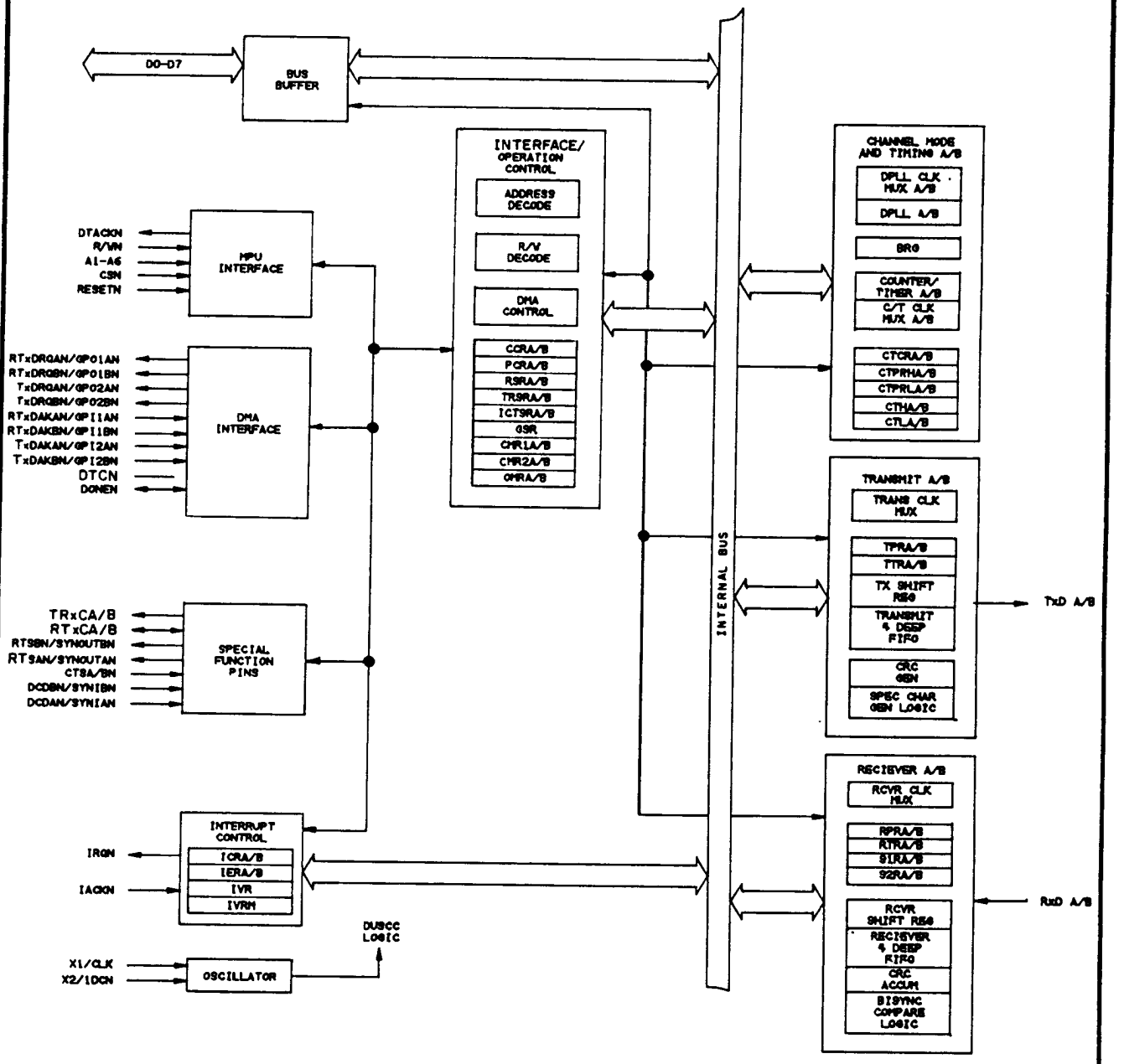

FIGURE 2. Logic diagram.

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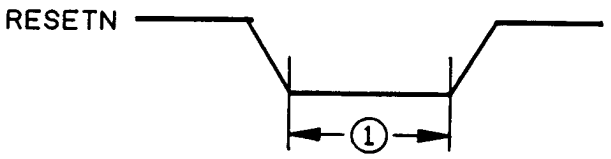

FIGURE 3. Reset timing.

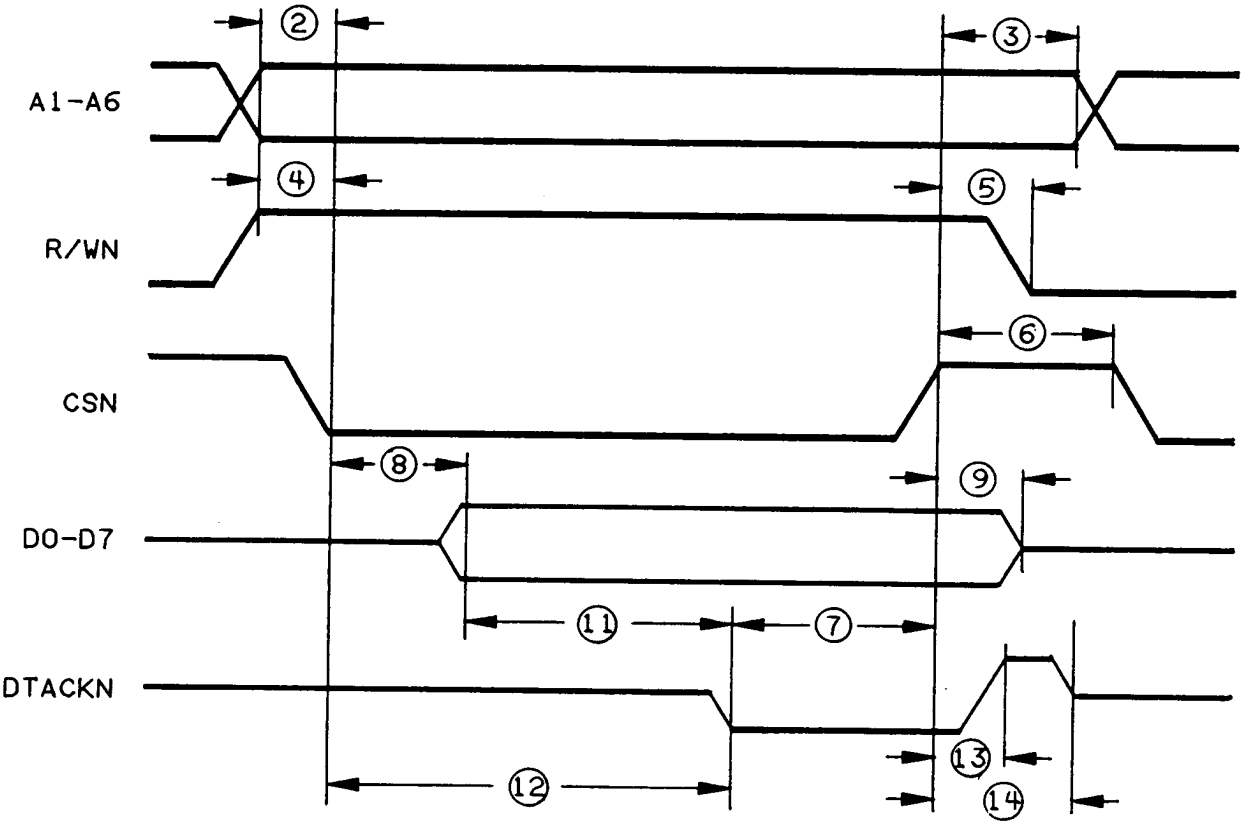

FIGURE 4. Bus timing (read cycle).

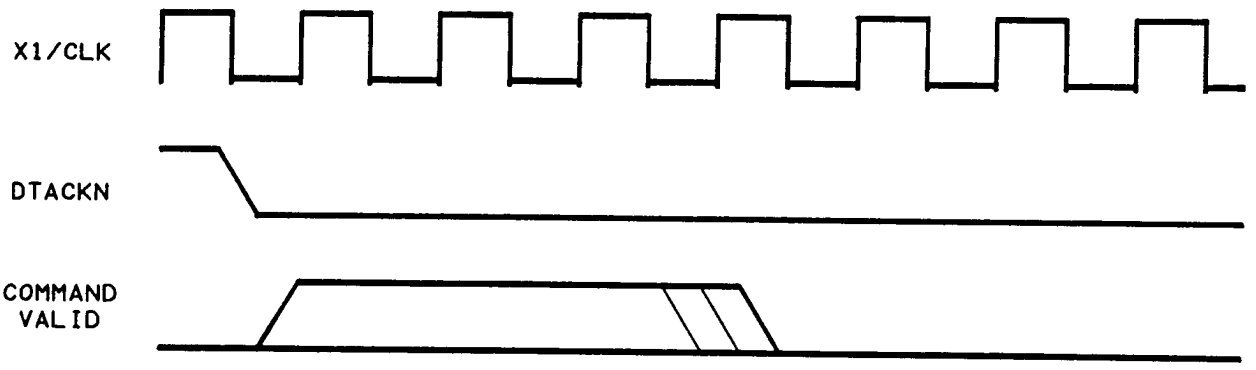

FIGURE 5. Command timing.

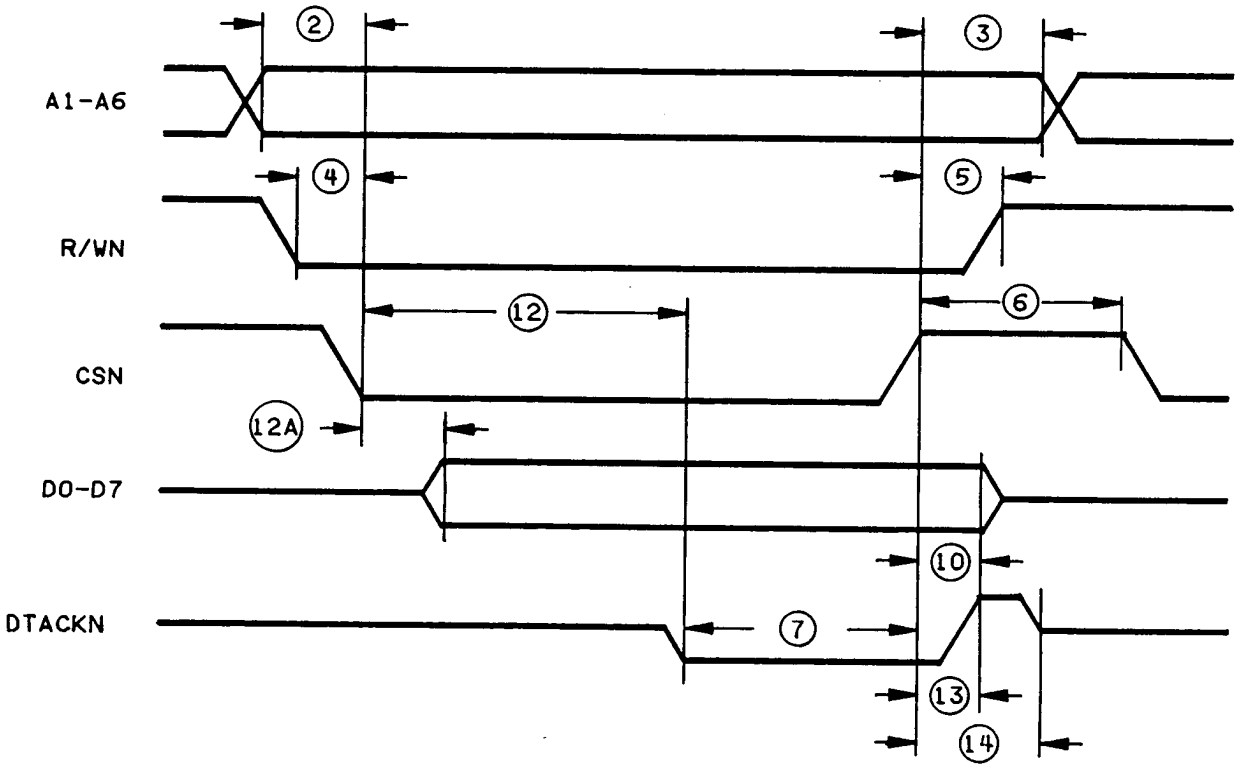

FIGURE 6. Bus timing (write cycle).

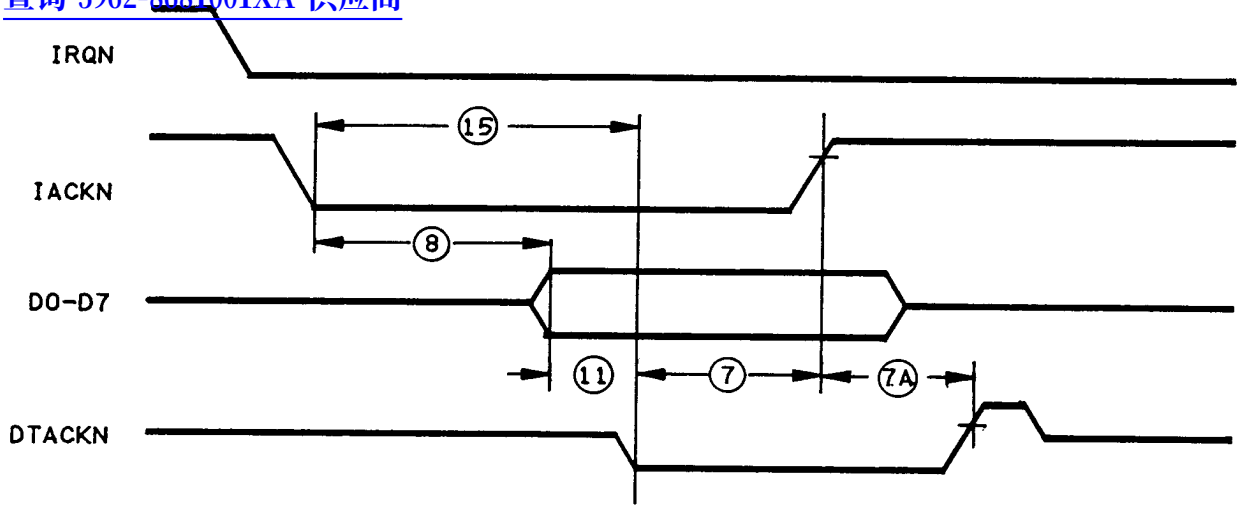

FIGURE 7. Interrupt cycle timing.

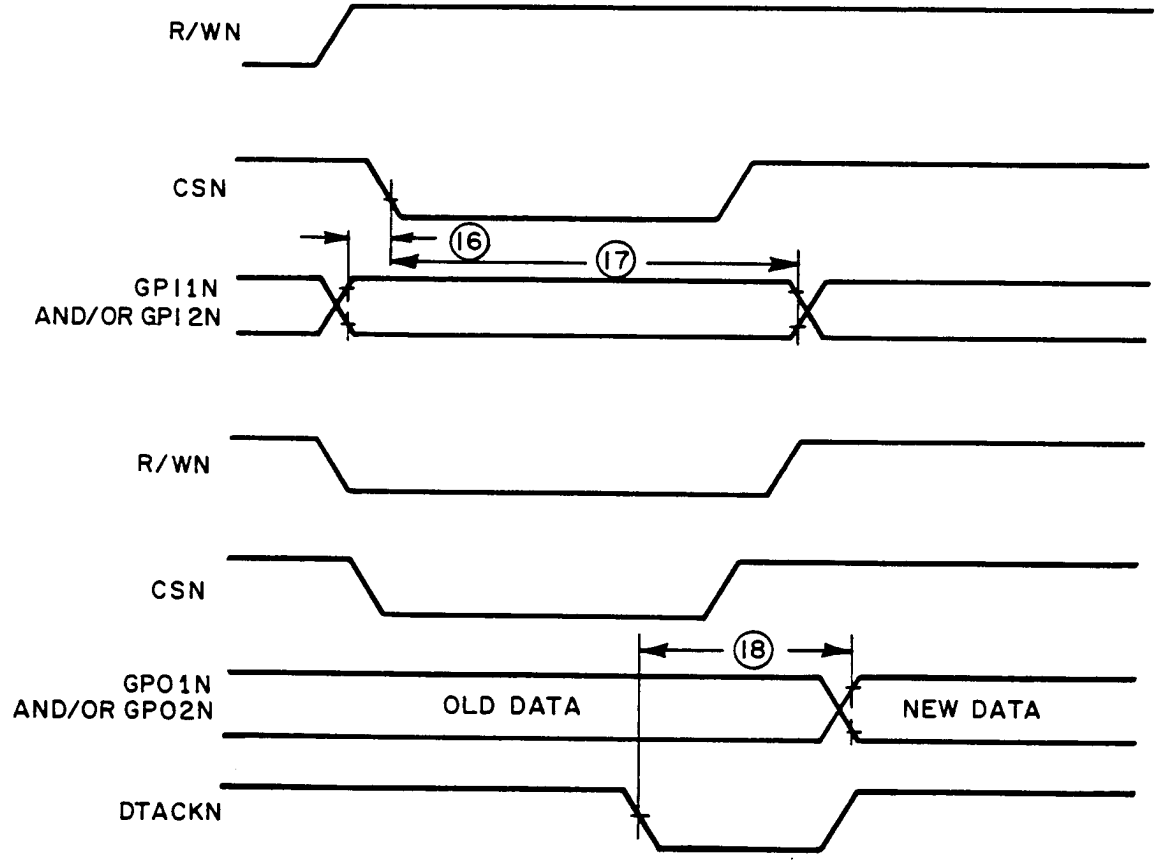

FIGURE 8. Port timing.

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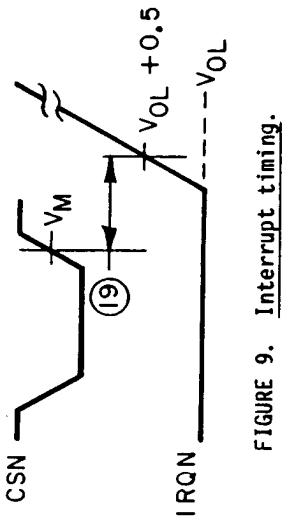
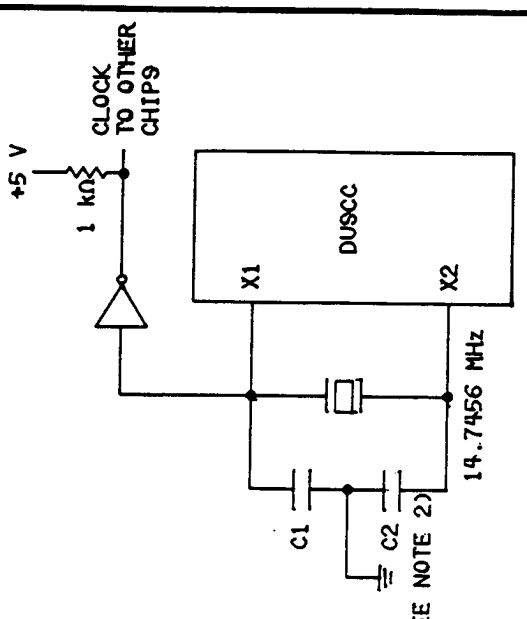
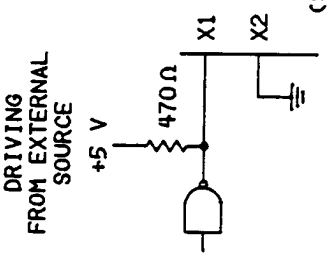
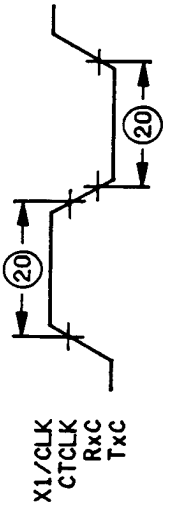


FIGURE 9. Interrupt timing.







NOTES:
1. Crystal series resistance should be less than 180 ohms.
2. C1 = C2: 0 - 5 pF + (stray < 5 pF).

FIGURE 10. Clock timing.

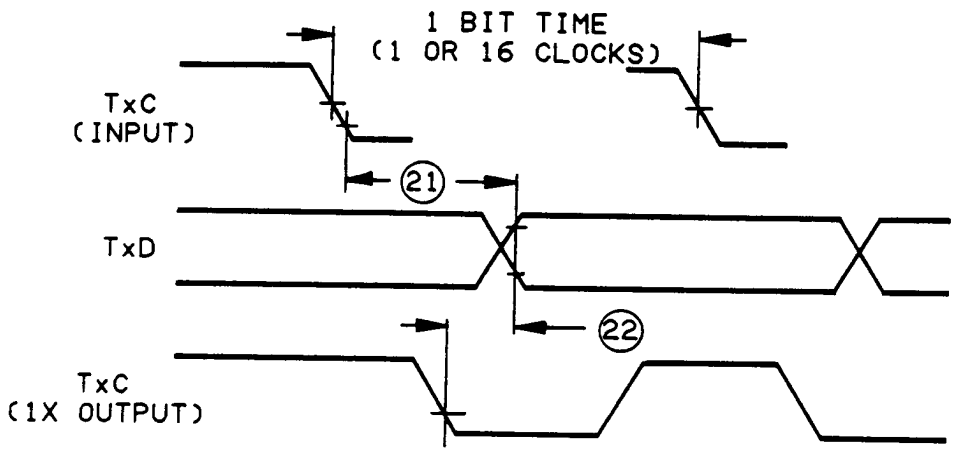


FIGURE 11. Transmit timing.

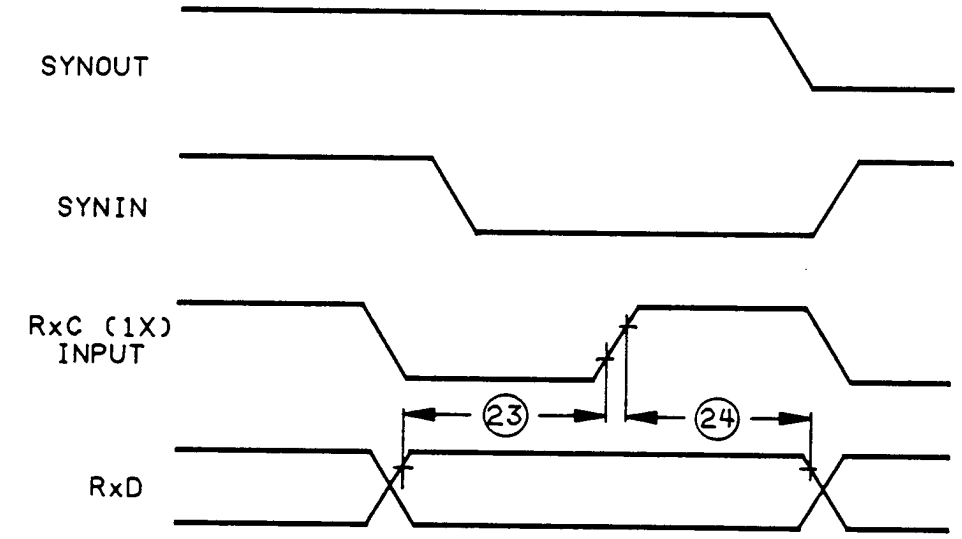


FIGURE 12. Recieve timing.

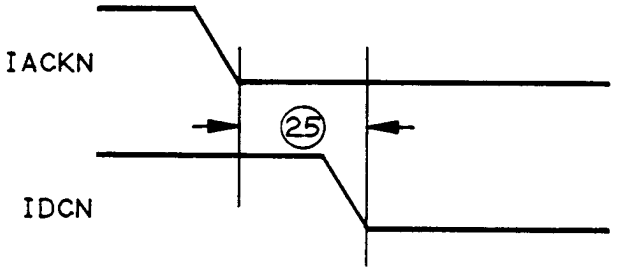


FIGURE 13. Interrupt daisy chain timing.

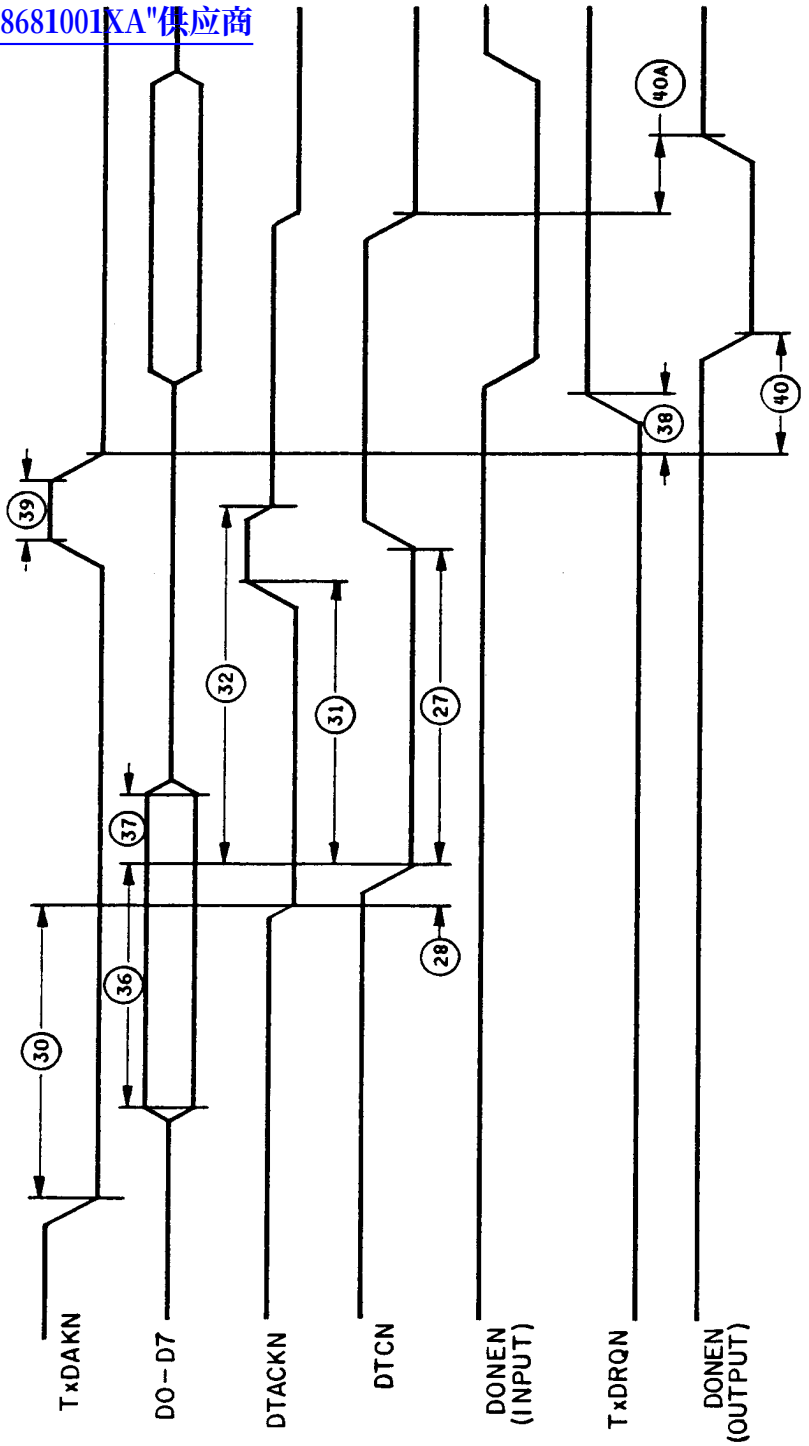


FIGURE 14. DMA transmit write timing - single address DMA mode.

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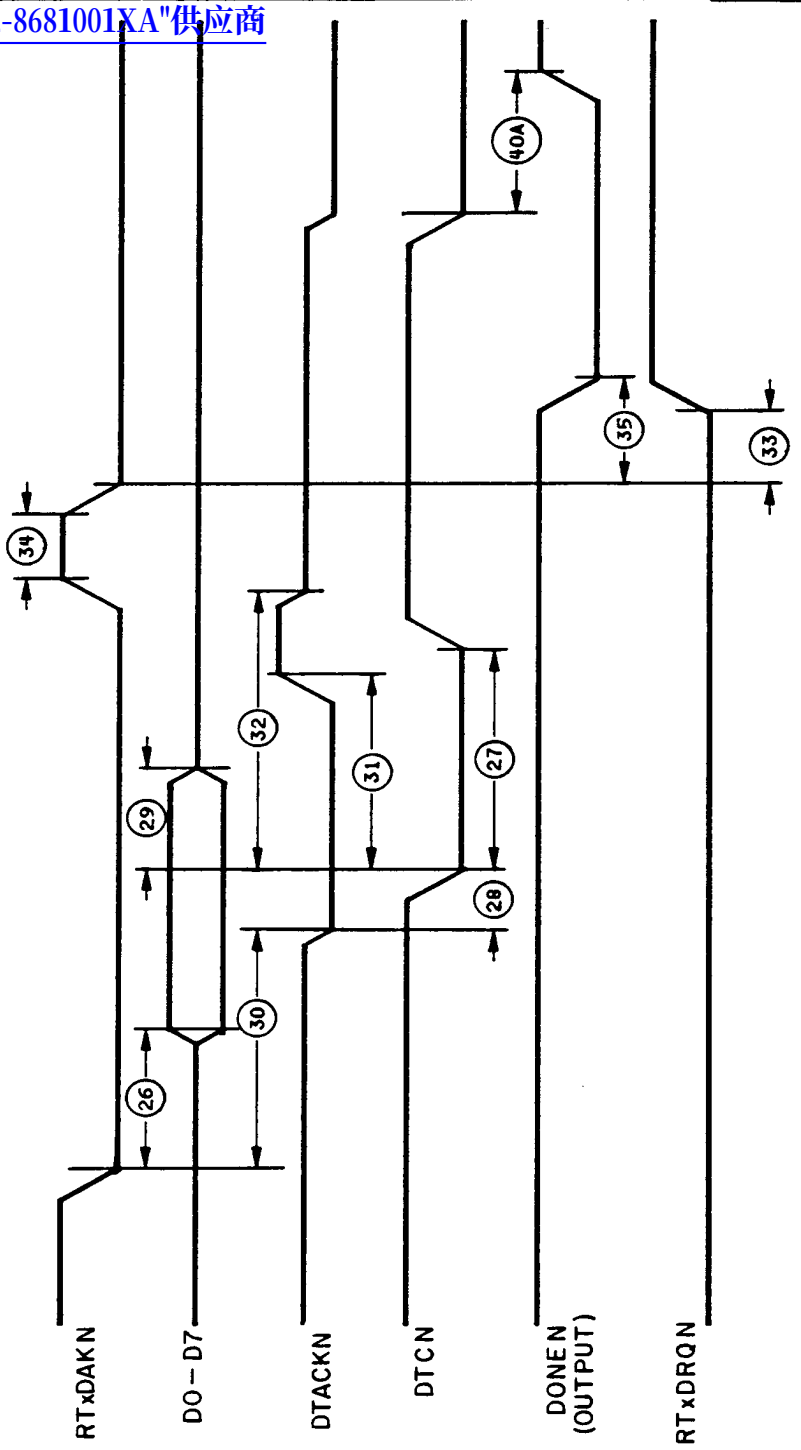

FIGURE 15. DMA reciever read timing - single address DMA mode.

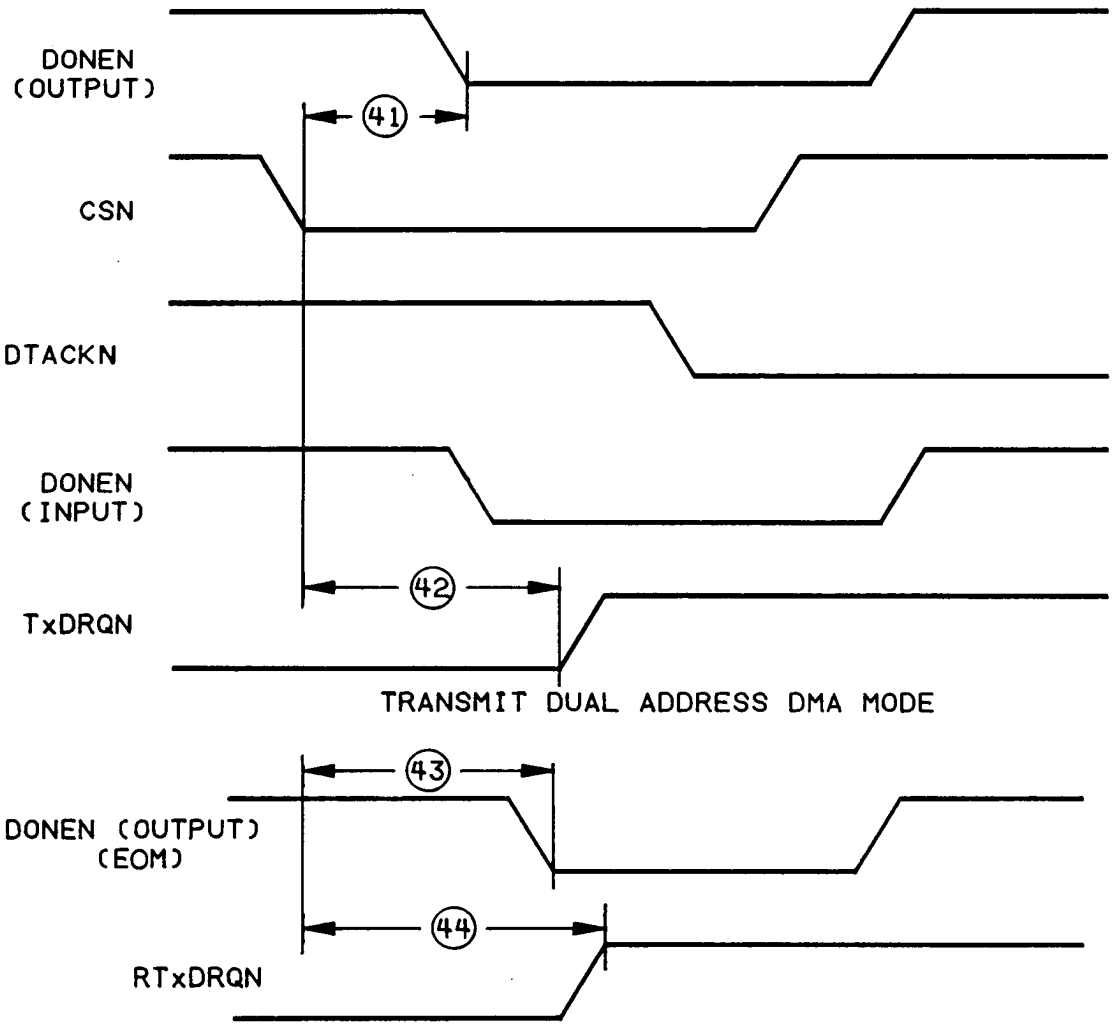

FIGURE 16. Dual address DMA mode timing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

1/ Any subgroup at the same temperature may be combined using a multifunction tester.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions.

Mnemonic	Pin	Type	Name and function
A6-A1	45-47 2-4	I	Address lines: Active high. Address inputs which specify which of the internal registers is accessed for read/write operations.
D7-D0,	18-21 28-31	I/O	Bidirectional data bus: Active high, three-state. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is low, during interrupt acknowledge cycles and single address DMA acknowledge cycles.
R/WN	26	I	Read/Write: A high input indicates a read cycle and a low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	Chip select: Active low input. When low, data transfers between the CPU and the DUSCC are enabled on D0-D7 as controlled by R/WN and A1-A6 inputs. When CSN is high, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single address DMA transfers) and D0-D7 are placed in the 3-state condition.
IRQN	6	O	Interrupt request: Active low, open drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	Interrupt acknowledge: Active low. When IACK is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	Crystal or external clock: When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock must be supplied at this input. This clock input is used to drive the internal bit rate generator, as an optional input to the counter/timer (CT) or digital phase lock loop (DPLL), and to provide other required clocking signals.
X2/IDCN	42	I/O	Crystal or interrupt daisy chain: When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide an interrupt daisy chain active low output which propagates the IACKN signal to lower priority devices if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2 and is not used as an interrupt daisy chain output.

Mnemonic	Pin	Type	Name and function
RESETN	7	I	Master reset: Active low. A low on this pin resets the transmitters and receivers and resets the registers shown in figure 2. Reset is asynchronous, i.e., no clock is required.
RxDA,RxDB	37,12	I	Channel A (B) receiver serial data input: The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA,TxDB	36,13	O	Channel A (B) transmitter serial data output: The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA,RTxCB	39,10	I/O	Channel A (B) receiver/transmitter clock: As an input it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4 MHz.
TRxCA,TRxCB	40,9	I/O	Channel A (B) transmitter/receiver clock: As an input it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter bit rate generator (BRG) clock (16X), the receiver BRG (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4 MHz.
CTSA/BN, LCA/BN	32,17	I/O	Channel A (B) clear to send input or loop control output: Active low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in bit oriented protocol (BOP) loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38,11	I	Channel A (B) data carrier detect or external sync input: The function of this pin is programmable. As a DCD active low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active low external sync input, it is used in character oriented protocol (COP) modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in protocol standard X.21.

Mnemonic	Pin	Type	Name and function
RTxDRQA/BN, GPO1A/BN	34,15	O	Channel A (B) receiver/transmitter DMA service request or general purpose output: Active low. For half duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33,16	O	Channel A (B) transmitter DMA service request or general purpose output or request-to-send: Active low. For full duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full duplex DMA mode, this pin can be programmed as a general purpose output or a request-to-send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	44,5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input: Active low. For half duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	35,14	I	Channel A (B) transmitter DMA acknowledge or general purpose input: Active low. When the channel is programmed for full duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full duplex single address DMA mode.
DTACKN	22	O	Data transfer acknowledge: Active low, 3-state. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-state) a short period after it is negated. In single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-state) a short period after it is negated. When negated, DTACKN becomes an open drain output and requires an external pull-up resistor.
DTCN	23	I	Device transfer complete: Active low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.

Mnemonic	Pin	Type	Name and function
DONEN	27	I/O	Done: Active low open drain.
RTSA/BN, SYNOUTA/BN	41,8	O	Channel A (B) sync detect or request-to-send: Active low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a request-to-send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{CC}	48	I	+5 V ±10 percent power supply.
GND	24	I	Signal and power ground.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8681001XX	18324	68562/BXA	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 South Market Ct. Sacramento, Ca. 95834

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987—549-096