MMBFJ309LT1G, MMBFJ310LT1G

JFET - VHF/UHF Amplifier Transistor

N−Channel

ON Semiconductor®

http://onsemi.com

Features

- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

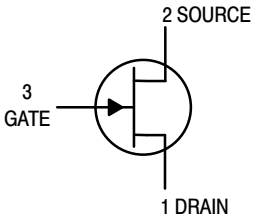
Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DS}	25	Vdc
Gate−Source Voltage	V_{GS}	25	Vdc
Gate Current	I_G	10	mAdc

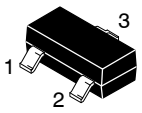
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board, (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

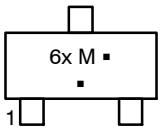
1. FR−5 = 1.0 x 0.75 x 0.062 in.





SOT−23 (TO−236)
CASE 318
STYLE 10

MARKING DIAGRAM



6x = Device Code
x = U for MMBFJ309LT1
x = T for MMBFJ310LT1
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBFJ309LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
MMBFJ310LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate−Source Breakdown Voltage (I_G = −1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	−25	−	−	Vdc
Gate Reverse Current (V_{GS} = −15 Vdc) (V_{GS} = −15 Vdc, T_A = 125°C)		I_{GSS}	− −	− −	−1.0 −1.0	nAdc μAdc
Gate Source Cutoff Voltage (V_{DS} = 10 Vdc, I_D = 1.0 nAdc)	MMBFJ309 MMBFJ310	$V_{GS(off)}$	−1.0 −2.0	− −	−4.0 −6.5	Vdc
ON CHARACTERISTICS						
Zero−Gate−Voltage Drain Current (V_{DS} = 10 Vdc, V_{GS} = 0)	MMBFJ309 MMBFJ310	I_{DSS}	12 24	− −	30 60	mAdc
Gate−Source Forward Voltage (I_G = 1.0 mAdc, V_{DS} = 0)		$V_{GS(f)}$	−	−	1.0	Vdc
SMALL−SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)		$\|Y_{fs}\|$	8.0	−	18	mmhos
Output Admittance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)		$\|y_{os}\|$	−	−	250	μmhos
Input Capacitance (V_{GS} = −10 Vdc, V_{DS} = 0 Vdc, f = 1.0 MHz)		C_{iss}	−	−	5.0	pF
Reverse Transfer Capacitance (V_{GS} = −10 Vdc, V_{DS} = 0 Vdc, f = 1.0 MHz)		C_{rss}	−	−	2.5	pF
Equivalent Short−Circuit Input Noise Voltage (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 100 Hz)		$\bar{e}_n$	−	10	−	$nV/\sqrt{Hz}$

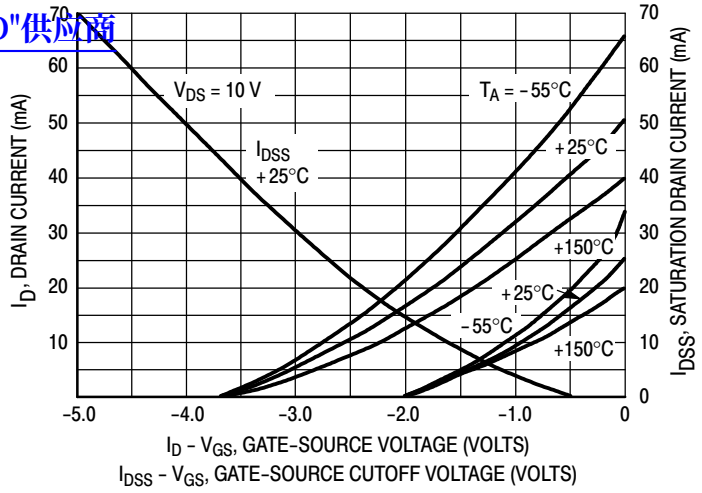


Figure 1. Drain Current and Transfer Characteristics versus Gate−Source Voltage

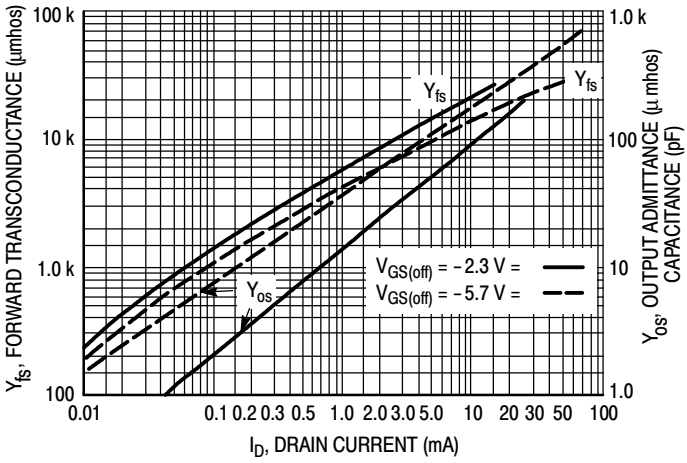


Figure 2. Common−Source Output Admittance and Forward Transconductance versus Drain Current

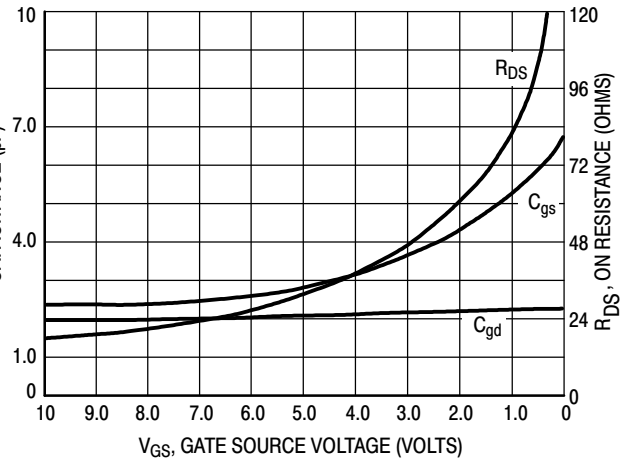


Figure 3. On Resistance and Junction Capacitance versus Gate−Source Voltage

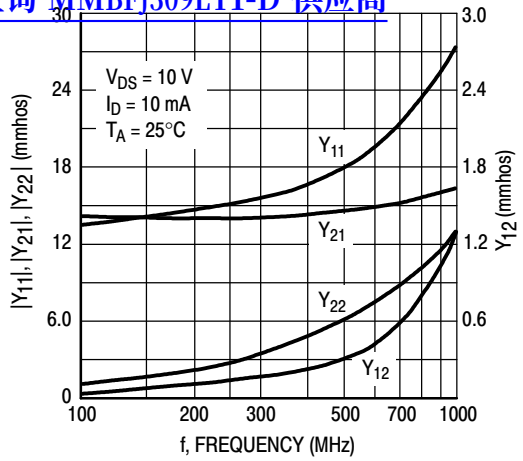


Figure 4. Common−Gate Y Parameter Magnitude versus Frequency

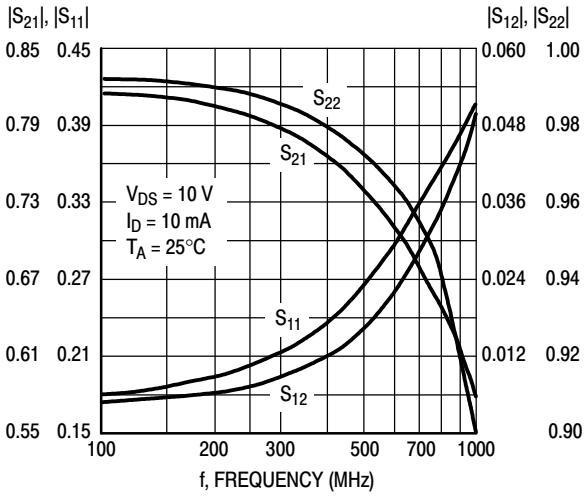


Figure 5. Common−Gate S Parameter Magnitude versus Frequency

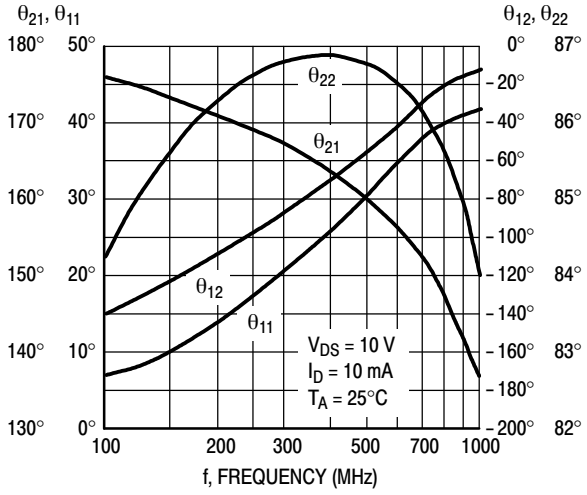


Figure 6. Common−Gate Y Parameter Phase−Angle versus Frequency

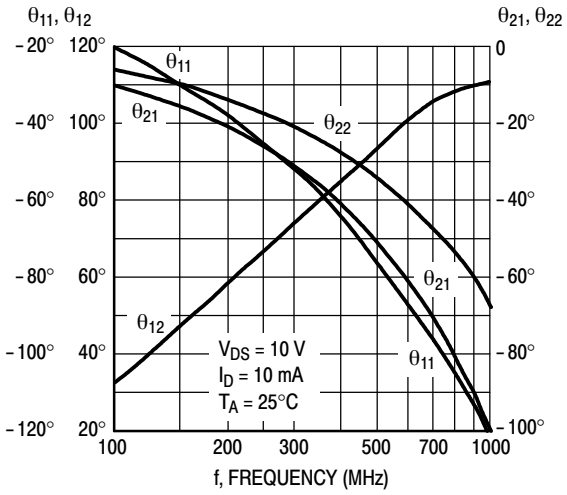
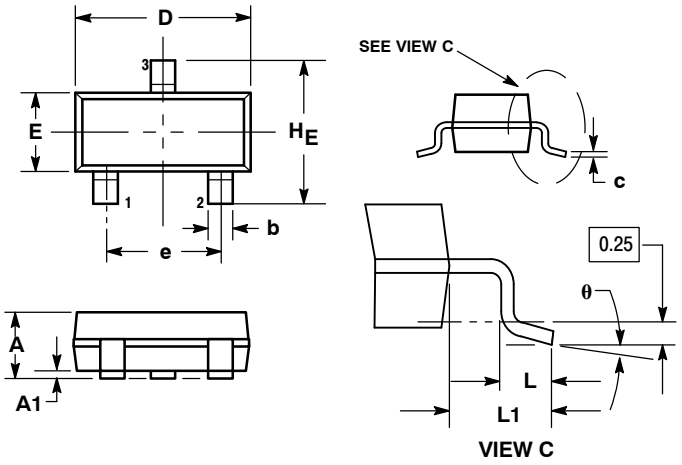


Figure 7. S Parameter Phase−Angle versus Frequency

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

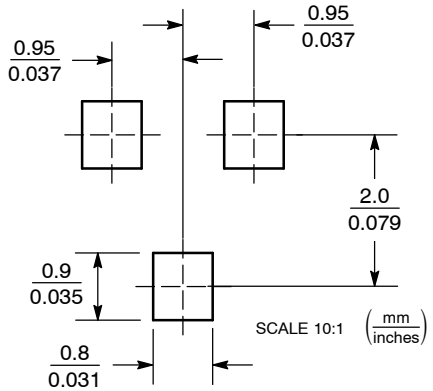


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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