Ultra-Small, Low-Power, SPI™-Compatible, 16-Bit Analog-to-Digital Converter with Internal Reference

Check for Samples: ADS1116, ADS1118

FEATURES

- **ULTRA-SMALL QFN PACKAGE: 2mm × 1,5mm × 0,4mm**
- **WIDE SUPPLY RANGE: 2.0V to 5.5V**
- **LOW CURRENT CONSUMPTION: Continuous Mode: Only 150μA Single-Shot Mode: Auto Shutdown**
- **PROGRAMMABLE DATA RATE: 8SPS to 860SPS**
- **INTERNAL LOW-DRIFT VOLTAGE REFERENCE**
- **INTERNAL OSCILLATOR**
- **INTERNAL PGA**
- **FOUR SINGLE-ENDED OR TWO DIFFERENTIAL INPUTS (ADS1118)**
- **INTERNAL TEMPERATURE SENSOR (ADS1118)**

APPLICATIONS

- **PORTABLE INSTRUMENTATION**
- **CONSUMER GOODS**
- **BATTERY MONITORING**
- **TEMPERATURE MEASUREMENT**
- **FACTORY AUTOMATION AND PROCESS CONTROLS**

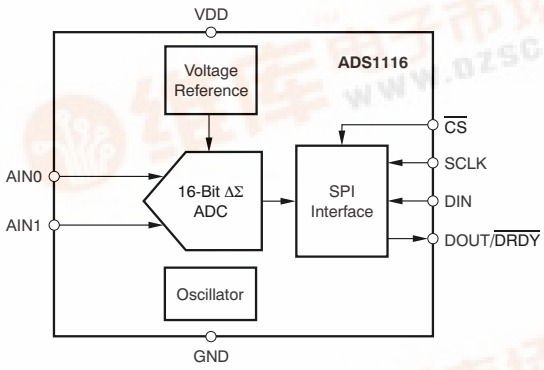
DESCRIPTION

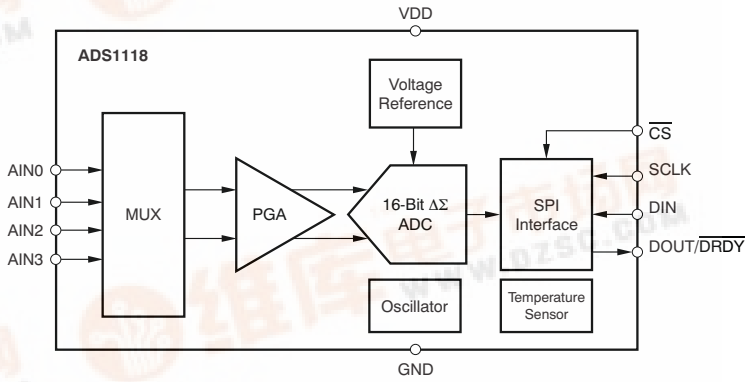
The ADS1116 and ADS1118 are precision analog-to-digital converters (ADCs) with 16 bits of resolution offered in an ultra-small, leadless QFN-10 package or an MSOP-10 package. The ADS1116/8 are designed with precision, power, and ease of implementation in mind. The ADS1116/8 feature an onboard reference and oscillator. Data are transferred via an SPI-compatible serial interface. The ADS1116/8 operate from a single power supply ranging from 2V to 5.5V.

The ADS1116/8 can perform conversions at rates up to 860 samples per second (SPS). An onboard PGA is available on the ADS1118 that offers input ranges from the supply to as low as ±256mV, allowing both large and small signals to be measured with high resolution. The ADS1118 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs.

The ADS1116/8 operate either in continuous conversion mode or a single-shot mode that automatically powers down after a conversion and greatly reduces current consumption during idle periods. The ADS1116/8 are specified from –40°C to +125°C.

PRODUCT PREVIEW





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	ADS1116, ADS1118	UNIT
VDD to GND	–0.3 to +5.5	V
Analog input current	100, momentary	mA
Analog input current	10, continuous	mA
Analog input voltage to GND	–0.3 to VDD + 0.3	V
DIN, DOUT/$\overline{\text{DRDY}}$, SCLK, $\overline{\text{CS}}$ voltage to GND	–0.5 to +5.5	V
Maximum junction temperature	+150	°C
Storage temperature range	–60 to +150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT FAMILY

DEVICE	PACKAGE DESIGNATOR MSOP/QFN	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	TEMPERATURE SENSOR	PGA	INPUT CHANNELS (Differential/ Single-Ended)
ADS1116	TBD	16	860	No	No	1/1
ADS1118	TBD	16	860	Yes	Yes	2/4
ADS1018	TBD	12	3300	Yes	Yes	2/4

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +125°C, VDD = 3.3V, and Full-Scale (FS) = ±2.048V, unless otherwise noted.
Typical values are at +25°C.

PARAMETER	TEST CONDITIONS	ADS1116, ADS1118 MIN	ADS1116, ADS1118 TYP	ADS1116, ADS1118 MAX	UNIT
ANALOG INPUT					
Full-scale input voltage(1)	$V_{IN} = (AIN_P) – (AIN_N)$		±4.096/PGA		V
Analog input voltage	AIN_P or AIN_N to GND	GND		VDD	V
Differential input impedance			See Table 1		
Common-mode input impedance	FS = ±6.144V(1)		10		MΩ
	FS = ±4.096V(1), ±2.048V		6		MΩ
	FS = ±1.024V		3		MΩ
	FS = ±0.512V, ±0.256V		100		MΩ
SYSTEM PERFORMANCE					
Resolution	No missing codes	16			Bits
Data rate (DR)			8, 16, 32, 64, 128, 250, 475, 860		SPS
Data rate variation	All data rates	–10		10	%
Output noise		See Typical Characteristics			
Integral nonlinearity	DR = 8SPS, FS = ±2.048V, best fit(2)			1	LSB
Offset error	FS = ±2.048V, differential inputs		±1	±3	LSB
	FS = ±2.048V, single-ended inputs		±3		LSB
Offset drift	FS = ±2.048V		0.005		LSB/°C
Offset power-supply rejection	FS = ±2.048V		1		LSB/V
Gain error(3)	FS = ±2.048V at +25°C		0.01	0.15	%
Gain drift(3)	FS = ±0.256V		7		ppm/°C
	FS = ±2.048V		5	40	ppm/°C
	FS = ±6.144V(1)		5		ppm/°C
Gain power-supply rejection			80		ppm/V
PGA gain match(3)	Match between any two PGA gains		0.02	0.1	%
Gain match	Match between any two inputs		0.05	0.1	%
Offset match	Match between any two inputs		3		LSB
Common-mode rejection	At dc and FS = ±0.256V		105		dB
	At dc and FS = ±2.048V		100		dB
	At dc and FS = ±6.144V(1)		90		dB
	f_{CM} = 60Hz, DR = 8SPS		105		dB
	f_{CM} = 50Hz, DR = 8SPS		105		dB
Temperature sensor accuracy	–25°C to +85°C		0.2		°C
	–40°C to +125°C		0.4		°C
	vs Supply		0.2		°C/V

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.
(2) 99% of full-scale.
(3) Includes all errors from onboard PGA and reference.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

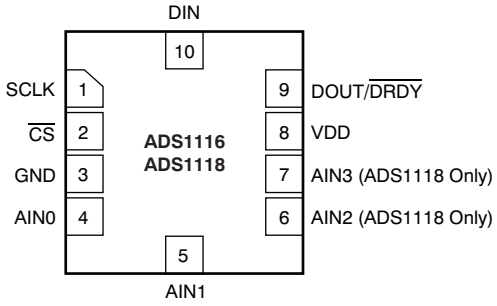
All specifications at –40°C to +125°C, VDD = 3.3V, and Full-Scale (FS) = ±2.048V, unless otherwise noted.
Typical values are at +25°C.

PARAMETER	TEST CONDITIONS	ADS1116, ADS1118			UNIT
		MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT					
Logic level					
V_{IH}		0.7VDD		5.5	V
V_{IL}		GND – 0.5		0.3VDD	V
V_{OH}	I_{OH} = 1mA	0.8VDD			V
V_{OL}	I_{OL} = 1mA	GND		0.2VDD	V
Input leakage					
I_H	V_{IH} = 5.5V			10	µA
I_L	V_{IL} = GND	10			µA
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage		2		5.5	V
Supply current	Power-down current at +25°C		0.5	2	µA
	Power-down current up to +125°C			5	µA
	Operating current at +25°C		150	200	µA
	Operating current up to +125°C			300	µA
Power dissipation	VDD = 5.0V		0.9		mW
	VDD = 3.3V		0.5		mW
	VDD = 2.0V		0.3		mW
TEMPERATURE					
Storage temperature		–60		+150	°C
Specified temperature		–40		+125	°C

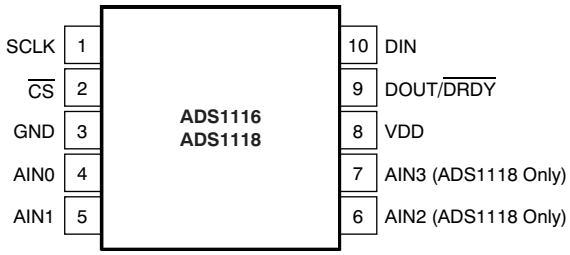
PRODUCT PREVIEW

PIN CONFIGURATIONS

RUG PACKAGE
QFN-10
(TOP VIEW)



DGS PACKAGE
MSOP-10
(TOP VIEW)



PIN DESCRIPTIONS

PIN #	DEVICE		ANALOG/ DIGITAL INPUT/ OUTPUT	DESCRIPTION
	ADS1116	ADS1118		
1	SCLK	SCLK	Digital Input	Serial clock input
2	$\overline{CS}$	$\overline{CS}$	Digital Input	Chip select; active low
3	GND	GND	Analog	Ground
4	AIN0	AIN0	Analog Input	Differential channel 1: Positive input or single-ended channel 1 input
5	AIN1	AIN1	Analog Input	Differential channel 1: Negative input or single-ended channel 2 input
6	NC(1)	AIN2	Analog Input	Differential channel 2: Positive input or single-ended channel 3 input (NC for ADS1116)
7	NC	AIN3	Analog Input	Differential channel 2: Negative input or single-ended channel 4 input (NC for ADS1116)
8	VDD	VDD	Analog	Power supply: 2V to 5.5V
9	DOUT/$\overline{DRDY}$	DOUT/$\overline{DRDY}$	Digital Output	Serial data out combined with data ready; active low
10	DIN	DIN	Digital Input	Serial data input

(1) NC pins may be left floating or tied to ground.

PRODUCT PREVIEW

SPI TIMING CHARACTERISTICS

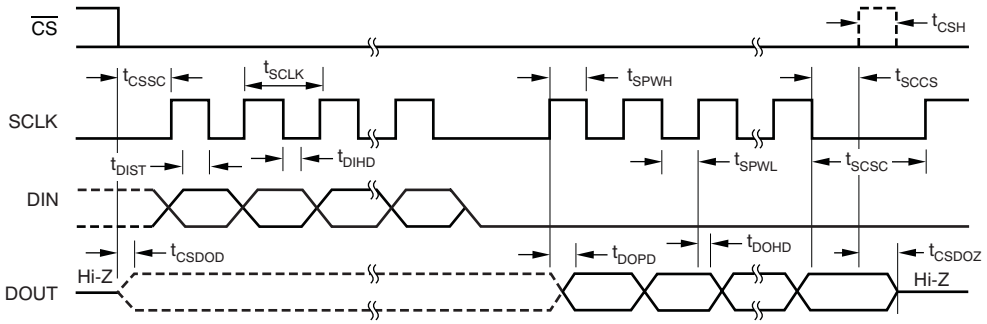


Figure 1. Serial Interface Timing

TIMING REQUIREMENTS: SERIAL INTERFACE TIMING

At T_A = –40°C to +125°C and VDD = 2V to 5.5V, unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{CSSC}	$\overline{CS}$ low to first SCLK: setup time(1)	100		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	SCLK pulse width: high	100		ns
t_{SPWL}	SCLK pulse width: low(2)	100		ns
			2^{18}	t_{CLK}
t_{DIST}	Valid DIN to SCLK falling edge: setup time	50		ns
t_{DIHD}	Valid DIN to SCLK falling edge: hold time	50		ns
t_{DOPD}	SCLK rising edge to valid new DOUT: propagation delay(3)		50	ns
t_{DOHD}	SCLK rising edge to DOUT invalid: hold time	0		ns
t_{SCSC}	Final SCLK falling edge of op code command to first SCLK rising edge of next op code command	8		t_{CLK}
t_{CSDOD}	$\overline{CS}$ low to DOUT driven: propagation delay	100		ns
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z: propagation delay	100		ns
t_{CSH}	$\overline{CS}$ high pulse	4		µs
t_{SCCS}	Final SCLK falling edge to $\overline{CS}$ high	16		µs

(1) $\overline{CS}$ can be tied low.
(2) Holding SCLK low longer than 28µs resets the SPI interface (enabled by SPIRST bit).
(3) DOUT load = 20pF || 100kΩ to DGND.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

OPERATING CURRENT vs TEMPERATURE

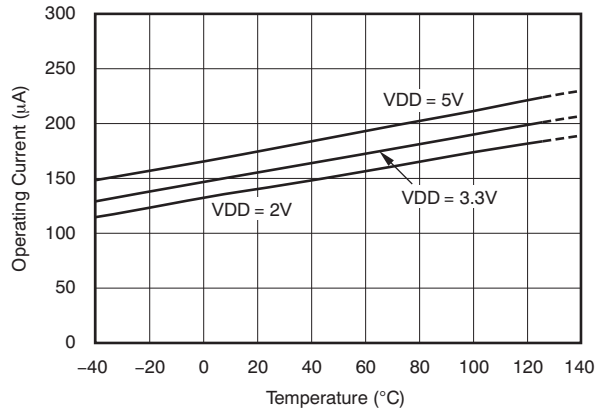


Figure 2.

SHUTDOWN CURRENT vs TEMPERATURE

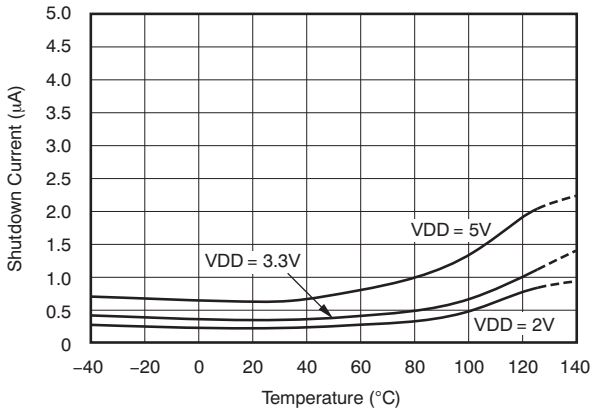


Figure 3.

SINGLE-ENDED OFFSET ERROR vs TEMPERATURE(1)

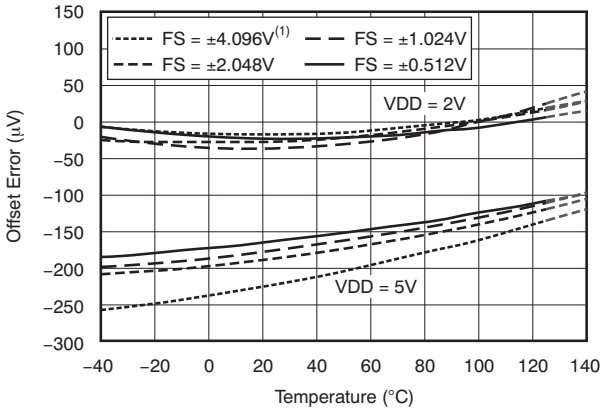


Figure 4.

DIFFERENTIAL OFFSET vs TEMPERATURE

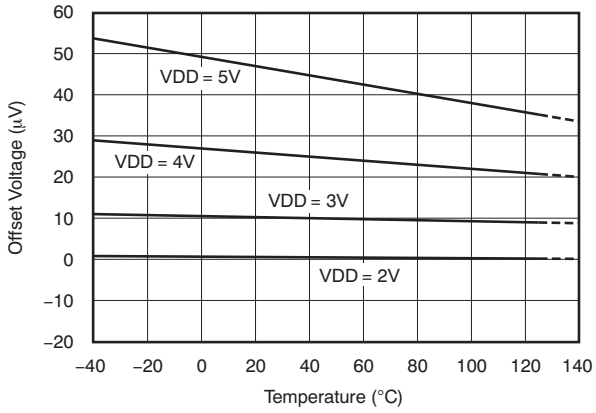


Figure 5.

GAIN ERROR vs TEMPERATURE

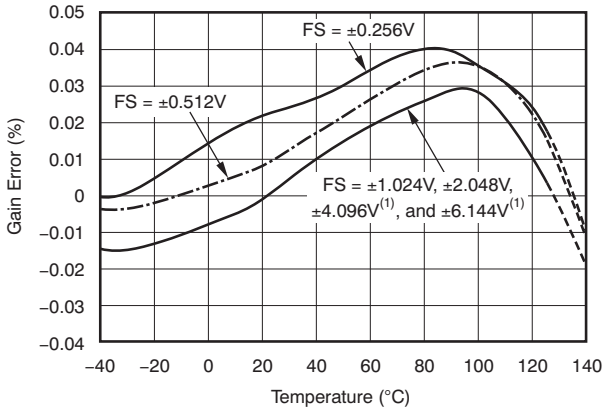


Figure 6.

GAIN ERROR vs SUPPLY

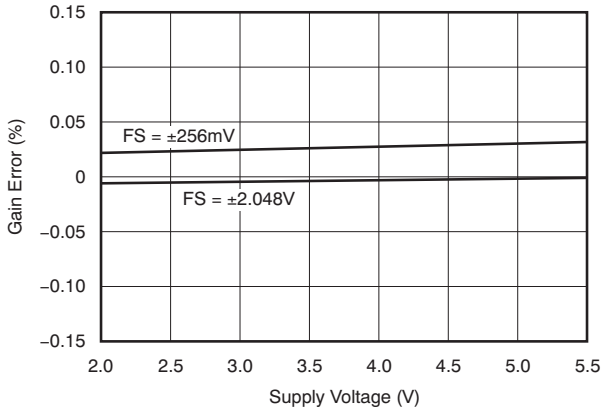


Figure 7.

PRODUCT PREVIEW

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

INL vs SUPPLY VOLTAGE(2)

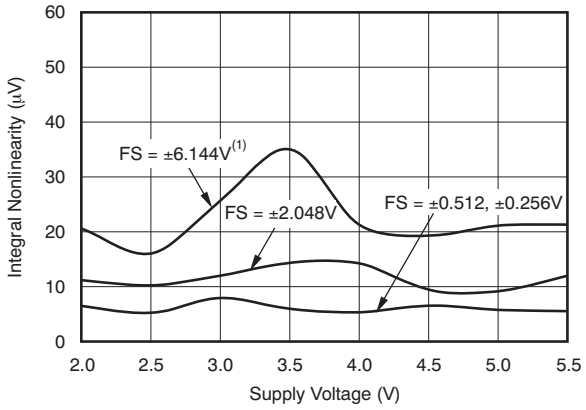


Figure 8.

INL vs INPUT SIGNAL

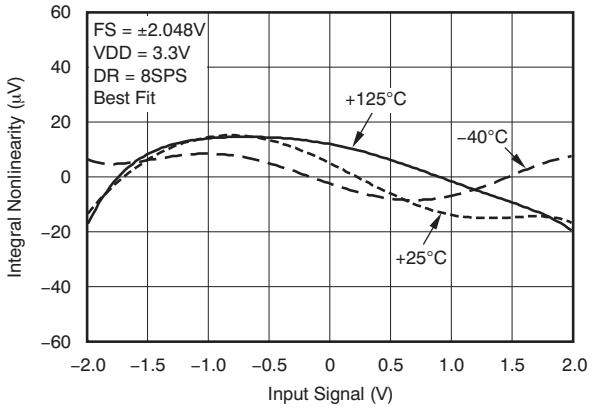


Figure 9.

INL vs INPUT SIGNAL

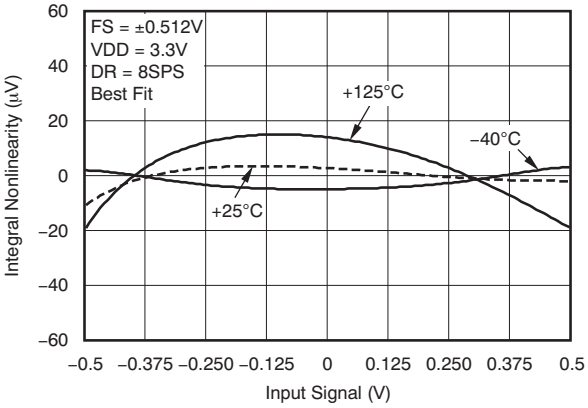


Figure 10.

INL vs INPUT SIGNAL

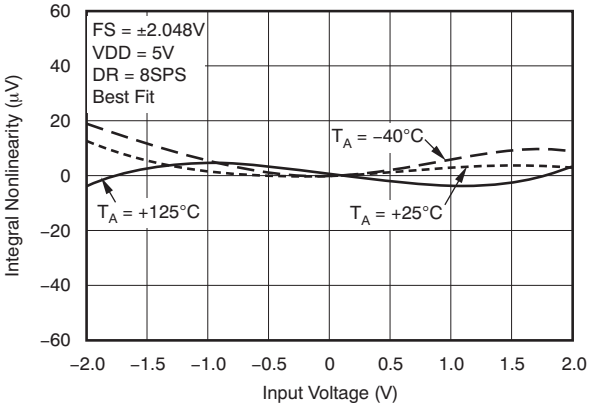


Figure 11.

INL vs INPUT SIGNAL

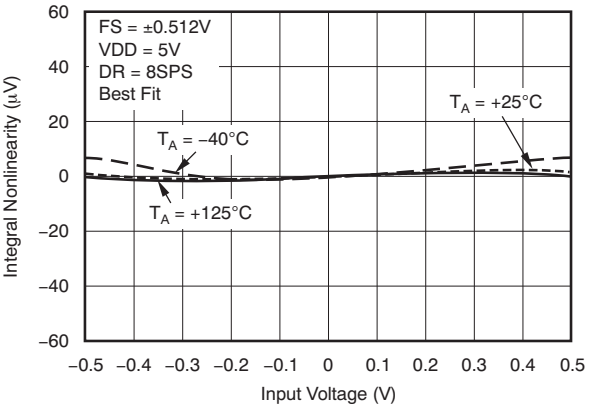


Figure 12.

INL vs TEMPERATURE

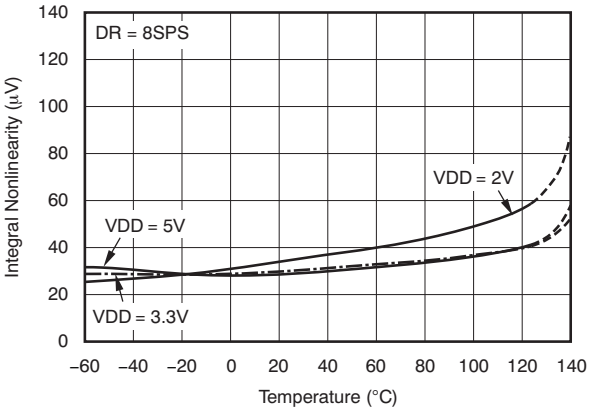


Figure 13.

(2) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

NOISE vs INPUT SIGNAL

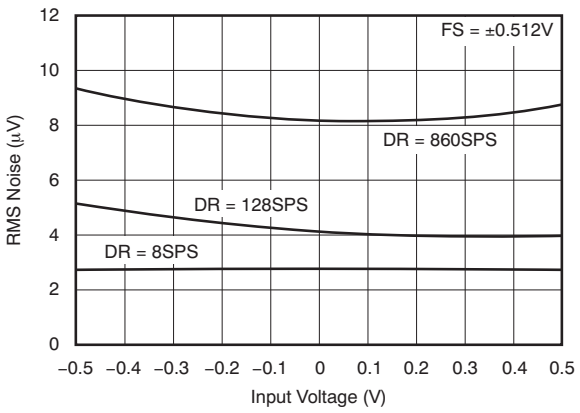


Figure 14.

NOISE vs SUPPLY VOLTAGE

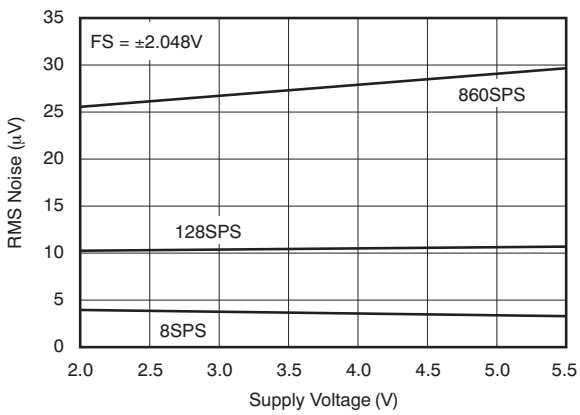


Figure 15.

NOISE vs TEMPERATURE

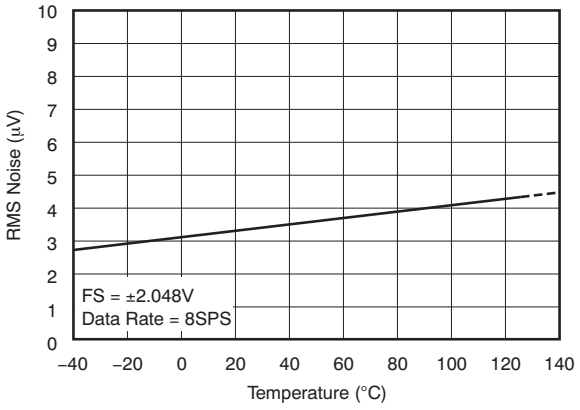


Figure 16.

GAIN ERROR HISTOGRAM

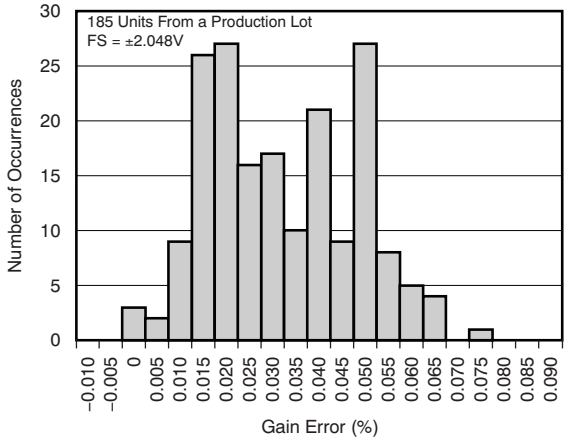


Figure 17.

OFFSET HISTOGRAM

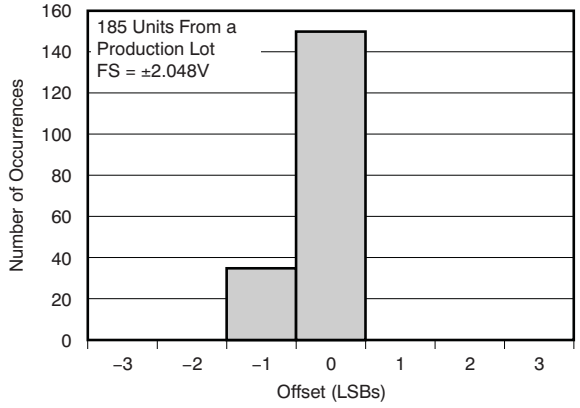


Figure 18.

TOTAL ERROR vs INPUT SIGNAL

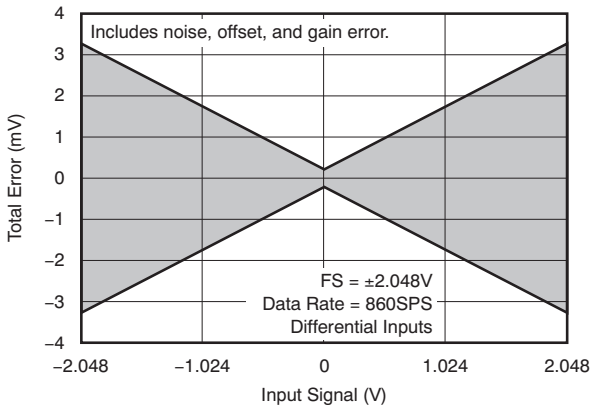


Figure 19.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

DATA RATE vs TEMPERATURE

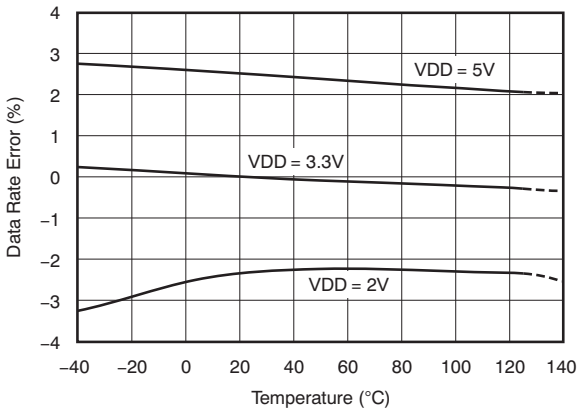


Figure 20.

FREQUENCY RESPONSE

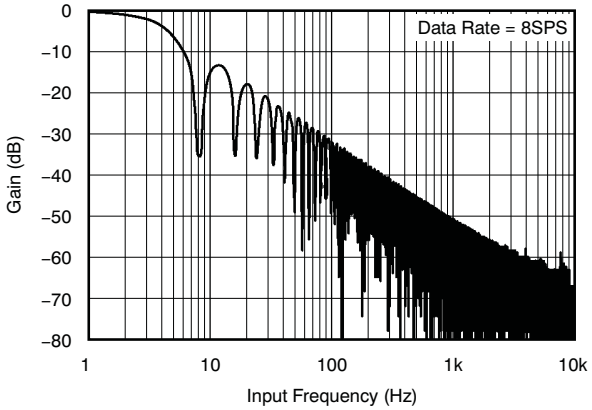


Figure 21.

PRODUCT PREVIEW

OVERVIEW

The ADS1116/8 are very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The ADS1116/8 are extremely easy to configure and design into a wide variety of applications, and allow precise measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the ADS1116/8 family to be intuitive and problem-free.

The ADS1116/8 consist of a ΔΣ analog-to-digital (A/D) core with adjustable gain (excludes the ADS1116), an internal voltage reference, a clock oscillator, and a serial interface (SPI). An additional feature available on the ADS1118 is a programmable digital comparator that provides an alert on a dedicated pin. All of these features are intended to reduce required external circuitry and improve performance. Figure 22 shows the ADS1118 functional block diagram.

The ADS1116/8 A/D core measures a differential signal, V_{IN}, that is the difference of AIN_P and AIN_N. A MUX is available on the ADS1118. This architecture results in a very strong attenuation in any common-mode signals. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1116/8 have two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal result register. The device then enters a low-power shutdown mode. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion.

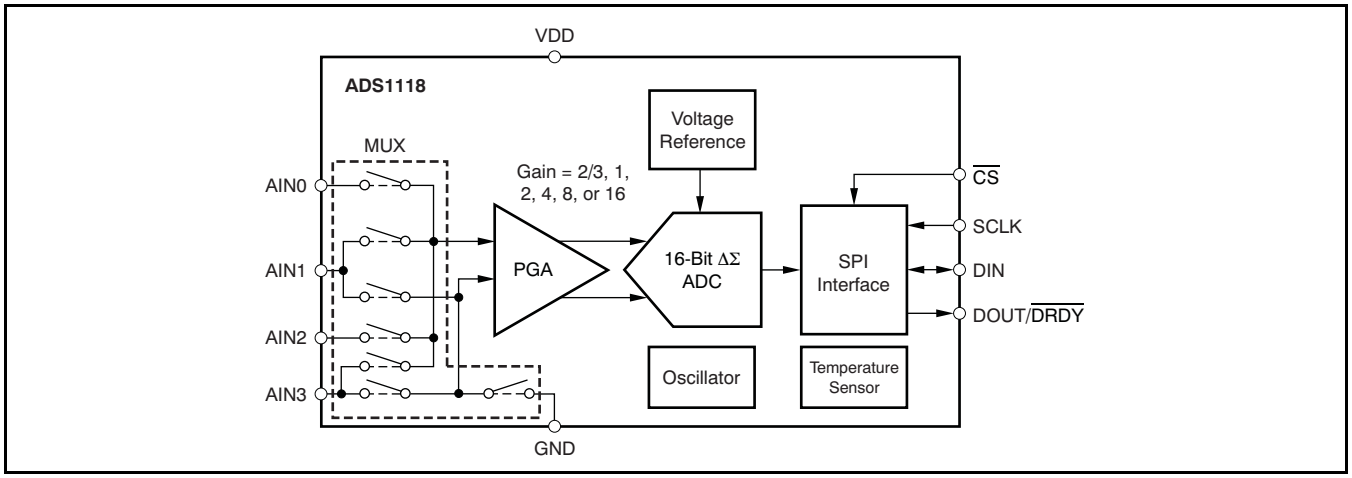


Figure 22. ADS1118 Functional Block Diagram

PRODUCT PREVIEW

MULTIPLEXER

The ADS1118 contains an input multiplexer, as shown in Figure 23. Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 may be measured differentially to AIN3. The multiplexer is configured by three bits in the Config Register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

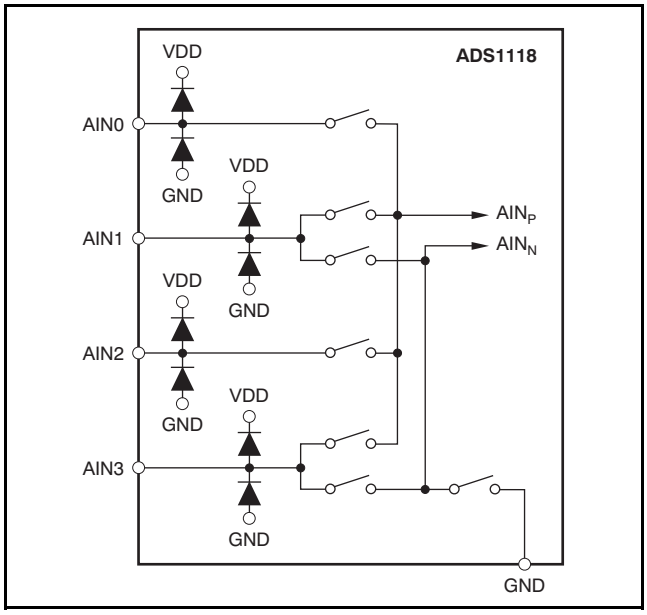


Figure 23. ADS1118 MUX

The ADS1116 does not have a multiplexer. Either one differential or one single-ended signal may be measured with these devices. For single-ended measurements, connect the AIN1 pin to GND. Note that in subsequent sections of this data sheet, AIN_P refers to AIN0 and AIN_N refers to AIN1 for the ADS1116 device.

When measuring single-ended inputs it is important to note that the negative range of the output codes are not used. These codes are for measuring negative differential signals such as (AIN_P – AIN_N) < 0. ESD diodes to VDD and GND protect the inputs on both devices (ADS1116 and ADS1118). To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the following range:

GND – 0.3V < AINx < VDD + 0.3V (1)

If it is possible that the voltages on the input pins may violate these conditions, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

Also, overdriving one unused input on the ADS1118 may affect conversions taking place on other input pins. If overdrive on unused inputs is possible, it is recommended to clamp the signal with external Schottky diodes.

ANALOG INPUTS

The ADS1116/8 use a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The capacitors used are small, and to external circuitry the average loading appears resistive. This structure is shown in Figure 25. The resistance is set by the capacitor values and the rate at which they are switched. Figure 24 shows the on/off setting of the switches illustrated in Figure 25. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to AIN_P, C_{A2} to AIN_N, and C_B to (AIN_P – AIN_N). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7V and C_B discharges to 0V. This charging draws a very small transient current from the source driving the ADS1116/8 analog inputs. The average value of this current can be used to calculate the effective impedance (R_{eff}), where $R_{eff} = V_{IN}/I_{AVERAGE}$.

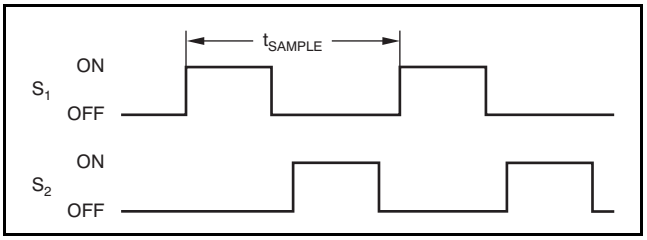


Figure 24. S_1 and S_2 Switch Timing for Figure 25

PRODUCT PREVIEW

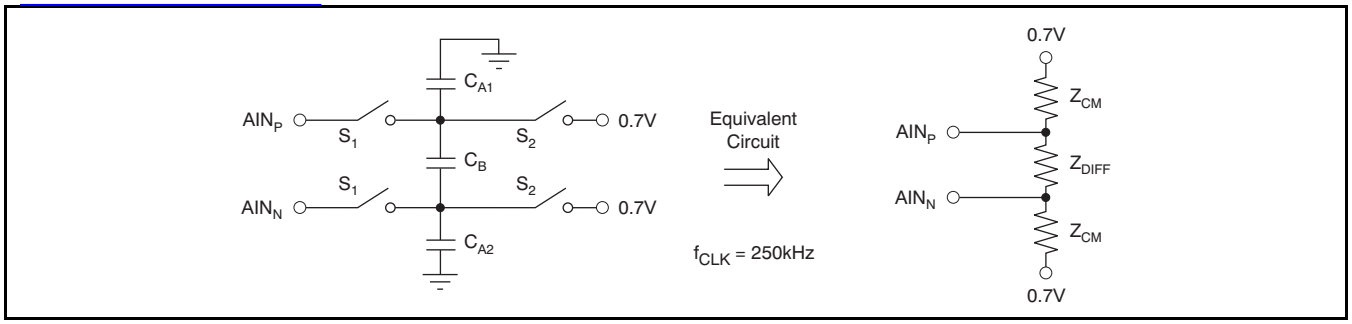


Figure 25. Simplified Analog Input Circuit

The common-mode input impedance is measured by applying a common-mode signal to shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately 6MΩ for the default PGA gain setting. In Figure 25, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7V. The current that flows through the pin connected to 0.7V is the differential current and scales with the PGA gain setting. In Figure 25, the differential input impedance is Z_{DIFF}. Table 1 describes the typical differential input impedance.

Table 1. Differential Input Impedance

FS (V)	DIFFERENTIAL INPUT IMPEDANCE
±6.144V(1)	22MΩ
±4.096V(1)	15MΩ
±2.048V	4.9MΩ
±1.024V	2.4MΩ
±0.512V	710kΩ
±0.256V	710kΩ

1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1116/8 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Note that active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in Table 1 for typical input impedance are valid.

FULL-SCALE INPUT

A programmable gain amplifier (PGA) is implemented before the ΔΣ core of the ADS1118. The PGA can be set to gains of 2/3, 1, 2, 4, 8, and 16. Table 2 shows the corresponding full-scale (FS) ranges. The PGA is configured by three bits in the Config register. The ADS1116 has a fixed full-scale input range of ±2.048V. The PGA = 2/3 setting allows input measurement to extend up to the supply voltage when VDD is larger than 4V. Note though that in this case (as well as for PGA = 1 and VDD < 4V), it is not possible to reach a full-scale output code on the ADC. Analog input voltages may never exceed the analog input voltage limits given in the Electrical Characteristics table.

Table 2. PGA Gain Full-Scale Range

PGA SETTING	FS (V)
2/3	±6.144V(1)
1	±4.096V(1)
2	±2.048V
4	±1.024V
8	±0.512V
16	±0.256V

1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

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DATA FORMAT

The ADS1116/8 provide 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Figure 26 shows code transitions versus input voltage.

Table 3. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ FS (2^{15} – 1)/2^{15}	7FFFh
+FS/2^{15}	0001h
0	0
–FS/2^{15}	FFFFh
≤ –FS	8000h

1. Excludes the effects of noise, INL, offset, and gain errors.

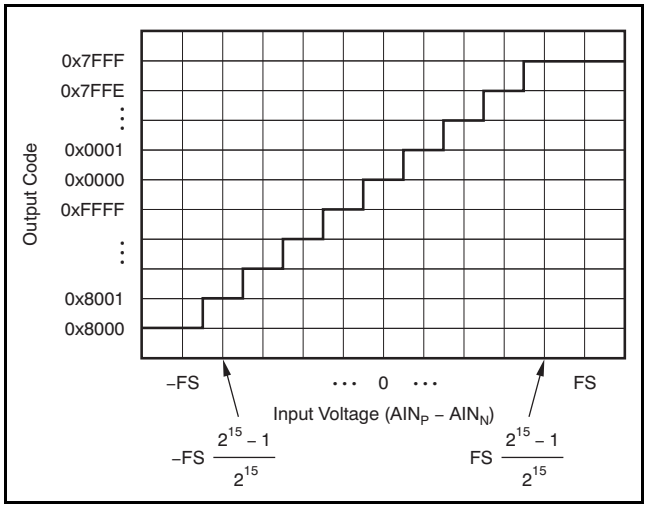

Figure 26. ADS1116/8 Code Transition Diagram

ALIASING

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. Nevertheless, they can contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1116/8 digital filter provides some attenuation of high-frequency noise, but the digital sinc filter frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter is adequate.

When designing an input filter circuit, be sure to take into account the interaction between the filter network and the input impedance of the ADS1116/8.

OPERATING MODES

The ADS1116/8 operate in one of two modes: continuous conversion or single-shot. In continuous conversion mode, the ADS1116/8 continuously perform conversions. Once a conversion has been completed, the ADS1116/8 place the result in the Conversion Register and immediately begin another conversion. In single-shot mode, the ADS1116/8 wait until the OS bit is set high. Once asserted, the bit is set to '0', indicating that a conversion is currently in progress. Once conversion data are ready, the OS bit reasserts and the device powers down. Writing a '1' to the OS bit during a conversion has no effect.

RESET AND POWER-UP

When the ADS1116/8 powers up, a reset is performed. As part of the reset process, the ADS1116/8 set all of the bits in the Config Register to the respective default settings.

DUTY CYCLING FOR LOW POWER

For many applications, improved performance at low data rates may not be required. For these applications, the ADS1116/8 support duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1116/8 in power-down mode with a data rate set to 860SPS could be operated by a microcontroller that instructs a single-shot conversion every 125ms (8SPS). Because a conversion at 860SPS only requires about 1.2ms, the ADS1116/8 enter power-down mode for the remaining 123.8ms. In this configuration, the ADS1116/8 consume about 1/100th the power of the ADS1116/8 operated in continuous conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller. The ADS1116/8 offer lower data rates that do not implement duty cycling as well as improved noise performance if it is needed.

PRODUCT PREVIEW

SERIAL INTERFACE

The SPI-compatible serial interface consists of either four signals: $\overline{CS}$, SCLK, DIN, and DOUT; or three signals, in which case $\overline{CS}$ may be tied low. The interface is used to read conversion data, read and write registers, and control the ADS1118 operation.

CHIP SELECT ($\overline{CS}$)

The chip select ($\overline{CS}$) selects the ADS1116/8 for SPI communication. This feature is useful when multiple devices share the serial bus. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT enters a high-impedance state; as such, DOUT cannot provide indication of data ready. If the ADS1116/8 do not share the serial bus with another device, $\overline{CS}$ may be tied low.

SERIAL CLOCK (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT pins into and out of the ADS1116/8. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for $2^{16}/f_{CLK}$ periods, the serial interface resets and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

DATA INPUT (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1116/8 (op code commands and register data). The devices latch data on DIN on the falling edge of SCLK.

DATA OUTPUT (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADS1118. In Read Data Continuous mode, DOUT goes low when conversion data are ready and goes high 16 CLK cycles before the data ready signal. **Fig TBD** shows DOUT with $\overline{CS}$ = 0 and no data retrieval. Data on DOUT are shifted out on the rising edge of SCLK. DOUT goes to a high-impedance state when $\overline{CS}$ is high.

POWER-DOWN MODE

When the PWDN bit in the configuration register is set to '1', or the op code for power-down mode is sent, the ADS1118 enters a lower power standby state. This condition is also the default state the ADS1118 enters when power is supplied. In this mode, the ADS1118 uses no more than 2μA of current. During this time, the device responds to commands, but does not perform any data conversion. To exit this mode, simply send the op code to enable continuous conversion mode, or write a '0' to the PWDN bit in the configuration register.

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REGISTERS

The ADS1116/8 has two registers that are accessible via the SPI port. The Conversion Register contains the result of the last conversion. The Config Register allows the user to change the ADS1116/8 operating modes and query the status of the devices.

Conversion Register

This 16-bit register contains the result of the last conversion in binary twos complement format. Following power-up, the Conversion Register is cleared to '0', and remains '0' until the first conversion is completed.

The register format is shown in Table 4.

Config Register

The 16-bit register can be used to control the ADS1116/8 operating mode, input selection, data rate, PGA settings, and comparator modes. The register format is shown in Table 5.

Table 4. Conversion Register (Read-Only)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. Config Register (Read/Write)

BIT	15	14	13	12	11	10	9	8
NAME	OS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
BIT	7	6	5	4	3	2	1	0
NAME	DR2	DR1	DR0	TS_MODE	PULL_UP_EN	NOP1	NOP2	CNV_RDY_FL

Default = 8583h.

Bit 15 **OS: Operational status/single-shot conversion start**

This bit determines the operational status of the device.
This bit can only be written when in power-down mode.

For a write status:
0 : No effect
1 : Begin a single conversion (when in power-down mode)
For a read status:
0 : Device is currently performing a conversion
1 : Device is not currently performing a conversion

Bits[14:12] **MUX[2:0]: Input multiplexer configuration (ADS1118 only)**

These bits configure the input multiplexer. They serve no function on the ADS1116/4.

000 : AIN_P = AIN0 and AIN_N = AIN1 (default)
001 : AIN_P = AIN0 and AIN_N = AIN3
010 : AIN_P = AIN1 and AIN_N = AIN3
011 : AIN_P = AIN2 and AIN_N = AIN3
100 : AIN_P = AIN0 and AIN_N = GND
101 : AIN_P = AIN1 and AIN_N = GND
110 : AIN_P = AIN2 and AIN_N = GND
111 : AIN_P = AIN3 and AIN_N = GND

Bits[11:9] **PGA[2:0]: Programmable gain amplifier configuration (ADS1118 only)**

These bits configure the programmable gain amplifier. They serve no function on the ADS1116.

000 : FS = ±6.144V(1)
001 : FS = ±4.096V(1)
010 : FS = ±2.048V (default)
011 : FS = ±1.024V
100 : FS = ±0.512V
101 : FS = ±0.256V
110 : FS = ±0.256V
111 : FS = ±0.256V

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

Bit 8 **MODE: Device operating mode**

This bit controls the current operational mode of the ADS1116/8.
0 : Continuous conversion mode
1 : Power-down single-shot mode (default)

Bits[7:5] **DR[2:0]: Data rate**

These bits control the data rate setting.

000 : 8SPS	100 : 128SPS (default)
001 : 16SPS	101 : 250SPS
010 : 32SPS	110 : 475SPS
011 : 64SPS	111 : 860SPS

Bit 4 **TS_MODE: Temperature sensor mode (ADS1118 only)**

This bit configures the ADC to convert temperature or input signals. It should be left as '0' in the ADS1116.
0 : ADC mode (default)
1 : Temperature sensor mode

Bit 3 **PULL_UP_EN: Pull-up enable**

This bit enables a weak pull-up resistor on the DOUT pin. When enabled, a 400kΩ resistor connects the bus line to supply. When disabled, the DOUT pin floats.
0 : Pull-up resistor disabled on DOUT pin (default)
1 : Pull-up resistor enabled on DOUT pin

Bits[2:0] **NOP: No operation**

The NOP bits control whether data are written to the Configuration register or not. In order for data to be written to the Configuration register, the NOP bits must be written as '01'. Any other value written to the NOP bits results in a NOP command. This means that DIN can be held high or low during SCLK pulses without data being written to the Configuration register.
00 : Invalid data, do not update the contents of the Configuration register.
01 : Valid data, update the Configuration register (default)
10 : Invalid data, do not update the contents of the Configuration register.
11: Invalid data, do not update the contents of the Configuration register.

Bit 0 **CNV_RDY_FL: Conversion ready flag**

This bit is active low and indicates when data are ready from the converter. When it is high, a conversion is not yet ready and is in process. The purpose of the conversion ready flag bit is to return the DOUT pin line to a high state to prepare for the falling edge from new data.
0 : Data ready, no conversion in progress
1 : Data not ready, conversion in progress (default)

DATA RETRIEVAL

Data may be read in one of two modes: Single-Shot and Continuous Conversion mode. The mode is selected by writing to the OS bit in the Configuration Register.

Continuous Conversion Mode

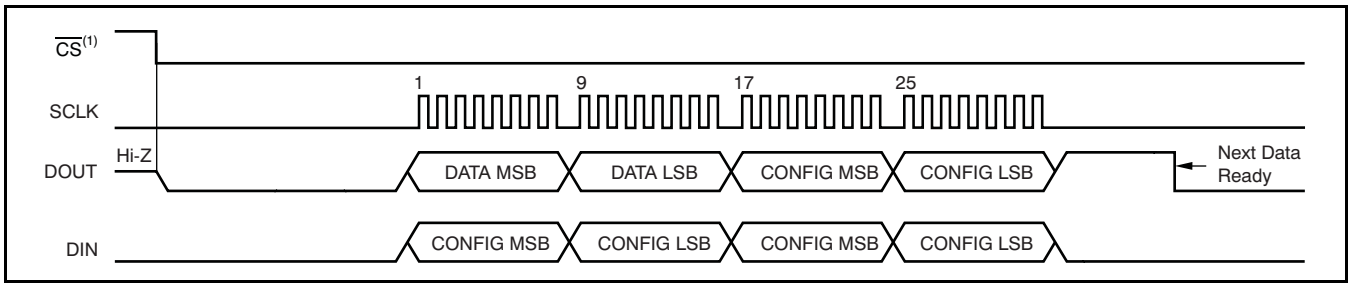
In Continuous Conversion mode, the conversion data are read from the device without an op code command. When DOUT asserts low (indicating that new conversion data are ready), the conversion data are read by shifting the data out on DOUT. The MSB of the data (bit 15) on DOUT is clocked out on the first rising edge of SCLK.

As shown in Figure 27, the data consist of two bytes for the conversion result and an additional two bytes for the Configuration Register readback. The data read operation must be completed $16/f_{CLK}$ cycles before DOUT asserts again.

One-Shot Mode

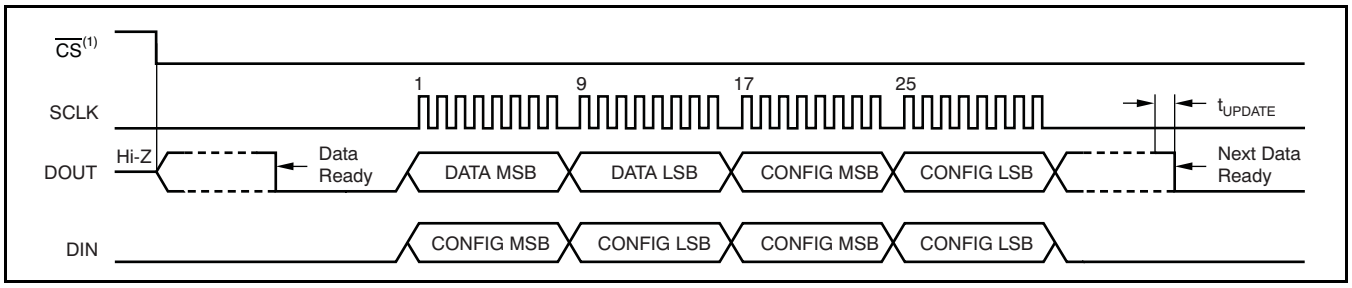
In One-Shot mode, the conversion data are buffered, holding the current data until new conversion data replace it. The conversion data are read by writing a '1' to the OS bit, followed by shifting the conversion data out.

The data consist of two bytes for the conversion result and two bytes for the Configuration Register; see Figure 28. As opposed to the Continuous Conversion mode, DOUT does not assert low.



(1) $\overline{CS}$ may be held low. If $\overline{CS}$ is low, DOUT asserts low.

Figure 27. Continuous Conversion Mode Timing



(1) $\overline{CS}$ may be held low.

Figure 28. One-Shot Mode Timing

PRODUCT PREVIEW

APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADS1116/8 in various situations.

BASIC CONNECTIONS

For many applications, connecting the ADS1116/8 is simple. A basic connection diagram for the ADS1118 is shown in Figure 29.

The fully differential voltage input of the ADS1116/8 is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADS1116/8 can read bipolar differential signals, these devices cannot accept negative voltages on either input. It may be helpful to think of the ADS1116/8 positive voltage input as *noninverting*, and of the negative input as *inverting.*

When the ADS1116/8 are converting data, they draw current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1116/8 interface directly to standard SPI controllers. Any microcontroller SPI peripheral can operate with the ADS1116/8.

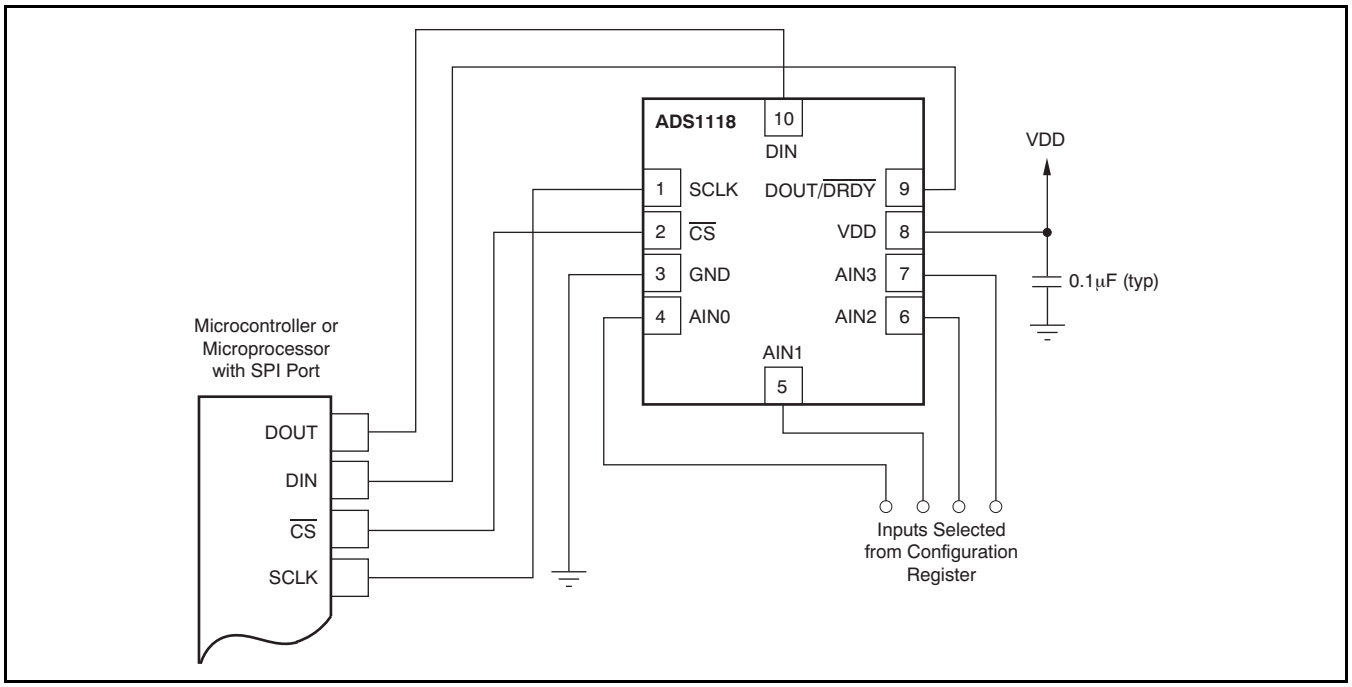


Figure 29. Typical Connections of the ADS1118

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CONNECTING MULTIPLE DEVICES

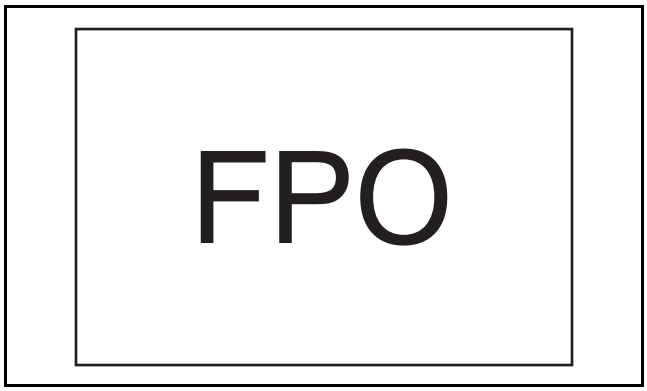
TBD

USING GPIO PORTS FOR COMMUNICATION

TBD

NOTE: ADS1116/8 power and input connections omitted for clarity.

Figure 30. Using GPIO with a Single ADS1118



NOTE: ADS1116/8 power and input connections omitted for clarity. The ADDR pin selects the SPI address.

Figure 31. Connecting Multiple ADS1116/8s

NOTE: ADS1116/8 power and input connections omitted for clarity. ADDR, A3, A2, A1, and A0 select the SPI addresses.

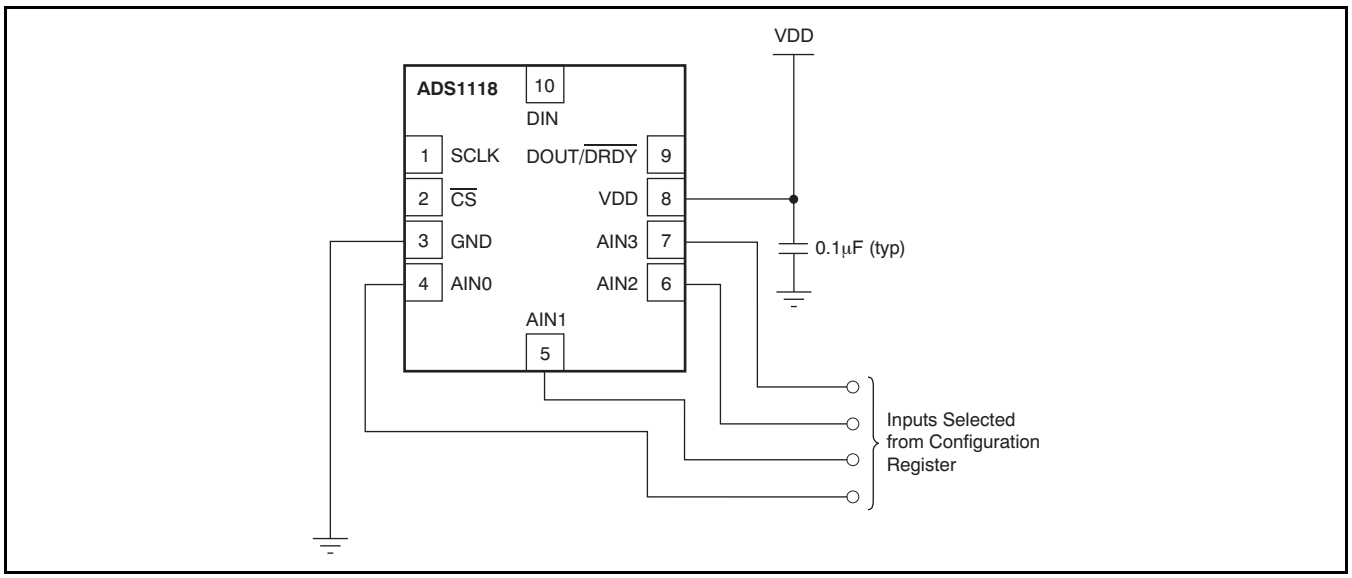
Figure 32. Connecting Multiple Device Types

PRODUCT PREVIEW

SINGLE-ENDED INPUTS

Although the ADS1118 has two differential inputs, the device can easily measure four single-ended signals. Figure 33 shows a single-ended connection scheme. The ADS1118 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection on the configuration register. The single-ended signal can range from 0V to supply. The ADS1118 loses no linearity anywhere within the input range. Negative voltages cannot be applied to this circuit because the ADS1118 can only accept positive voltages.

The ADS1118 input range is bipolar differential with respect to the reference. The single-ended circuit shown in Figure 33 covers only half the ADS1118 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.



NOTE: Digital and address pin connections omitted for clarity.

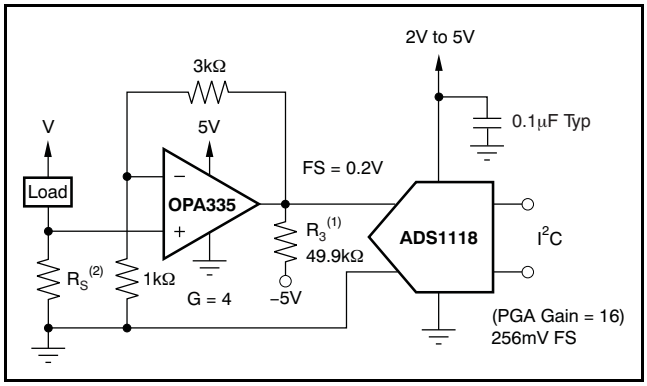
Figure 33. Measuring Single-Ended Inputs

PRODUCT PREVIEW

LOW-SIDE CURRENT MONITOR

Figure 34 shows a circuit for a low-side shunt-type current monitor. The circuit monitors the voltage across a shunt resistor, which is sized as small as possible while giving a measurable output voltage. This voltage is amplified by an OPA335 low-drift op amp, and the result is read by the ADS1118.

It is suggested that the ADS1118 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 16, the op amp should be set up to give a maximum output voltage no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1118 is 0.2V.



(1) Pull-down resistor to allow accurate swing to 0V.

(2) R_S is sized for a 50mV drop at full-scale current.

Figure 34. Low-Side Current Measurement

The ADS1116/8 are fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1116/8 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1116/8 analog inputs can withstand momentary currents as large as 100mA.

If the ADS1116/8 are driven by an op amp with high-voltage supplies (such as ±12V), protection should be provided, even if the op amp is configured so that it does not output out-of-range voltages. Many op amps drift to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1116/8. This incremental damage results in slow, long-term failure, which can be disastrous for permanently installed, low-maintenance systems.

If an op amp or other front-end circuitry is used with an ADS1116/8, performance characteristics must be taken into account when designing the application.

TEXAS INSTRUMENTS

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
ADS1118IDGSR	PREVIEW	MSOP	DGS	10		TBD	Call TI	Call TI
ADS1118IDGST	PREVIEW	MSOP	DGS	10		TBD	Call TI	Call TI
ADS1118IRUGR	PREVIEW	X2QFN	RUG	10		TBD	Call TI	Call TI
ADS1118IRUGT	PREVIEW	X2QFN	RUG	10		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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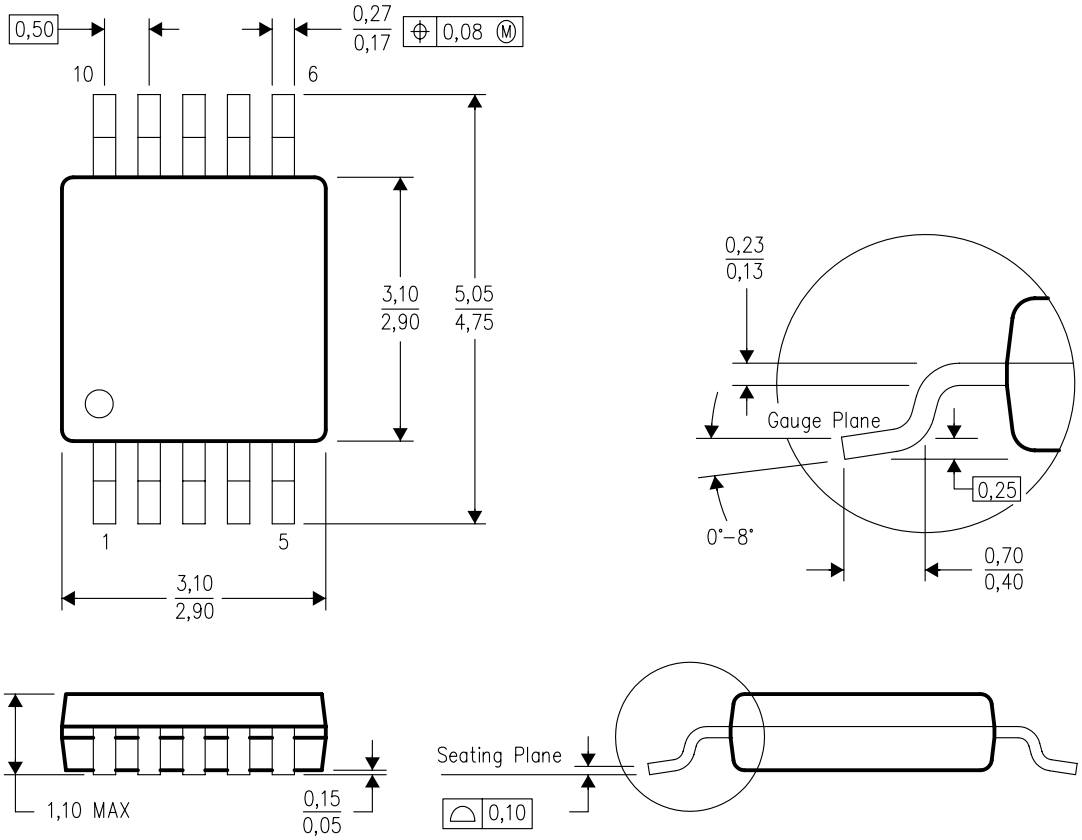
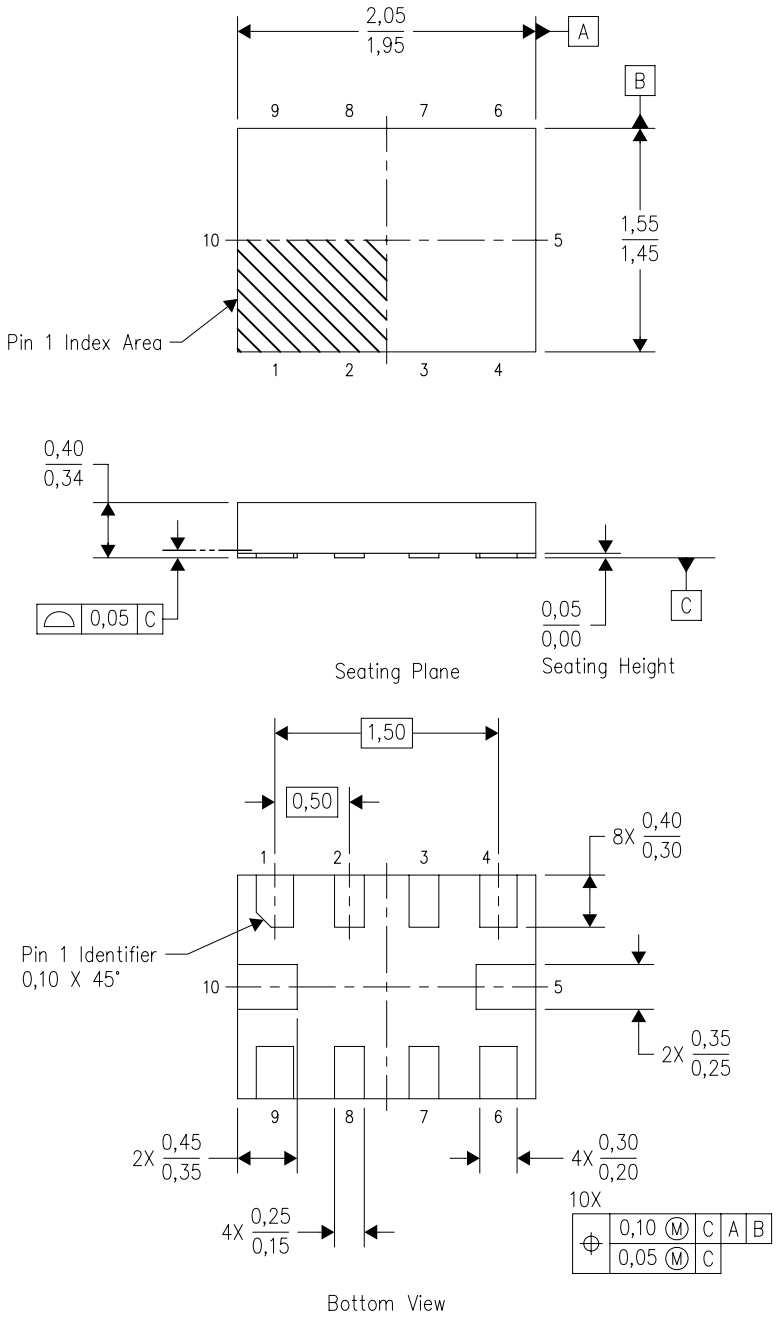
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

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