

INTERNATIONAL RECTIFIER



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REPETITIVE AVALANCHE AND dv/dt RATED

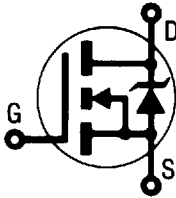
HEXFET® TRANSISTORS IRHM7250

IRHM8250

2N7269

JANSR2N7269

JANSH2N7269



N-CHANNEL

MEGA RAD HARD

200 Volt, 0.100Ω, MEGA RAD HARD HEXFET

International Rectifier's MEGA RAD HARD Technology HEXFETs demonstrate excellent threshold voltage stability and breakdown voltage stability at total radiation doses as high as 1×10^6 Rads (Si). Under **identical** pre and post radiation test conditions, International Rectifier's RAD HARD HEXFETs retain **identical** electrical specifications up to 1×10^5 Rads (Si) total dose. At 1×10^6 Rads (Si) total dose, under the same pre-dose test conditions, only minor shifts in the electrical specifications are observed and are so specified in table 1. No compensation in gate drive circuitry required! In addition, these devices are capable of surviving transient ionization pulses as high as 1×10^{12} Rads (Si)/Sec, and return to normal operation within a few microseconds. Single Event Effect (SEE) testing of International Rectifier RAD HARD HEXFETs has demonstrated virtual immunity to SEE failure. Since the MEGA RAD process utilizes International Rectifier's patented HEXFET technology, the user can expect the highest quality and reliability in the industry.

RAD HARD HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits in space and weapons environments.

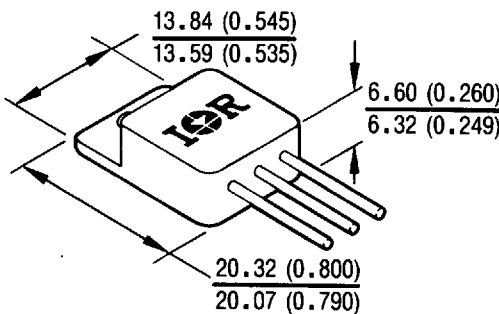
Product Summary

Part Number	V_{DSS}	$R_{DS(on)}$	I_D
IRHM7250	200V	0.100Ω	26A
IRHM8250	200V	0.100Ω	26A

FEATURES:

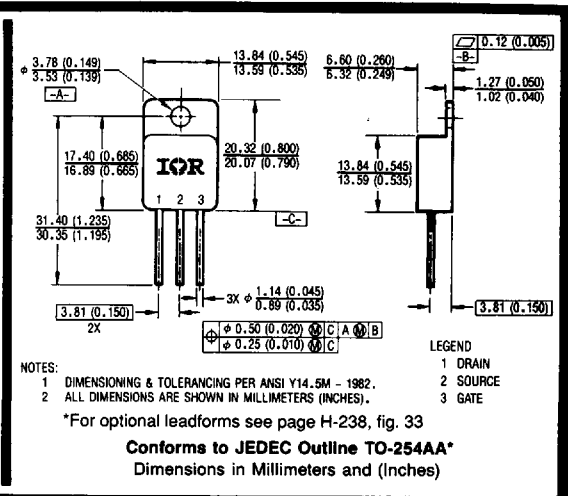
- Radiation Hardened up to 1×10^6 Rads (Si)
- Single Event Burnout (SEB) Hardened
- Single Event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-Ray) Hardened
- Neutron Tolerant
- Identical Pre and Post Electrical Test Conditions
- Repetitive Avalanche Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets

CASE STYLE AND DIMENSIONS



CAUTION

**BERYLLIA WARNING PER MIL-S-19500
SEE PAGE H-238**



Absolute Maximum Ratings ①

Parameter	IRHM7250, IRHM8250	Units
I_D @ $V_{GS} = 12V$, $T_C = 25^\circ C$	Continuous Drain Current	26
I_D @ $V_{GS} = 12V$, $T_C = 100^\circ C$	Continuous Drain Current	16
I_{DM}	Pulsed Drain Current ②	104
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	150
	Linear Derating Factor	1.2
V_{GS}	Gate-to-Source Voltage	± 20
E_{AS}	Single Pulse Avalanche Energy ③	500 (See Fig. 29)
I_{AR}	Avalanche Current ②	26 (See E_{AR})
E_{AR}	Repetitive Avalanche Energy ②	15 (See Fig. 30)
dv/dt	Peak Diode Recovery dv/dt ④	5.0 (See Fig. 30)
T_J	Operating Junction	-55 to 150
T_{STG}	Storage Temperature Range	
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)
	Weight	9.3 (typical)

Electrical Characteristics @ $T_J = 25^\circ C$ (Unless Otherwise Specified) ①

Parameter	Min.	Typ.	Max.	Units	Test Conditions ①
BV_{DSS}	200	—	—	V	$V_{GS} = 0V$, $I_D = 1.0$ mA
$\Delta BV_{DSS}/\Delta T_J$	—	0.27	—	V/ $^\circ C$	Reference to $25^\circ C$, $I_D = 1.0$ mA
$R_{DS(on)}$	—	—	0.100	Ω	$V_{GS} = 12V$, $I_D = 16A$ ⑤
	—	—	0.105		$V_{GS} = 12V$, $I_D = 26A$
$V_{GS(th)}$	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0$ mA
g_{fs}	8.0	—	—	S/(V)	$V_{DS} \geq 15V$, $I_{DS} = 16A$ ⑤
I_{DSS}	—	—	25	μA	$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$
	—	—	250		$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$, $T_J = 125^\circ C$
I_{GSS}	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	—	—	-100		$V_{GS} = -20V$
Q_g	—	—	170	nC	$V_{GS} = 12V$, $I_D = 26A$
Q_{gs}	—	—	30		$V_{DS} = 0.5 \times \text{Max. Rating}$
Q_{gd}	—	—	60		See Fig. 23 and 31
$t_d(on)$	—	—	33	ns	$V_{DD} = 100V$, $I_D = 26A$, $R_G = 2.35\Omega$
t_r	—	—	140		
$t_d(off)$	—	—	140		See Fig. 28
t_f	—	—	140		
L_D	—	8.7	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	—	8.7	—		Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	—	4700	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$
C_{oss}	—	850	—		$f = 1.0$ MHz
C_{rss}	—	210	—		See Fig. 22

Source-Drain Diode Ratings and Characteristics ①

Parameter	Min.	Typ.	Max.	Units	Test Conditions ①
I_S	—	—	26	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	—	—	104		
V_{SD}	—	—	1.9	V	$T_J = 25^\circ C$, $I_S = 26A$, $V_{GS} = 0V$ ⑤
t_{rr}	—	—	820	ns	$T_J = 25^\circ C$, $I_F = 26A$, $di/dt \leq 100$ A/ μs ⑤
Q_{RR}	—	—	12	μC	$V_{DD} \leq 50V$
t_{on}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
R_{thJC}	—	—	0.83	K/W ⑥
R_{thJA}	—	—	48	
R_{thCS}	—	0.21	—	

Typical socket mount

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Radiation Performance of Rad Hard HEXFET's

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier uses two radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019. International Rectifier has imposed a standard gate voltage of 12 volts per note 7 and figure 8a and a V_{DSS} bias condition equal to 80% of the device rated voltage per note 8 and figure 8b. Pre and Post radiation limits of the devices irradiated to 1x10⁵ Rads (Si) are identical and are presented in table 1, column 1, IRHM7250. Device performance limits at a post radiation level of 1x10⁶ Rads (Si) are presented in Table 1, column 2, IRHM8250. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Typical delta curves showing radiation response appear in Figures 1 through 5. Typical post radiation curves appear in Figures 10 through 17.

Both pre and post radiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison. It should be noted that at a radiation level of 1x10⁵ Rads (Si), no change in limits are specified in DC parameters. At a radiation level of 1x10⁶ Rads (Si), leakage remains low and the device is usable with no change in drive circuitry required.

High dose rate testing may be done on a special request basis, using a dose rate up to 1x10¹² Rads (Si)/Sec. Photocurrent and transient voltage waveforms are shown in Figure 7, and the recommended test circuit to be used is shown in figure 9.

International Rectifier radiation hardened HEXFETs have been characterized in Neutron and heavy ion Single Event Effects (SEE) environments. The effects on bulk silicon of the type used by International Rectifier on RAD HARD HEXFETs are shown in figure 6. Single Event Effects characterization is shown in Table 3.

Table 1. Low Dose Rate ⑦ ⑧

Parameter	IRHM7250		IRHM8250		Units	Test Conditions ⑪
	100K Rads (Si) min.	max.	1000K Rads (Si) min.	max.		
B _V DSS Drain-to-Source Breakdown Voltage	200	—	200	—	V	V _{GS} = 0V, I _D = 1.0 mA
V _{GS(th)} Gate Threshold Voltage ⑤	2.0	4.0	1.25	4.5	V	V _{GS} = V _{DS} , I _D = 1.0 mA
I _{GSS} Gate-to-source Leakage Forward	—	100	—	100	nA	V _{GS} = +20V
I _{GSS} Gate-to-Source Leakage Reverse	—	-100	—	-100	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	—	25	—	50	μA	V _{DS} = 0.8 x Max Rating, V _{GS} = 0
R _{DS(on)1} Static Drain-to-Source On-State Resistance One	—	0.100	—	0.155	Ω	V _{GS} = 12V, I _D = 16A
V _{SD} Diode Forward Voltage ⑤	—	1.9	—	1.9	V	T _C = 25°C, I _S = 26A, V _{GS} = 0V

Table 2. High Dose Rate ⑨

Parameter	10 ¹¹ Rads (Si)/sec			10 ¹² Rads (Si)/sec			Units	Test Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
V _{DSS} Drain-to-Source Voltage	—	—	160	—	—	160	V	Applied drain-to-source voltage during gamma-dot
I _{PP}	—	15	—	—	15	—	A	Peak radiation induced photo-current
di/dt	—	—	160	—	—	8.0	A/μsec	Rate of rise of photo-current
L ₁	1.0	—	—	20	—	—	μH	Circuit inductance required to limit di/dt

Table 3. Single Event Effects

Parameter	Typ	Units	Ion	LET (Si) (MeV/mg/cm ²)	Range (μm)	V _{DS} Bias (V)	V _{GS} Bias (V)
V _{DS} ⑩	200	V	Ni	28	~ 41	200	-5

① See Figures 18 through 31 for pre-radiation curves.

② Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 26) Refer to Current HEXFET reliability report

③ @ V_{DD} = 25V, Starting T_J = 25°C, L = 1.9 mH, R_G = 25Ω, Peak I_L = 26A

④ I_{SD} ≤ 26A, di/dt ≤ 190 A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C Suggested R_G = 2.35Ω

⑤ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑥ K/W = °C/W
W/K = W/°C

⑦ Total Dose Irradiation with V_{GS} Bias. +12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019. (See figure 8a)

⑧ Total Dose Irradiation with V_{DS} Bias. V_{DS} = 0.8 rated BV_{DSS} (pre-radiation) applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019. (See figure 8b)

⑨ This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 Mev), 30 nsec pulse. See figure 9.

⑩ Study sponsored by NASA. Evaluation performed at Brookhaven National Labs.

⑪ All Pre-Radiation and Post-Radiation test conditions are identical to facilitate direct comparison for circuit applications.

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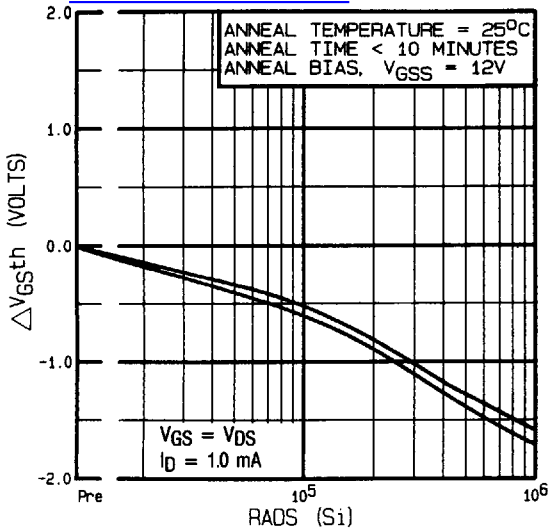


Fig. 1 — Typical Response of Gate Threshold Voltage Vs. Total Dose Exposure

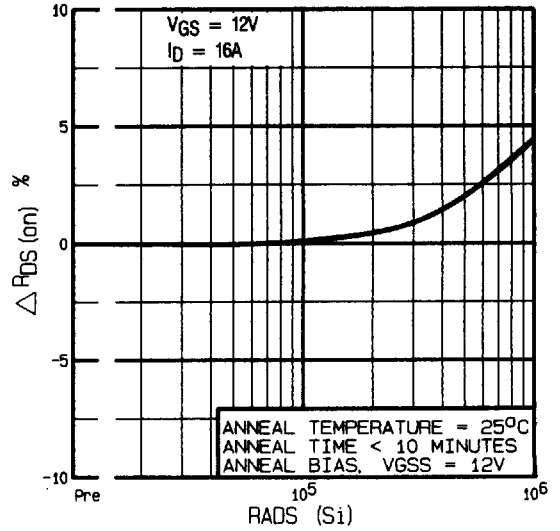


Fig. 2 — Typical Response of On-State Resistance Vs. Total Dose Exposure

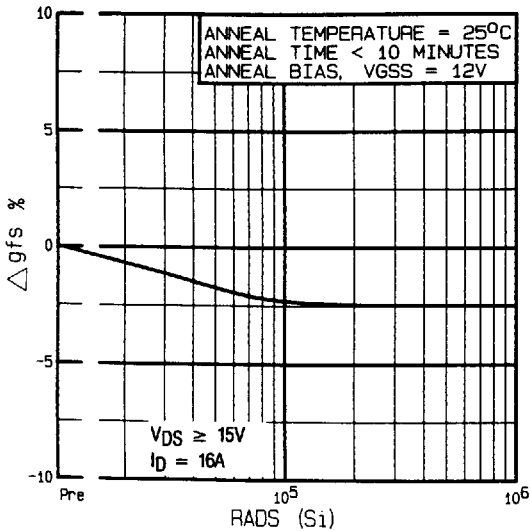


Fig. 3 — Typical Response of Transconductance Vs. Total Dose Exposure

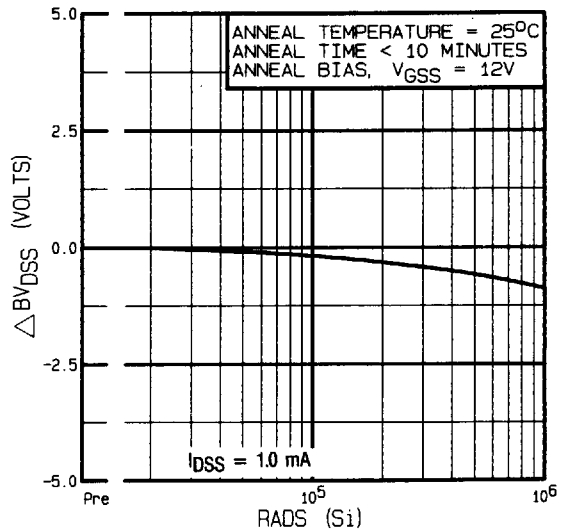


Fig. 4 — Typical Response of Drain-to-Source Breakdown Vs. Total Dose Exposure

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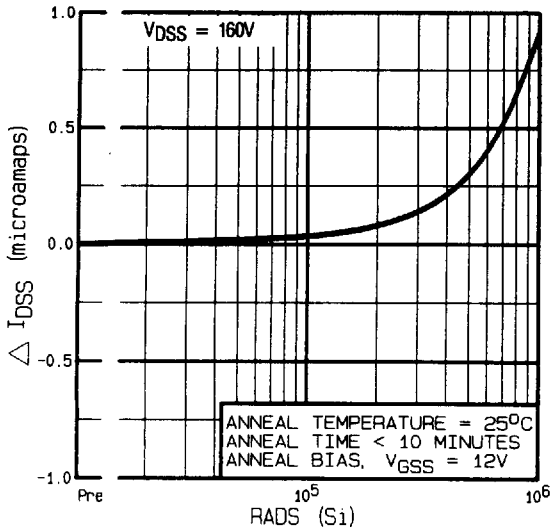


Fig. 5 — Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

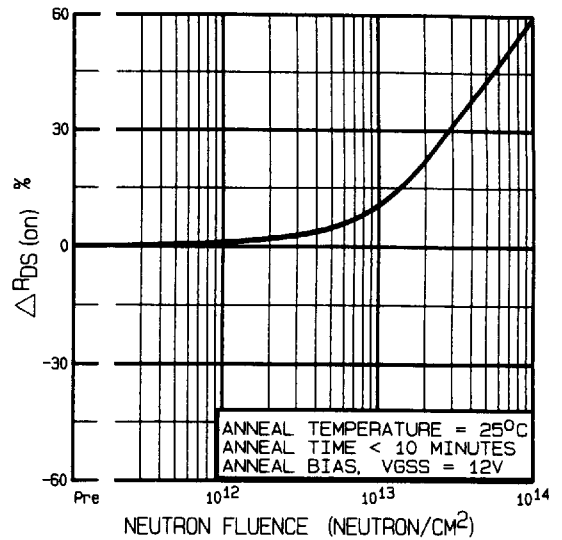


Fig. 6 — Typical On-State Resistance Vs. Neutron Fluence Level

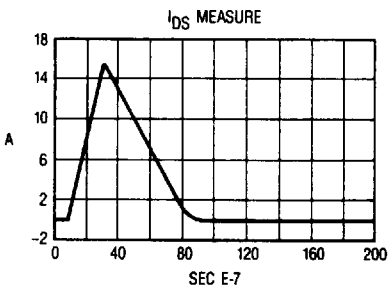
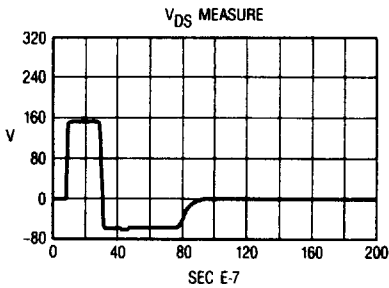


Fig. 7 — Typical Transient Response of Rad Hard HEXFET During 1×10^{12} Rad (Se)/Sec Exposure

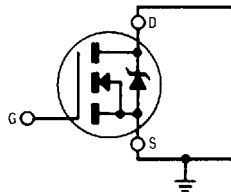


Fig. 8a — Gate Stress of V_{GSS} Equals 12 Volts During Radiation

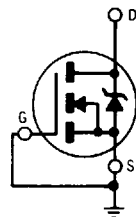


Fig. 8B — V_{DSS} Stress Equals 80% of B_{VDSS} During Radiation

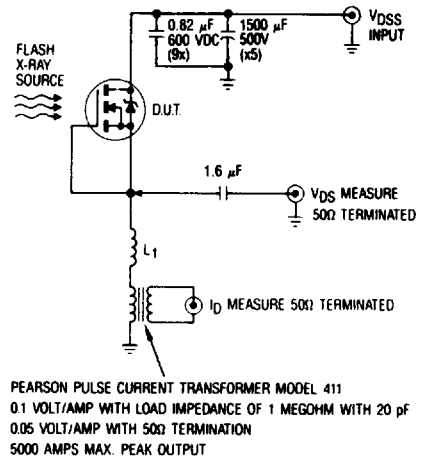


Fig. 9 — High Dose Rate (Gamma Dot) Test Circuit

Note: Bias Conditions during radiation; $V_{GS} = 12\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$

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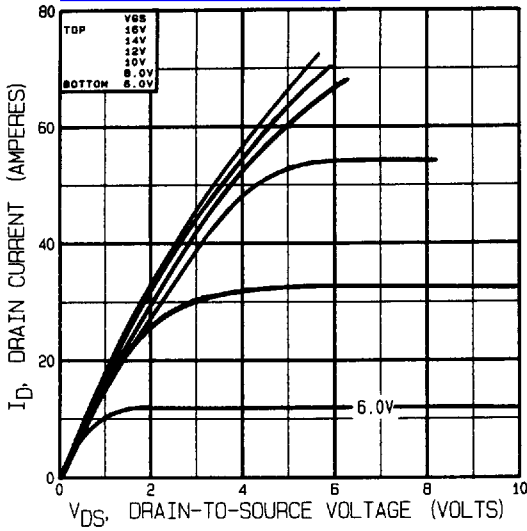


Fig. 10 — Typical Output Characteristics Pre-Radiation

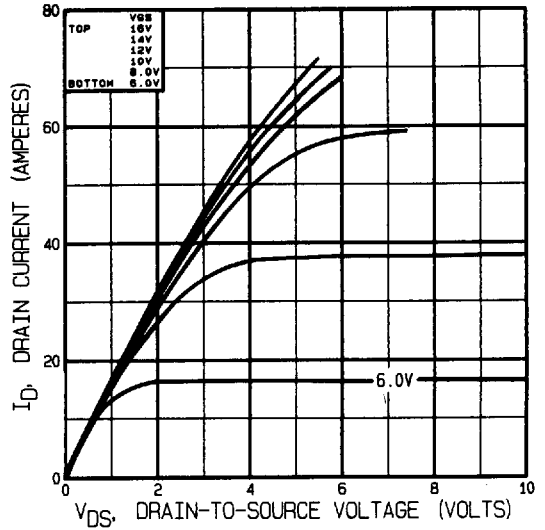


Fig. 11 — Typical Output Characteristics Post-Radiation 100K Rads (Si)

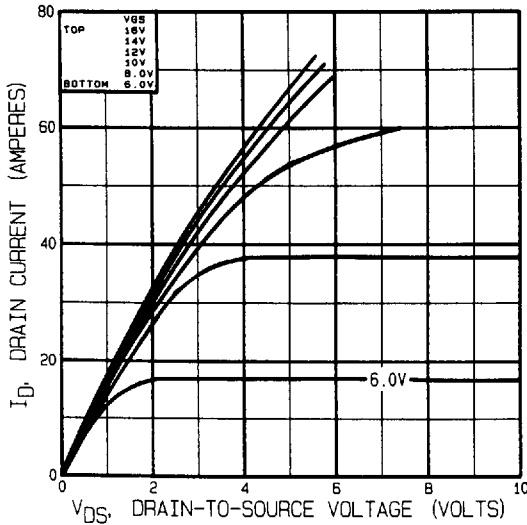


Fig. 12 — Typical Output Characteristics Post-Radiation 300K Rads (Si)

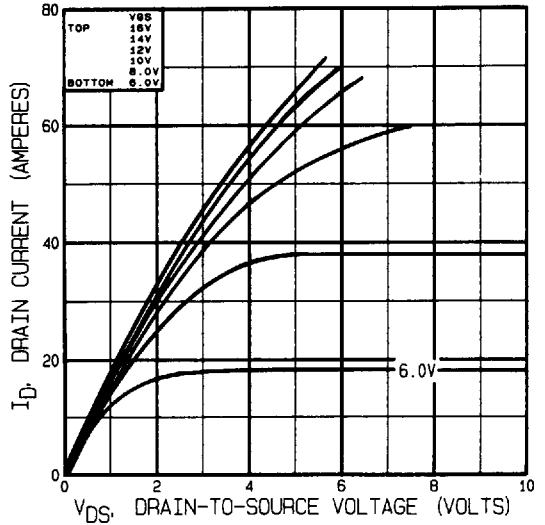


Fig. 13 — Typical Output Characteristics Post-Radiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation; $V_{GS} = 0$ Vdc, $V_{DS} = 160$ Vdc

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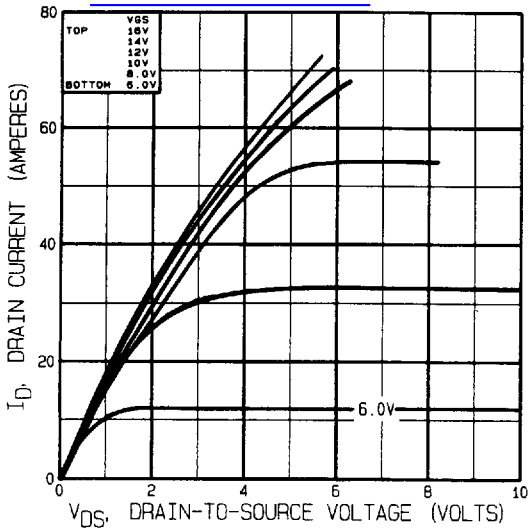


Fig. 14 — Typical Output Characteristics
Pre-Radiation

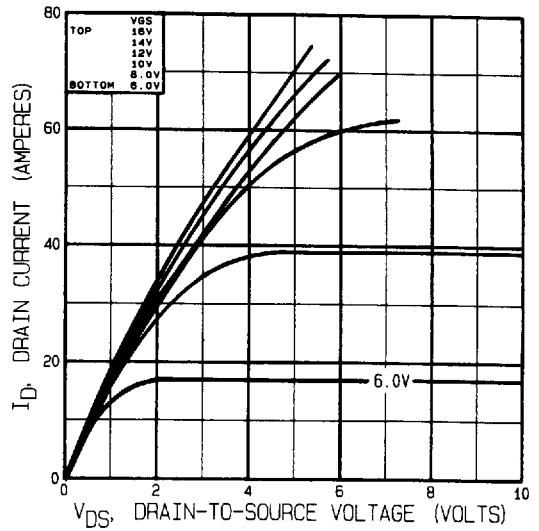


Fig. 15 — Typical Output Characteristics
Post-Radiation 100K Rads (Si)

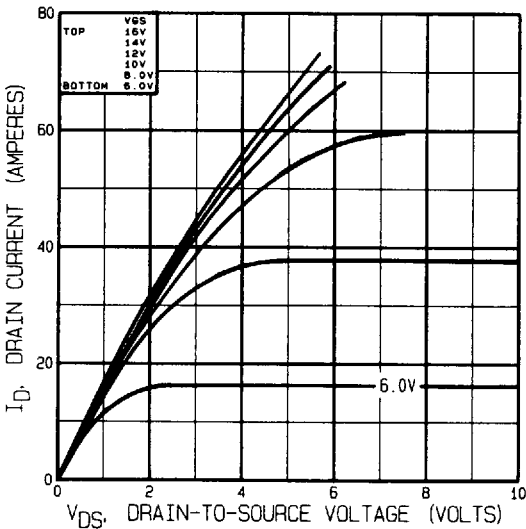


Fig. 16 — Typical Output Characteristics
Post-Radiation 300K Rads (Si)

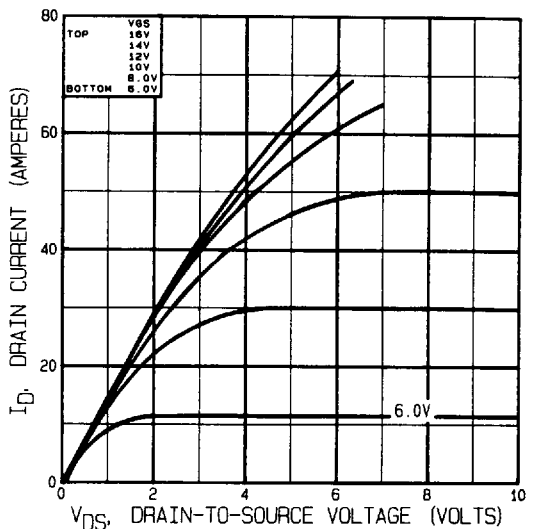


Fig. 17 — Typical Output Characteristics
Post-Radiation 1 Mega Rads (Si)

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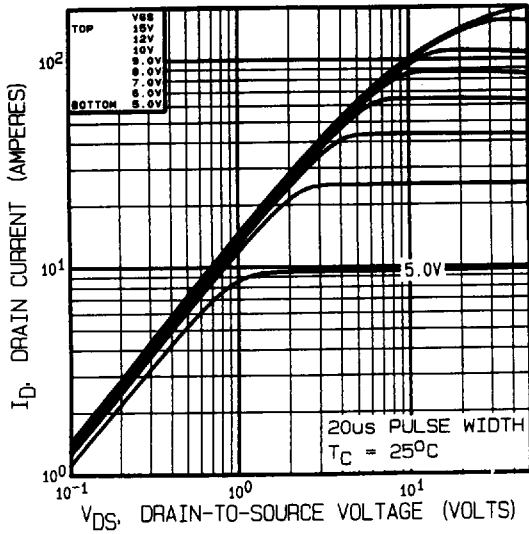


Fig. 18 — Typical Output Characteristics, $T_C = 25^\circ\text{C}$

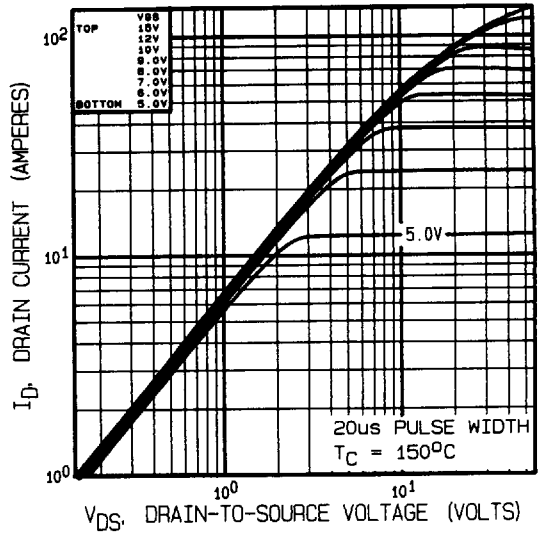


Fig. 19 — Typical Output Characteristics, $T_C = 150^\circ\text{C}$

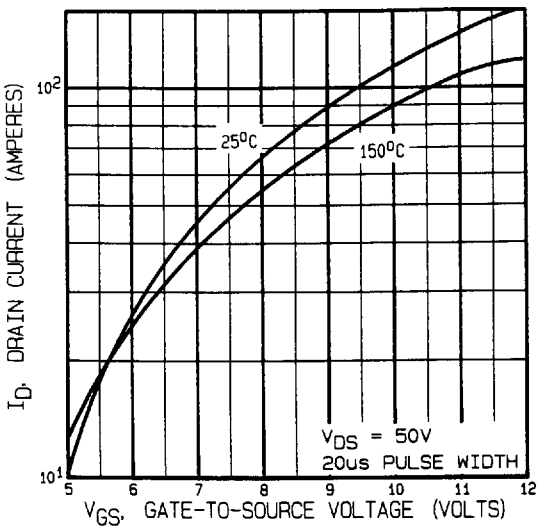


Fig. 20 — Typical Transfer Characteristics

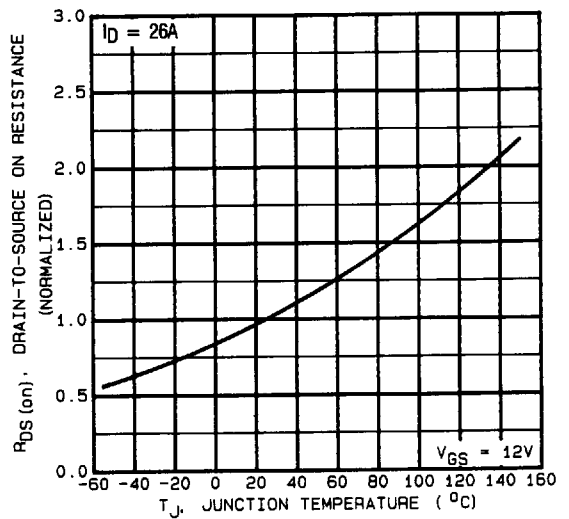


Fig. 21 — Normalized On-Resistance Vs. Temperature

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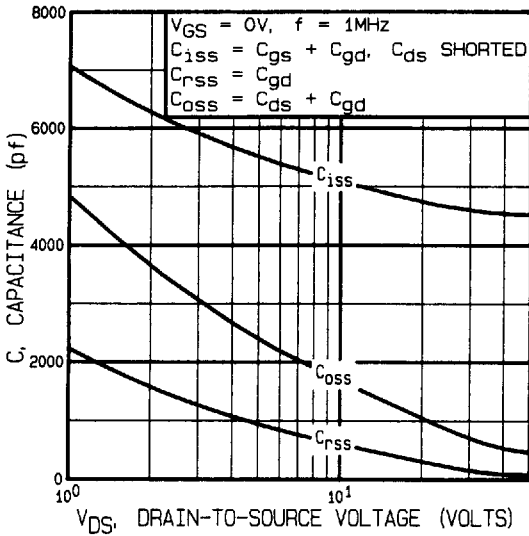


Fig. 22 — Typical Capacitance Vs. Drain-to-Source Voltage

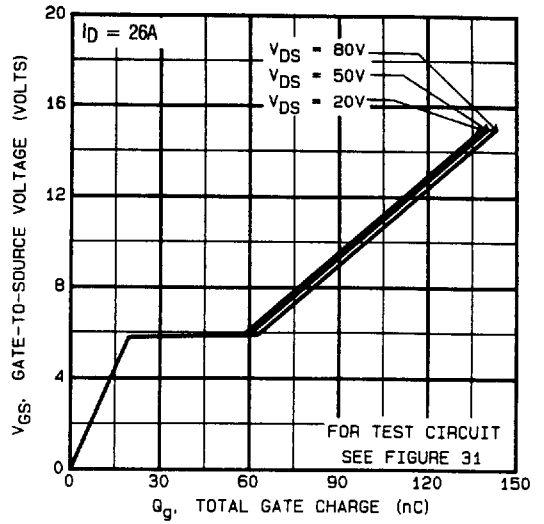


Fig. 23 — Typical Gate Charge Vs. Gate-to-Source Voltage

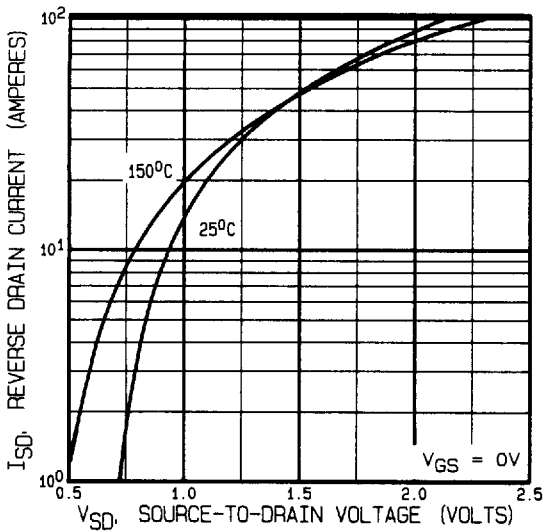


Fig. 24 — Typical Source-Drain Diode Forward Voltage

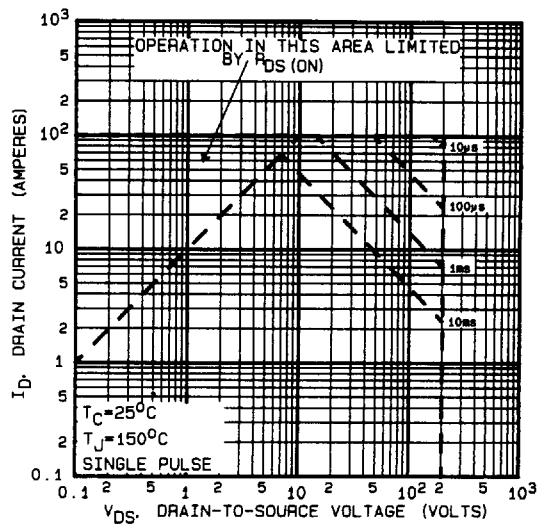


Fig. 25 — Maximum Safe Operating Area



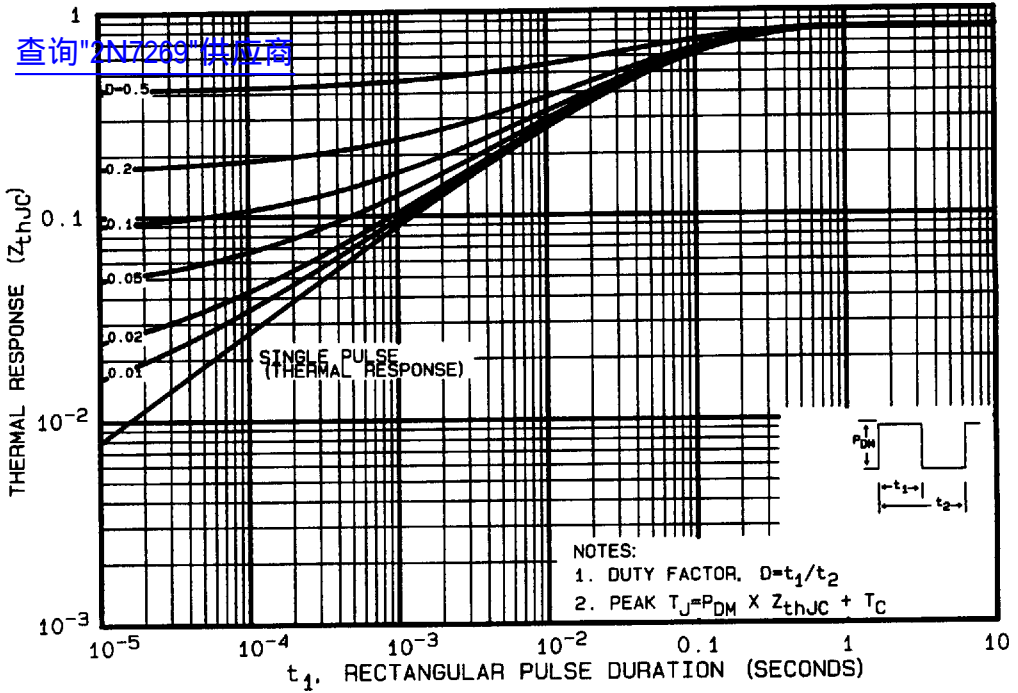


Fig. 26 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

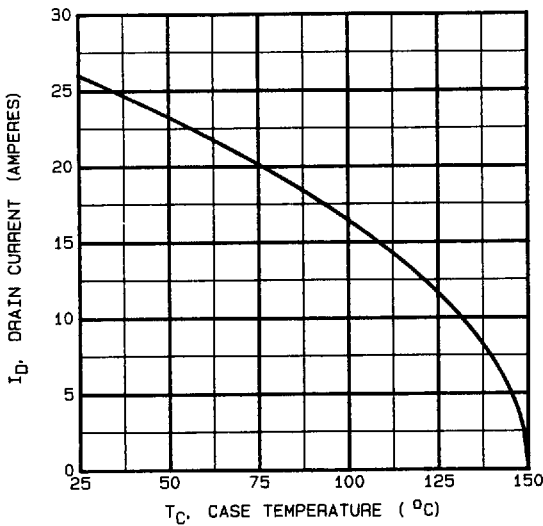


Fig. 27 — Maximum Drain Current Vs. Case Temperature

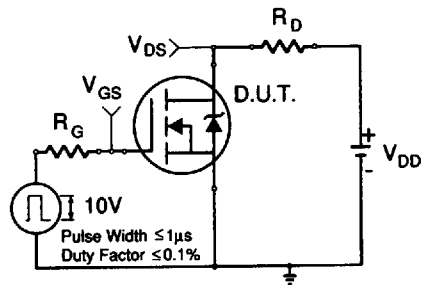


Fig. 28a — Switching Time Test Circuit

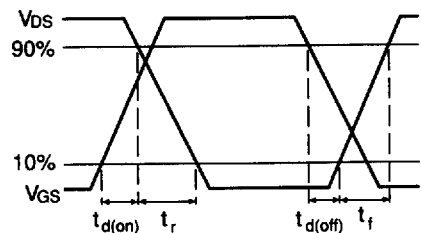


Fig. 28b — Switching Time Waveforms

Pre-Radiation

IRHM7250, IRHM8250, JANSR-, JANSH-, 2N7269 Devices

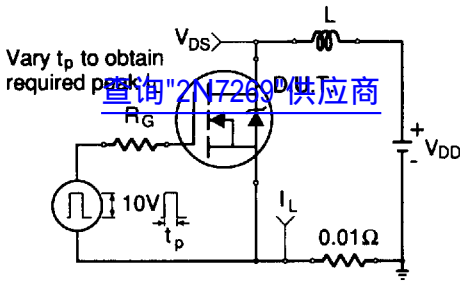


Fig. 29a — Unclamped Inductive Test Circuit

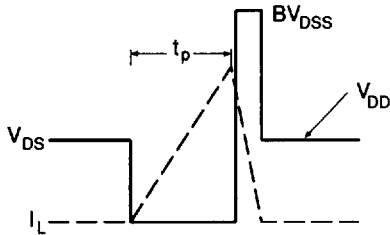


Fig. 29b — Unclamped Inductive Waveforms

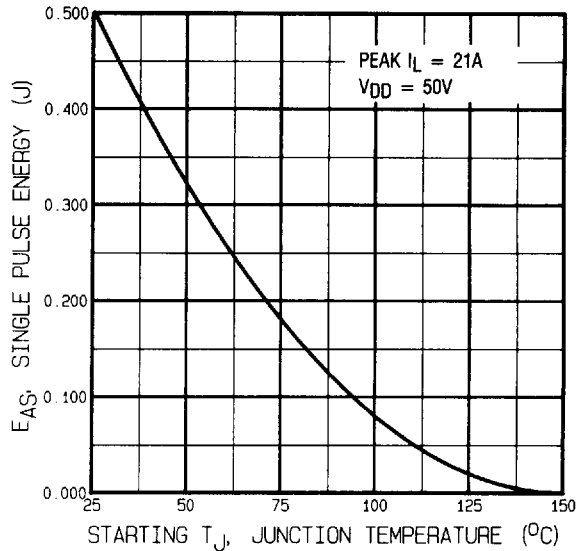


Fig. 29c — Maximum Avalanche Energy Vs. Starting Junction Temperature

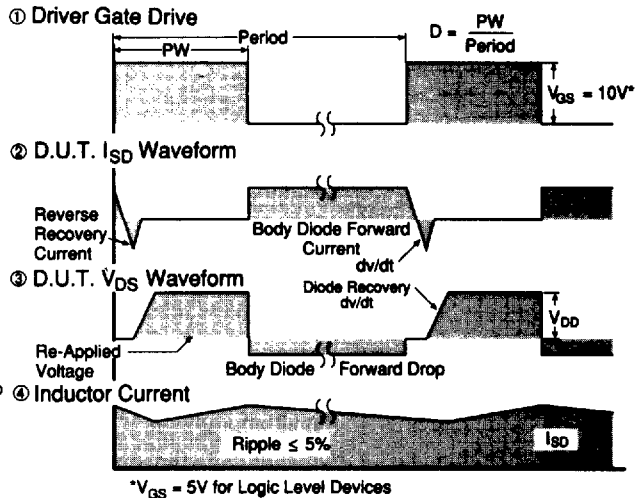
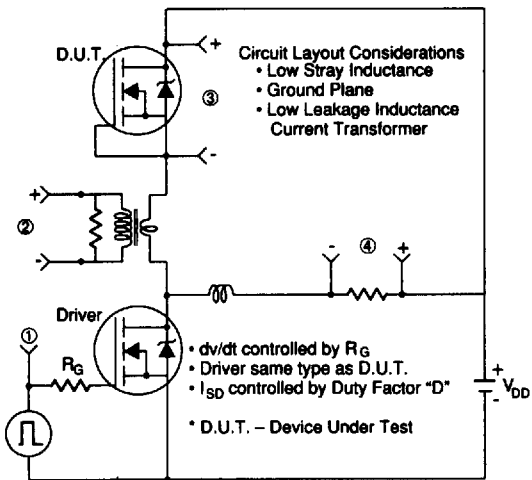


Fig. 30. — Peak Diode Recovery dv/dt Test Circuit

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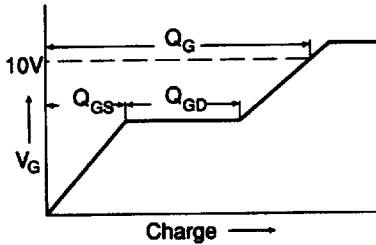


Fig. 31a — Basic Gate Charge Waveform

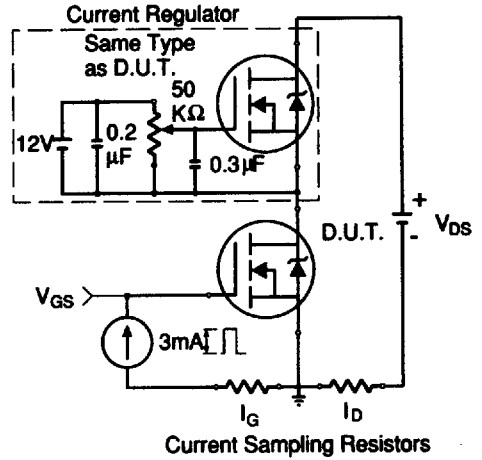


Fig. 31b — Gate Charge Test Circuit

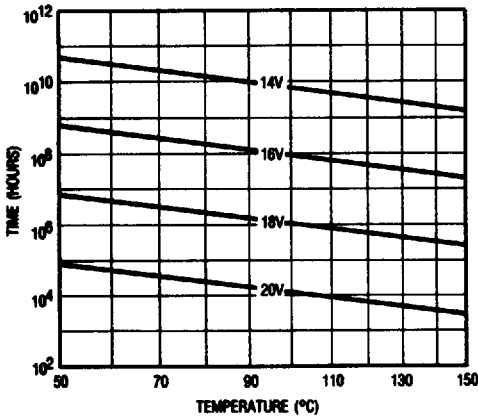


Fig. 32 — Typical Time to Accumulated 1% Failure

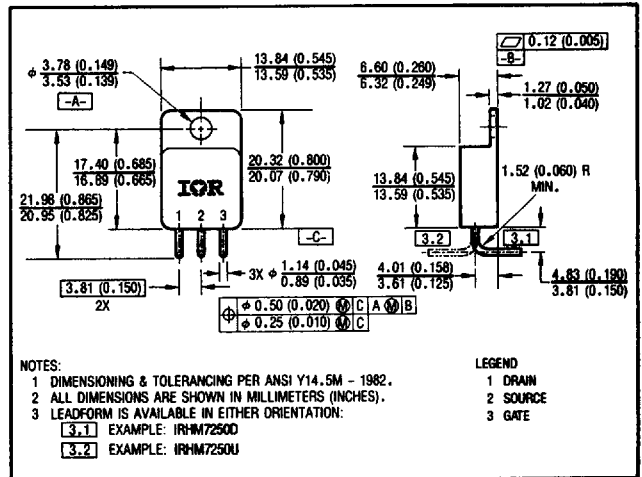


Fig. 33 — Optional Leadforms for Outline TO-254

BERYLLIA WARNING PER MIL-S-19500

Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.