MC14014B, MC14021B

8-Bit Static Shift Register

The MC14014B and MC14021B 8−bit static shift registers are constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel−to−serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

Features

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- “Q” Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin−for−Pin Replacement for CD4014B
- MC14021B Pin−for−Pin Replacement for CD4021B
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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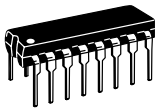
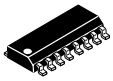
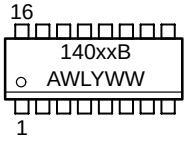
MARKING DIAGRAMS

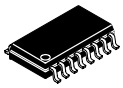


PDIP−16
P SUFFIX
CASE 648

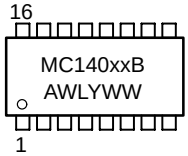


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

TRUTH TABLE

SERIAL OPERATION:

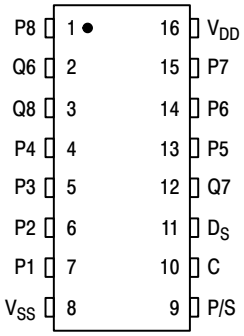
t	Clock	D_S	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n	↗	0	0	0	?	?
n+1	↗	1	0	1	0	?
n+2	↗	0	0	0	1	0
n+3	↗	1	0	1	0	1
	↘	X	0	Q6	Q7	Q8

PARALLEL OPERATION:

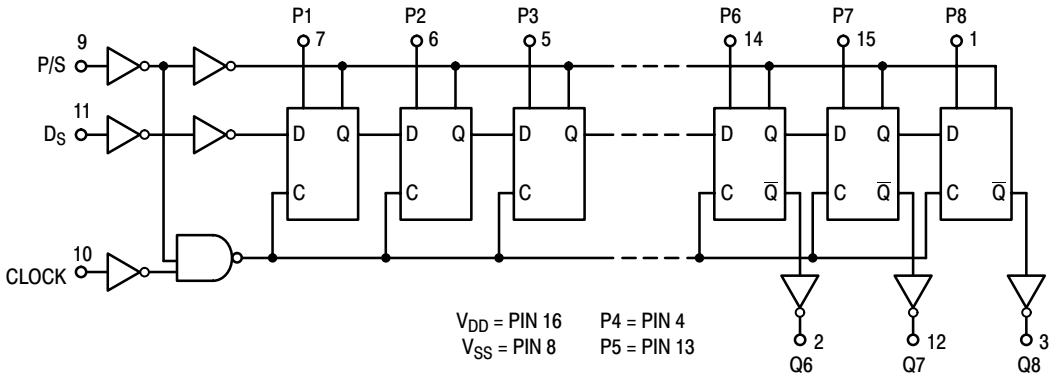
Clock					
MC14014B	MC14021B	D_S	P/S	P_n	$*Q_n$
↗	X	X	1	0	0
↗	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

PIN ASSIGNMENT



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	−	1.5	−	2.25	1.5	−	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	−	3.0	−	4.50	3.0	−	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	−	4.0	−	6.75	4.0	−	4.0	
(V_O = 0.5 or 4.5 Vdc)	"1" Level	V_{IH}	5.0	3.5	−	3.5	2.75	−	3.5	−	Vdc
(V_O = 1.0 or 9.0 Vdc)			10	7.0	−	7.0	5.50	−	7.0	−	
(V_O = 1.5 or 13.5 Vdc)			15	11	−	11	8.25	−	11	−	
Output Drive Current		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	− 3.0	−	− 2.4	− 4.2	−	− 1.7	−	
(V_{OH} = 4.6 Vdc)			5.0	− 0.64	−	− 0.51	− 0.88	−	− 0.36	−	
(V_{OH} = 9.5 Vdc)			10	− 1.6	−	− 1.3	− 2.25	−	− 0.9	−	
(V_{OH} = 13.5 Vdc)			15	− 4.2	−	− 3.4	− 8.8	−	− 2.4	−	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	−	0.51	0.88	−	0.36	−	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	−	1.3	2.25	−	0.9	−	
(V_{OL} = 1.5 Vdc)			15	4.2	−	3.4	8.8	−	2.4	−	
Input Current		I_{in}	15	−	± 0.1	−	±0.00001	± 0.1	−	± 1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	− − −	5.0 10 15	− − −	0.005 0.010 0.015	5.0 10 15	− − −	150 300 600	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.75 μA/kHz) f + I_{DD} I_T = (1.50 μA/kHz) f + I_{DD} I_T = (2.25 μA/kHz) f + I_{DD}							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

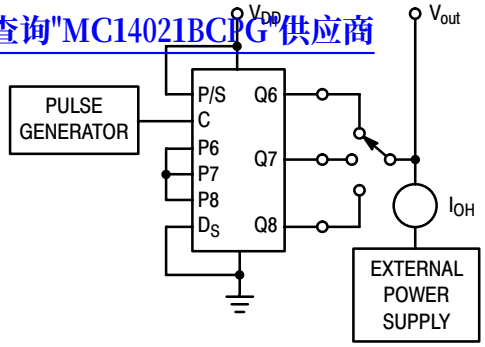
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.0015.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Propagation Delay Time (Clock to Q, P/S to Q) t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 90 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 – – –	 400 170 115	 800 340 230	ns
Clock Pulse Width	t_{WH}	5.0 10 15	400 175 135	150 75 40	– – –	ns
Clock Frequency	f_{cl}	5.0 10 15	– – –	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Parallel/Serial Control Pulse Width	t_{WH}	5.0 10 15	400 175 135	150 75 40	– – –	ns
Setup Time P/S to Clock	t_{su}	5.0 10 15	200 100 80	100 50 40	– – –	ns
Hold Time Clock to P/S	t_h	5.0 10 15	20 20 25	– 2.5 – 10 0	– – –	ns
Setup Time Data (Parallel or Serial) to Clock or P/S	t_{su}	5.0 10 15	350 80 60	150 50 30	– – –	ns
Hold Time Clock to D_S	t_h	5.0 10 15	45 35 35	0 0 5	– – –	ns
Hold Time Clock to P_n	t_h	5.0 10 15	50 45 45	25 20 20	– – –	ns
Input Clock Rise Time	$t_{r(cl)}$	5.0 10 15	– – –	– – –	15 5 4	μs

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Preset output under test to a logic “1” level.

Figure 1. Output Source Current Test Circuit

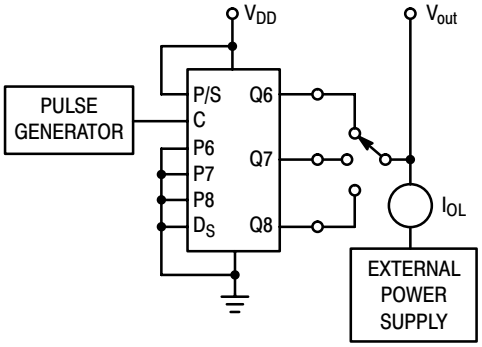


Figure 2. Output Sink Current Test Circuit

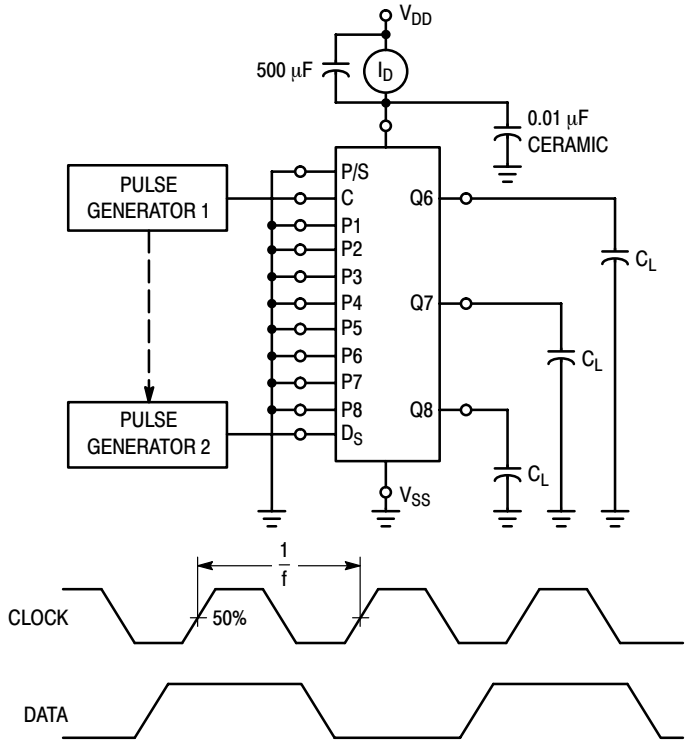


Figure 3. Power Dissipation Test Circuit and Waveform

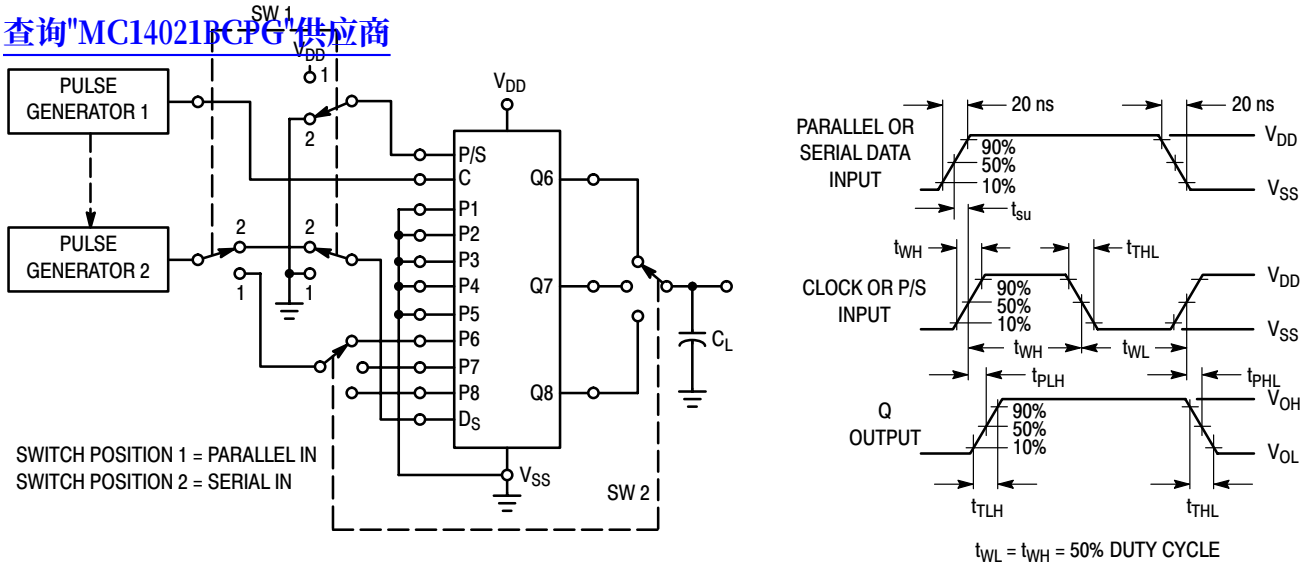


Figure 4. Switching Time Test Circuit and Waveforms

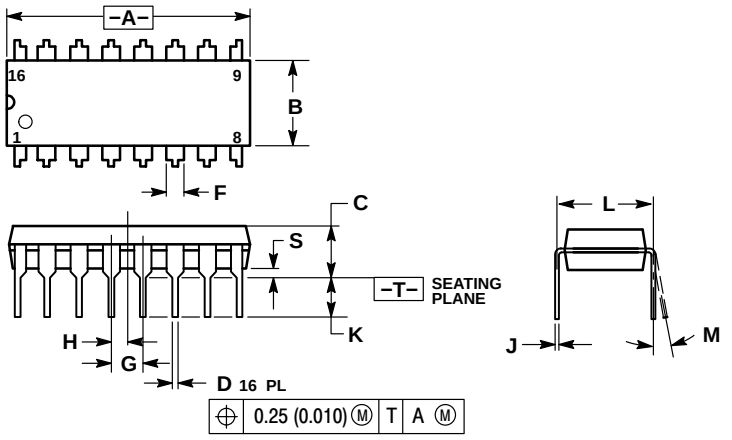
ORDERING INFORMATION

Device	Package	Shipping†
MC14014BCP	PDIP−16	500 Units / Rail
MC14014BCPG	PDIP−16 (Pb−Free)	500 Units / Rail
MC14014BD	SOIC−16	48 Units / Rail
MC14014BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14014BDR2	SOIC−16	2500 Units / Tape & Reel
MC14014BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
MC14014BF	SOEIAJ−16	50 Units / Rail
MC14014BFEL	SOEIAJ−16	2000 Units / Tape & Reel
MC14021BCP	PDIP−16	500 Units / Rail
MC14021BCPG	PDIP−16 (Pb−Free)	500 Units / Rail
MC14021BD	SOIC−16	48 Units / Rail
MC14021BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14021BDR2	SOIC−16	2500 Units / Tape & Reel
MC14021BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
MC14021BF	SOEIAJ−16	50 Units / Rail
MC14021BFEL	SOEIAJ−16	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

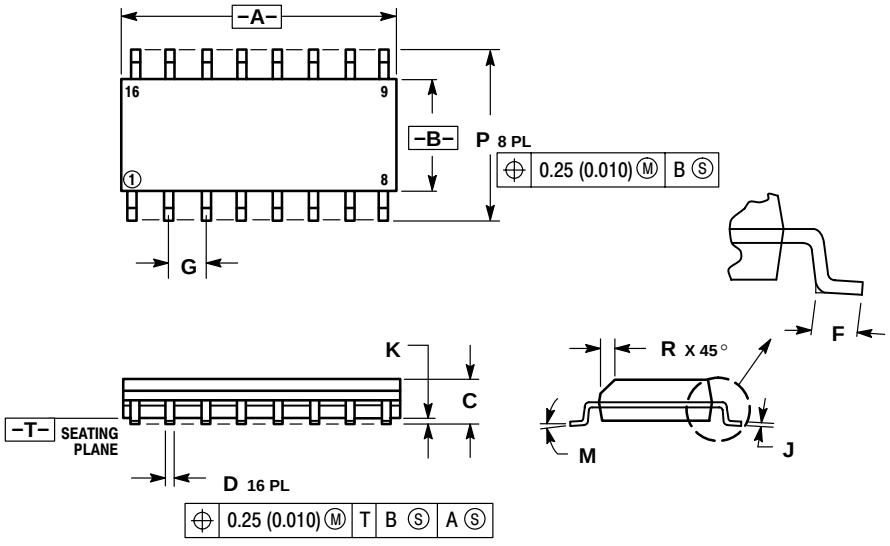
PDIP−16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC−16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B−05
ISSUE J

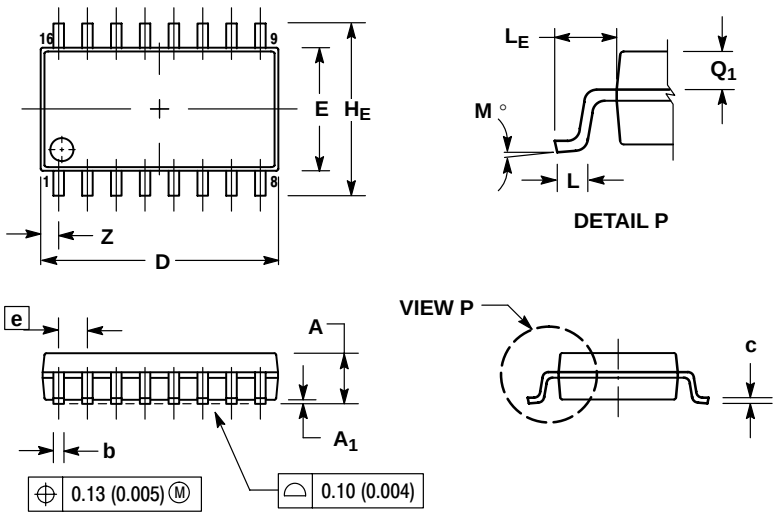


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

SOEIAJ−16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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