查询"MB90487PF"供应商

DS07-13722-5E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90480/485 Series

MB90F481/F482/487/F488/V480/V485

■ DESCRIPTION

The MB90480/485 series is a 16-bit general-purpose FUJITSU microcontroller designed for process control in consumer devices and other applications requiring high-speed real-time processing.

The F²MC-16LX CPU core instruction set retains the AT architecture of the F²MC*1 family, with additional instructions for high-level languages, expanded addressing mode, enhanced multiply-drive instructions, and complete bit processing. In addition, a 32-bit accumulator is provided to enable long-word processing.

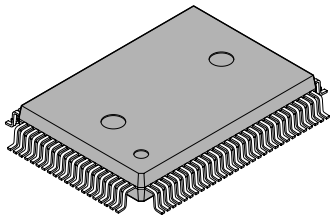
The MB90480/485 series features embedded peripheral resources including 8/16-bit PPG, expanded I/O serial interface, UART, 10-bit A/D converter, 16-bit I/O timer, 8/16-bit up-counter, PWC timer, I²C*2 interface, DTP/external interrupt, chip select, and 16-bit reload timer.

*1 : F²MC, an abbreviation for FUJITSU Flexible Microcontroller, is a registered trademark of FUJITSU, Ltd.

*2 : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C stand a Specification as defined by Philips.

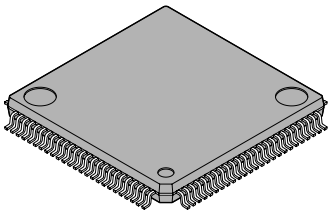
■ PACKAGES

100-pin plastic QFP



(FPT-100P-M06)

100-pin plastic LQFP



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FUJITSU

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■ FEATURES

- Clock
  Minimum instruction execution time: 40.0 ns/6.25 MHz base frequency multiplied ×4 (25 MHz internal operating frequency/3.3 V ± 0.3 V)
  62.5 ns/4 MHz base frequency multiplied ×4 (16 MHz internal operating frequency/3.0 V ± 0.3 V) PLL clock multiplier
- Maximum memory space: 16 Mbyte
- Instruction set optimized for controller applications
  Supported data types (bit, byte, word, or long word)
  Typical addressing modes (23 types)
  Enhanced signed multiplication/division instruction and RETI instruction functions
  32-bit accumulator for enhanced high-precision calculation
- Instruction set designed for high-level language (C) and multi-task operations
  System stack pointer adopted
  Instruction set compatibility and barrel shift instructions
- Non-multiplex bus/multiplex bus compatible
- Enhanced execution speed
  4 byte instruction queue
- Enhanced interrupt functions
  8 levels setting with programmable priority, 8 external interrupts
- Data transmission function (μDMA)
  Up to 16 channels
- Embedded ROM
  Flash versions : 192 KB, 256 KB, MASK versions : 192 KB
- Embedded RAM
  Flash versions : 4 KB, 6 KB, 10 KB, MASK versions : 10 KB
- General purpose ports
  Up to 84 ports
  (Except MB90V480 : Includes 16 ports with input pull-up resistance, 16 ports with output open drain settings)
- A/D converter
  8-channel RC sequential comparison type (10-bit resolution, 3.68 μs conversion time (at 25 MHz))
- I^2C interface (MB90485 series only) : 1channel, P76/P77 Nch OD pin (without Pch)
  Do not apply high voltage in excess of recommended operating ranges to the Nch open drain pin (with Pch) in MB90V485.
- μPG (MB90485 series only) : 1 channel
- UART: 1 channel
- I/O expanded serial interface (SIO) : 2 channels
- 8/16-bit PPG: 3 channels (with 8-bit × 6 channel/16-bit × 3 channel mode switching function)
- 8/16-bit up/down timer: 1 channel (with 8-bit × 2 channel/16-bit × 1-channel mode switching function)
- PWC (MB90485 series only) : 3 channels (Capable of compare the inputs to two of the three)
- 3 V/5 V I/F pin (MB90485 series only)
  P20 to P27, P30 to P37, P40 to P47, P70 to P77
- 16-bit reload timer: 1 channel
- 16-bit I/O timer: 2-channel input capture, 6-channel output compare, 1-channel free run timer
- On chip dual clock generator system
- Low-power consumption mode
  With stop mode, sleep mode, CPU intermittent operation mode, watch mode, timebase timer mode
- Packages: QFP 100/LQFP 100
- Process: CMOS technology
- Power supply voltage: 3 V, single source (some ports can be operated by 5 V power supply at MB90485 series)

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■ PRODUCT LINEUP

● MB90480 series

Item \ Part number		MB90F481	MB90F482	MB90V480
ROM size		FLASH 192 KB	FLASH 256 KB	—
RAM size		4 KB	6 KB	16 KB
CPU function		Number of instructions : 351 Instruction bit length : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data bit length : 1-bit, 8-bits, 16-bits Minimum execution time : 40 ns (25 MHz machine clock)		
Ports		General-purpose I/O ports: up to 84 General-purpose I/O ports (CMOS output) General-purpose I/O ports (with pull-up resistance) General-purpose I/O ports (N-ch open drain)		
UART		1 channel, start-stop synchronized		
8/16-bit PPG timer		8-bit × 6 channel/16-bit × 3 channel		
8/16-bit up/down counter/timer		6 event input pins, 8-bit up/down counters: 2 8-bit reload/compare registers: 2		
16-bit I/O timers	16-bit free run timer	Number of channels: 1 Overflow interrupt		
	Output compare (OCU)	Number of channels: 6 Pin input factor: A match signal of compare register		
	Input capture (ICU)	Number of channels: 2 Rewriting a register value upon a pin input (rising, falling, or both edges)		
DTP/external interrupt circuit		Number of external interrupt channels: 8 (edge or level detection)		
Extended I/O serial interface		2 channels, embedded		
Timebase timer		18-bit counter Interrupt cycles: 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (at 4 MHz base oscillator)		
A/D converter		Conversion resolution: 8/10-bit, switchable One-shot conversion mode (converts selected channel 1 time only) Scan conversion mode (conversion of multiple consecutive channels, programmable up to 8 channels) Continuous conversion mode (repeated conversion of selected channels) Stop conversion mode (conversion of selected channels with repeated pause)		
Watchdog timer		Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (minimum value, at 4 MHz base oscillator)		
Low-power consumption (standby) modes		Sleep mode, stop mode, CPU intermittent mode, watch timer mode, timebase timer mode		
Process		CMOS		
Type		FLASH model Not included security function		Evaluation model, user terminal, 3 V/5 V versions
Emulator power supply*		—		Included

* : It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply switching) about details.

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• **MB90485 series**

Item \ Part number		MB90487*1	MB90F488*2	MB90V485*1
ROM size		192 KB	FLASH 256 KB	—
RAM size		10 KB	10 KB	16 KB
CPU function		Number of instructions : 351 Instruction bit length : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data bit length : 1-bit, 8-bits, 16-bits Minimum execution time : 40 ns (25 MHz machine clock)		
Ports		General-purpose I/O ports: up to 84 General-purpose I/O ports (CMOS output) General-purpose I/O ports (with pull-up resistance) General-purpose I/O ports (N-ch open drain)		
UART		1 channel, start-stop synchronized		
8/16-bit PPG timer		8-bit × 6 channel/16-bit × 3 channel		
8/16-bit up/down counter/timer		6 event input pins, 8-bit up/down counters: 2 8-bit reload/compare registers: 2		
16-bit I/O timers	16-bit free run timer	Number of channels: 1 Overflow interrupt		
	Output compare (OCU)	Number of channels: 6 Pin input factor: A match signal of compare register		
	Input capture (ICU)	Number of channels: 2 Rewriting a register value upon a pin input (rising, falling, or both edges)		
DTP/external interrupt circuit		Number of external interrupt channels: 8 (edge or level detection)		
Extended I/O serial interface		2 channels, embedded		
I^2C interface *4		1 ch		
µPG		1 ch		
PWC		3 ch		
Timebase timer		18-bit counter Interrupt cycles: 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (at 4 MHz base oscillator)		
A/D converter		Conversion resolution: 8/10-bit, switchable One-shot conversion mode (converts selected channel 1 time only) Scan conversion mode (conversion of multiple consecutive channels, programmable up to 8 channels) Continuous conversion mode (repeated conversion of selected channels) Stop conversion mode (conversion of selected channels with repeated pause)		
Watchdog timer		Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (minimum value, at 4 MHz base oscillator)		
Low-power consumption (standby) modes		Sleep mode, stop mode, CPU intermittent mode, watch timer mode, timebase timer mode		
Process		CMOS		

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Item \ Part number	MB90487*1	MB90F488*2	MB90V485*1
Type	MASK model 3 V/5 V power supply*3	FLASH model 3 V/5 V power supply*3 Included security function	Evaluation model 3 V/5 V power supply*3
Emulator power supply*5	—	—	Included

*1 : Under development

*2 : Being planed

*3 : 3 V/5 V I/F pin : All pins should be for 3 V power supply without P20 to P27, P30 to P37, P40 to P47, and P70 to P77.

*4 : P76/P77 pins are Nch open drain pins (without Pch) at built-in I^2C. However, MB90V485 uses the Nch open drain pin (with Pch) .

*5 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

Note : As for MB90V485, Input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/µPG/I^2C become CMOS input.

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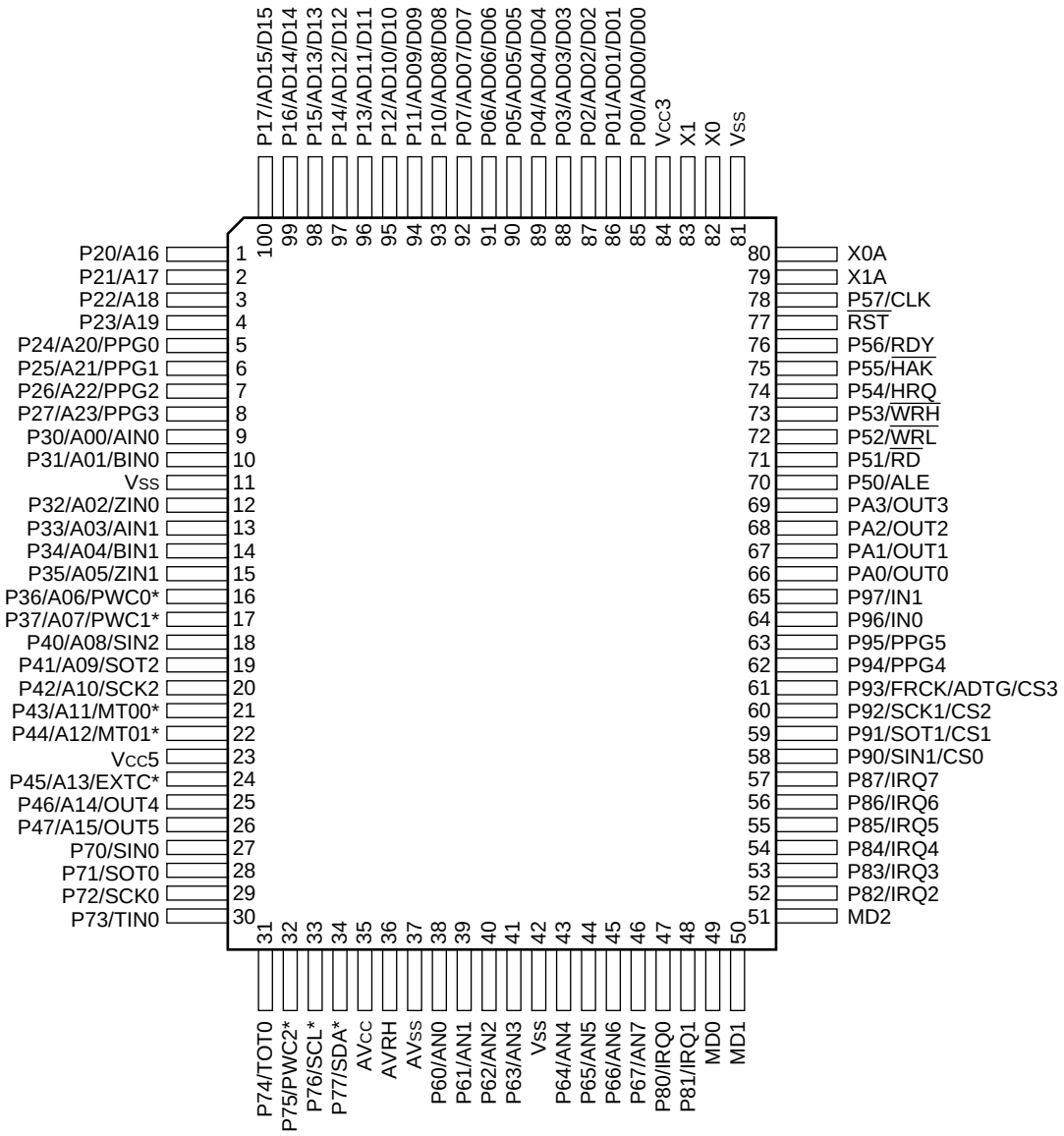
■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-100P-M06)

* : These are the pins for MB90485 series. The pins for MB90480 series are P36/A06, P37/A07, P43/A11, P44/A12, P45/A13, P75, P76 and P77.

Note : MB90485 series only

- I²C pin P77 and P76 are Nch open drain pin (without Pch) . However, MB90V485 uses the Nch open drain pin (with Pch) .
- P20 to P27, P30 to P37, P40 to P47 and P70 to P77 also used as 3 V/5 V I/F pin.
- As for MB90V485, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/µPG/I²C become CMOS input.

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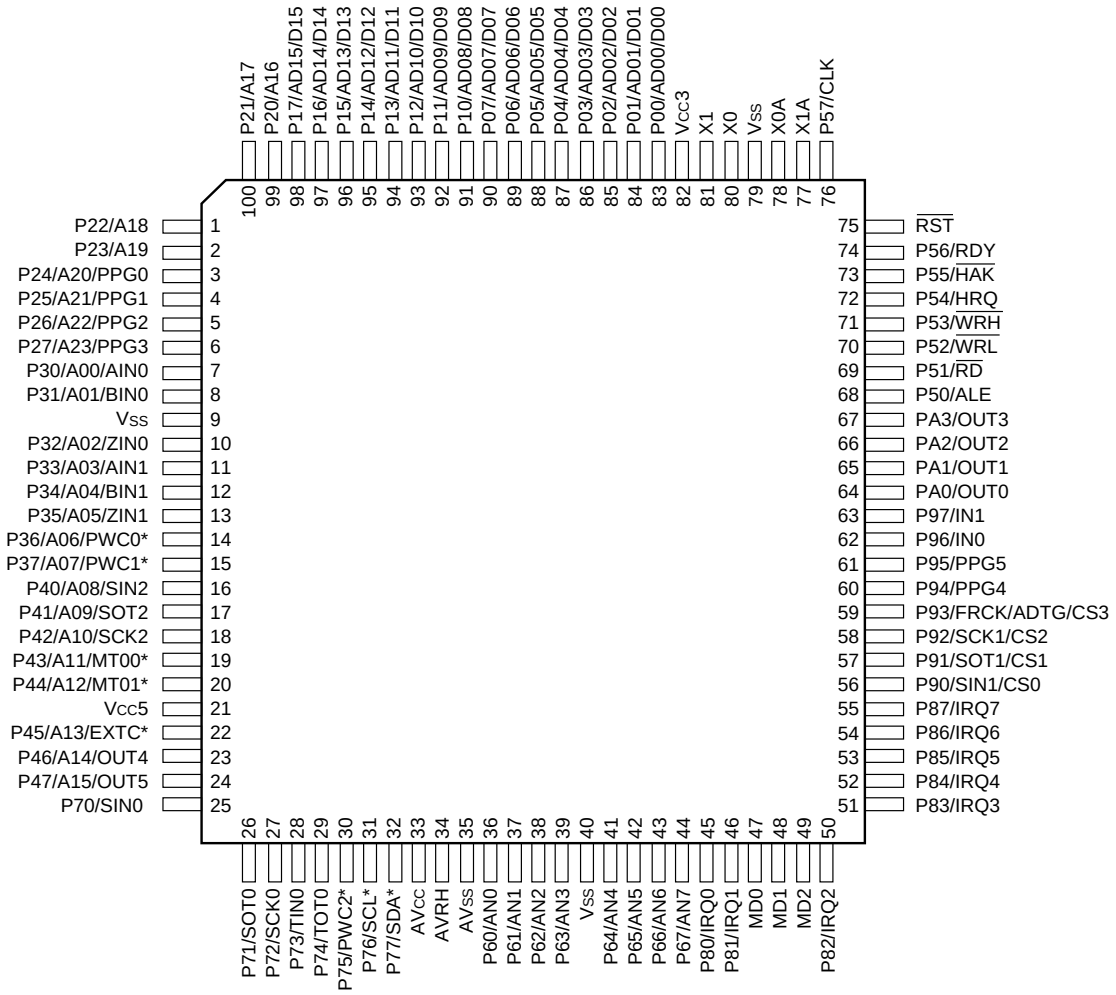
(TOP VIEW)



(FPT-100P-M05)

* : These are the pins for MB90485 series. The pins for MB90480 series are P36/A06, P37/A07, P43/A11, P44/A12, P45/A13, P75, P76 and P77.

Note : MB90485 series only

- I^2C pin P77 and P76 are Nch open drain pin (without Pch) . However, MB90V485 uses the Nch open drain pin (with Pch) .
- P20 to P27, P30 to P37, P40 to P47 and P70 to P77 also used as 3 V/5 V I/F pin.
- As for MB90V485, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/µPG/I^2C become CMOS input.

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■ PIN DESCRIPTIONS

Pin No.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
80	82	X0	A	Oscillator pin
81	83	X1	A	Oscillator pin
78	80	X0A	A	32 kHz oscillator pin
77	79	X1A	A	32 kHz oscillator pin
75	77	$\overline{RST}$	B	Reset input pin
83 to 90	85 to 92	P00 to P07	C (CMOS)	This is a general purpose I/O port. A setting in the pull-up resistance setting register (RDR0) can be used to apply pull-up resistance (RD00-RD07 = “1”) . (Disabled when pin is set for output.)
		AD00 to AD07		In multiplex mode, these pins function as the external address/data bus low I/O pins.
		D00 to D07		In non-multiplex mode, these pins function as the external data bus low output pins.
91 to 98	93 to 100	P10 to P17	C (CMOS)	This is a general purpose I/O port. A setting in the pull-up resistance setting resister (RDR1) can be used to apply pull-up resistance (RD10-RD17 = “1”) . (Disabled when pin is set for output.)
		AD08 to AD15		In multiplex mode, these pins function as the external address/data bus high I/O pins.
		D08 to D15		In non-multiplex mode, these pins function as the external data bus high output pins.
99, 100, 1,2	1 to 4	P20 to P23	E (CMOS/H)	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to "1" in external bus mode, these pins function as general purpose I/O ports.
		A16 to A19		When the bits of external address output control register (HACR) are set to "0" in multiplex mode, these pins function as address high output pins (A16-A19).
		A16 to A19		When the bits of external address output control register (HACR) are set to "0" in non-multiplex mode, these pins function as address high output pins (A16-A19).
3 to 6	5 to 8	P24 to P27	E (CMOS/H)	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to "1" in external bus mode, these pins function as general purpose I/O ports.
		A20 to A23		When the bits of external address output control register (HACR) are set to "0" in multiplex mode, these pins function as address high output pins (A20-A23).
		A20 to A23		When the bits of external address output control register (HACR) are set to "0" in non-multiplex mode, these pins function as address high output pins (A20-A23).
		PPG0 to PPG3		PPG timer output pins.
7	9	P30	E (CMOS/H)	This is a general purpose I/O port.
		A00		In non-multiplex mode, this pin functions as an external address pin.
		AIN0		8/16-bit up/down timer input pin (channel 0) .

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Pin No.		Pin name	Circuit type	Function	
LQFP*1	QFP*2				
8	10	P31	E (CMOS/H)	This is a general purpose I/O port.	
		A01		In non-multplex mode, this pin functions as an external address pin.	
		BIN0		8/16-bit up/down counter input pin (channel 0) .	
10	12	P32	E (CMOS/H)	This is a general purpose I/O port.	
		A02		In non-multiplex mode, this pin functions as an external address pin.	
		ZIN0		8/16-bit up/down counter input pin (channel 0)	
11	13	P33	E (CMOS/H)	This is a general purpose I/O port.	
		A03		In non-multiplex mode, this pin functions as an external address pin.	
		AIN1		8/16-bit up/down counter input pin (channel 1) .	
12	14	P34	E (CMOS/H)	This is a general purpose I/O port.	
		A04		In non-multiplex mode, this pin functions as an external address pin.	
		BIN1		8/16-bit up/down counter input pin (channel 1) .	
13	15	P35	E (CMOS/H)	This is a general purpose I/O port.	
		A05		In non-multiplex mode, this pin functions as an external address pin.	
		ZIN1		8/16-bit up/down counter input pin (channel 1)	
14 15	16 17*3	P36, P37	D (CMOS)	MB90480 series	This is a general purpose I/O port.
		A06, A07			In non-multiplex mode, this pin functions as an external address pin.
		P36, P37	E (CMOS/H)	MB90485 series	This is a general purpose I/O port.
		A06, A07			In non-multiplex mode, this pin functions as an external address pin.
		PWC0, PWC1			This is a PWC input pin.
16	18	P40	G (CMOS/H)	This is a general purpose I/O port.	
		A08		In non-multiplex mode, this pin functions as an external address pin.	
		SIN2		Simple serial I/O input pin.	
17	19	P41	F (CMOS)	This is a general purpose I/O port.	
		A09		In non-multiplex mode, this pin functions as an external address pin.	
		SOT2		Simple serial I/O output pin.	
18	20	P42	G (CMOS/H)	This is a general purpose I/O port.	
		A10		In non-multiplex mode, this pin functions as an external address pin.	
		SCK2		Simple serial I/O clock input/output pin.	
19 20	21 22	P43, P44	F (CMOS)	MB90480 series	This is a general purpose I/O port.
		A11, A12			In non-multiplex mode, this pin functions as an external address pin.
		P43, P44	F (CMOS)	MB90485 series	This is a general purpose I/O port.
		A11, A12			In non-multiplex mode, this pin functions as an external address pin.
		MT00, MT01			μPG output pin.

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Pin No. LQFP*1	Pin No. QFP*2	Pin name	Circuit type	Function	
22	24	P45	F (CMOS)	MB90480 series	This is a general purpose I/O port.
		A13			In non-multiplex mode, this pin functions as an external address pin.
		P45	G (CMOS/H)	MB90485 series	This is a general purpose I/O port.
		A13			In non-multiplex mode, this pin functions as an external address pin.
		EXTC*3			µPG input pin (MB90485 series only) .
23 24	25 26	P46, P47	F (CMOS)	This is a general purpose I/O port.	
		A14, A15		In non-multiplex mode, this pin functions as an external address pin.	
		OUT4/ OUT5		Output compare event output pins.	
68	70	P50	D (CMOS)	This is a general purpose I/O port. In external bus mode, this pin functions as the ALE pin.	
		ALE		In external bus mode, this pin functions as the address load enable (ALE) signal pin.	
69	71	P51	D (CMOS)	This is a general purpose I/O port. In external bus mode, this pin functions as the $\overline{RD}$ pin.	
		$\overline{RD}$		In external bus mode, this pin functions as the read strobe output ($\overline{RD}$) signal pin.	
70	72	P52	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the WRE pin in the EPCR register is set to “1”, this pin functions as the $\overline{WRL}$ pin.	
		$\overline{WRL}$		In external bus mode, this pin functions as the lower data write strobe output ($\overline{WRL}$) pin. When the WRE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	
71	73	P53	D (CMOS)	This is a general purpose I/O port. In external bus mode with 16-bit bus width, when the WRE bit in the EPCR register is set to “1”, this pin functions as the $\overline{WRH}$ pin.	
		$\overline{WRH}$		In external bus mode with 16-bit bus width, this pin functions as the upper data write strobe output ($\overline{WRH}$) pin. When the WRE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	
72	74	P54	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the HDE bit in the EPCR register is set to “1”, this pin functions as the HRQ pin.	
		HRQ		In external bus mode, this pin functions as the hold request input (HRQ) pin. When the HDE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	
73	75	P55	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the HDE bit in the EPCR register is set to “1”, this pin functions as the $\overline{HAK}$ pin.	
		$\overline{HAK}$		In external bus mode, this pin functions as the hold acknowledge ($\overline{HAK}$) pin. When the HDE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	

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Pin No.		Pin name	Circuit type	Function	
LQFP*1	QFP*2				
74	76	P56	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the RYE bit in the EPCR register is set to “1”, this pin functions as the RDY pin.	
		RDY		In external bus mode, this pin functions as the external ready (RDY) input pin. When the RYE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	
76	78	P57	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the CKE bit in the EPCR register is set to “1”, this pin functions as the CLK pin.	
		CLK		In external bus mode, this pin functions as the machine cycle clock (CLK) output pin. When the CKE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	
36 to 39	38 to 41	P60 to P63	H (CMOS)	These are general purpose I/O ports.	
		AN0 to AN3		These are the analog input pins.	
41 to 44	43 to 46	P64 to P67	H (CMOS)	These are general purpose I/O ports.	
		AN4 to AN7		These are the analog input pins.	
25	27	P70	G (CMOS/H)	This is a general purpose I/O port.	
		SIN0		This is the UART data input pin.	
26	28	P71	F (CMOS)	This is a general purpose I/O port.	
		SOT0		This is the UART data output pin.	
27	29	P72	G (CMOS/H)	This is a general purpose I/O port.	
		SCK0		This is the UART clock I/O pin.	
28	30	P73	G (CMOS/H)	This is a general purpose I/O port.	
		TIN0		This is the 16-bit reload timer event input pin.	
29	31	P74	F (CMOS)	This is a general purpose I/O port.	
		TOT0		This is the 16-bit reload timer output pin.	
30	32	P75	F (CMOS)	MB90480 series	This is a general purpose I/O port.
		P75	G (CMOS/H)	MB90485 series	This is a general purpose I/O port.
		PWC2*3			This is a PWC input pin.
31	33	P76	F (CMOS)	MB90480 series	This is a general purpose I/O port.
		P76	I (NMOS/H)	MB90485 series	This is a general purpose I/O port.
		SCL*3			Serves as the I²C interface data I/O pin. During operation of the I²C interface, leave the port output in a high impedance state.
32	34	P77	F (CMOS)	MB90480 series	This is a general purpose I/O port.
		P77	I (NMOS/H)	MB90485 series	This is a general purpose I/O port.
		SDA*3			Serves as the I²C interface data I/O pin. During operation of the I²C interface, leave the port output in a high impedance state.
45, 46	47, 48	P80, P81	E (CMOS/H)	These are general purpose I/O ports.	
		IRQ0, IRQ1		External interrupt input pins.	

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Pin No. LQFP*1	Pin No. QFP*2	Pin name	Circuit type	Function
50 to 55	52 to 57	P82 to P87	E (CMOS/H)	These are general purpose I/O ports.
		IRQ2 to IRQ7		External interrupt input pins.
56	58	P90	E (CMOS/H)	This is a general purpose I/O port.
		SIN1		Simple serial I/O data input pin.
		CS0		Chip select 0.
57	59	P91	D (CMOS)	This is a general purpose I/O port.
		SOT1		Simple serial I/O data output pin.
		CS1		Chip select 1.
58	60	P92	E (CMOS/H)	This is a general purpose I/O port.
		SCK1		Simple serial I/O data input/output pin.
		CS2		Chip select 2.
59	61	P93	E (CMOS/H)	This is a general purpose I/O port.
		FRCK		When the free run timer is in use, this pin functions as the external clock input pin.
		ADTG		When the A/D converter is in use, this pin functions as the external trigger input pin.
		CS3		Chip select 3.
60	62	P94	D (CMOS)	This is a general purpose I/O port.
		PPG4		PPG timer output pin.
61	63	P95	D (CMOS)	This is a general purpose I/O port.
		PPG5		PPG timer output pin.
62	64	P96	E (CMOS/H)	This is a general purpose I/O port.
		IN0		Input capture channel 0 trigger input pin.
63	65	P97	E (CMOS/H)	This is a general purpose I/O port.
		IN1		Input capture channel 1 trigger input pin.
64 to 67	66 to 69	PA0 to PA3	D (CMOS)	These are general purpose I/O ports.
		OUT0 to OUT3		Output compare event output pins.
33	35	AV_{CC}	—	A/D converter power supply pin.
34	36	AVRH	—	A/D converter external reference voltage supply pin.
35	37	AV_{SS}	—	A/D converter power supply pin.
47 to 49	49 to 51	MD0 to MD2	J (CMOS/H)	Operating mode selection input pins.
82	84	$V_{CC}3$	—	3.3 V ± 0.3 V power supply pins ($V_{CC}3$) .
21	23	$V_{CC}5$	—	MB90480 seriesv: 3.3 V ± 0.3 V power supply pin. Usually, use $V_{CC} = V_{CC}3 = V_{CC}5$ as a 3 V power supply.
				MB90485 series: 3 V/5 V power supply pin. 5 V power supply pin when P20 to P27, P30 to P37, P40 to P47, P70 to P77 are used as 5 V I/F pins. Usually, use $V_{CC} = V_{CC}3 = V_{CC}5$ as a 3 V power supply (when the 3 V power supply is used alone) .
9 40 79	11 42 81	V_{SS}	—	Power supply input pins (GND) .

*1 : LQFP : FPT-100P-M05
*2 : QFP : FPT-100P-M06
*3 : As for MB90V485, input pins become CMOS input.

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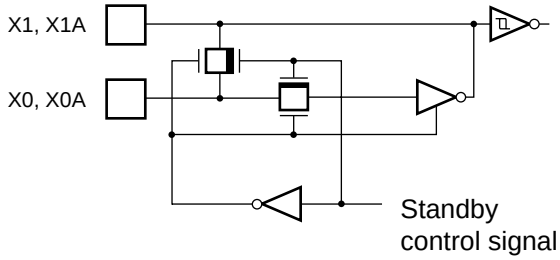
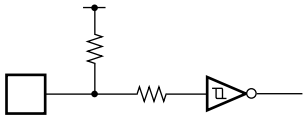
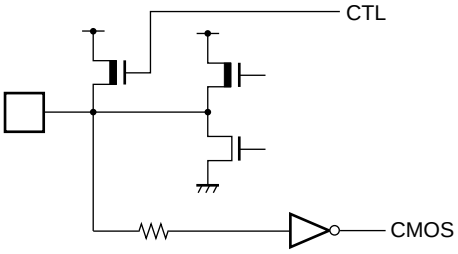
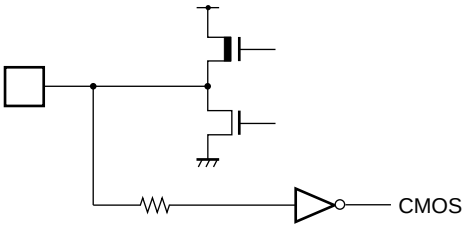
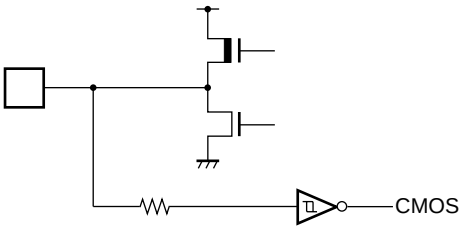
■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		Oscillator feedback resistance X1, X0 : approx. 1 MΩ X1A, X0A : approx. 10 MΩ with standby control
B		Hysteresis input with pull-up resistance Resistance : approx. 50 kΩ
C		With input pull-up resistance control Resistance : approx. 50 kΩ CMOS level input/output
D		CMOS level input/output
E		Hysteresis input CMOS level output

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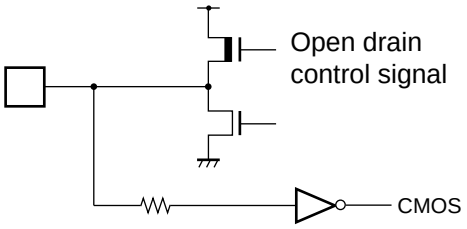
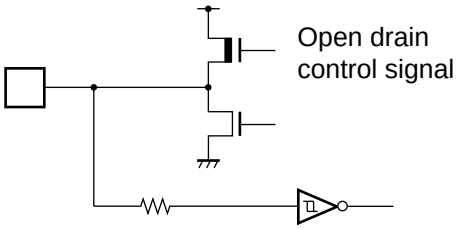
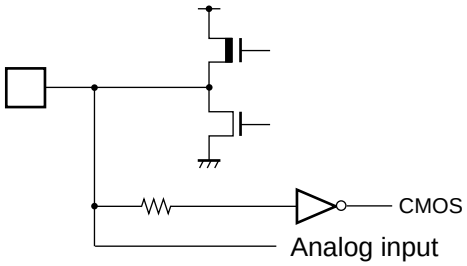
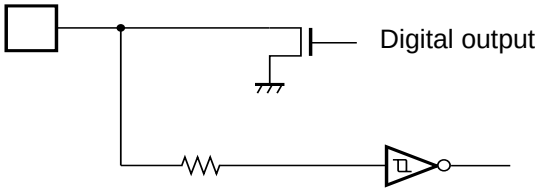
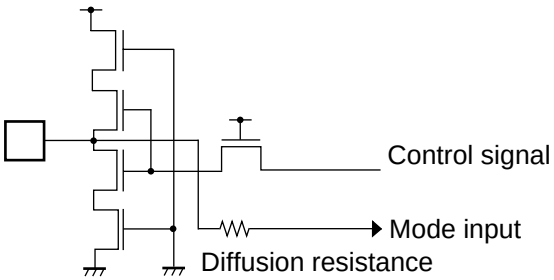
(Continued)

Type	Circuit	Remarks
F		CMOS level input/output with open drain control
G		CMOS level output Hysteresis input With open drain control
H		CMOS level input/output Analog input
I		Hysteresis input Nch open drain output
J	FLASH model 	(FLASH model) CMOS level input with high voltage control for flash testing
	MASK model 	(Mask model) Hysteresis input

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■ HANDLING DEVICES

1. Be careful never to exceed maximum rated voltages (preventing latchup)

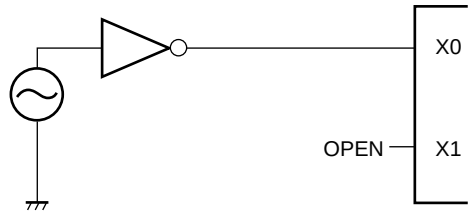
In CMOS IC devices, a condition known as latchup may occur if voltages higher than V_{CC} or loser than V_{SS} are applied to input or output pins other than medium-or high-voltage pins, or if the voltage applied between V_{CC} and V_{SS} exceeds the rated voltage level.
When latchup occurs, the power supply current increases rapidly causing the possibility of thermal damage to circuit elements. Therefore it is necessary to ensure that maximum ratings are not exceeded in circuit operation. Similarly, when turning the analog power supply on or off, it is necessary to ensure that the analog power supply voltages (AV_{CC} and AVRH) and analog input voltages do not exceed the digital power supply (V_{CC}) .

2. Treatment of unused pins

Leaving unused input pins unconnected can cause abnormal operation or latchup, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/ output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins.

3. Notes on Using External Clock

Even when using an external clock signal, an oscilltion stabilization delay is applied after a power-on reset or when recovering from sub-clock or stop mode. When using an external clock, 25 MHz should be the upper frequency limit.
The following figure shows a sample use of external clock signals.



4. Treatment of Power Supply Pins (V_{CC}/V_{SS})

When multiple V_{CC}/V_{SS} pins are present, device design considerations for prevention of latch-up and unwanted electromagnetic interference, abnormal storobe signal operation due to ground level rise, and conformity with total output current ratings require that all power supply pins must be externally connected to power supply or ground.
Consideration should be given to connecting power supply sources to the V_{CC}/V_{SS} terminals of this device with as low impedane as possible. It is also recommended that a bypass capacitor of approximately 0.1 µF be placed between the V_{CC} and V_{SS} lines as close to this device as possible.

5. Crystal Oscillator Circuits

Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

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6. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

7. Proper power-on/off sequence

The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be turned on after the digital power supply (V_{CC}) is turned on. The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be shut off before the digital power supply (V_{CC}) is shut off. Care should be taken that AVRH does not exceed AV_{CC}. Even when pins used as analog input pins are doubled as input ports, be sure that the input voltage does not exceed AV_{CC}.

8. Treatment of power supply pins on models with A/D converters

Even when the A/D converters are not in use, be sure to make the necessary connections AV_{CC} = AVRH = V_{CC}, and AV_{SS} = V_{SS}.

9. Precautions when turning the power supply on

In order to prevent abnormal operation in the chip's internal step-down circuits, a voltage rise time during power-on of 50 µs (0.2 V to 2.7 V) or greater should be assured.

10. Supply Voltage Stabilization

Even within the operating range of V_{CC} supply voltage, rapid voltage fluctuations may cause abnormal operation. As a standard for power supply voltage stability, it is recommended that the peak-to-peak V_{CC} ripple voltage at commercial supply frequency (50 Hz to 60 Hz) be 10 % or less of V_{CC}, and that the transient voltage fluctuation be no more than 0.1 V/ms or less when the power supply is turned on or off.

11. Notes on Using Power Supply

Only the MB90485 series usually uses a 3 V power supply. By setting $V_{CC}3$ = 3 V power supply and $V_{CC}5$ = 5 V power supply, P20 to P27, P30 to P37, P40 to P47 and P70 to P77 can be intefaced as 5 V power supplies separately from the main 3 V power supply. Note that the analog power supplies (such as AV_{CC} and AV_{SS}) for the A/D converter can be used only as 3 V power supplies.

Programming into FLASH memory must be performed at an operating voltage (V_{CC}) between 3.13 V and 3.6 V.

12. Treatment of N.C. pins

N.C. (internally connected) pins should always be left open.

13. When the MB90480/485 series microcontroller is used as a single system

When the MB90480/485 series microcontroller is used as a single system, use connections so the X0A = V_{SS}, and X1A = Open.

14. Writing to FLASH memory

For serial writing to FLASH memory, always ensure that the operating voltage V_{CC} is between 3.13 V and 3.6 V. For normal writing to FLASH memory, always ensure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

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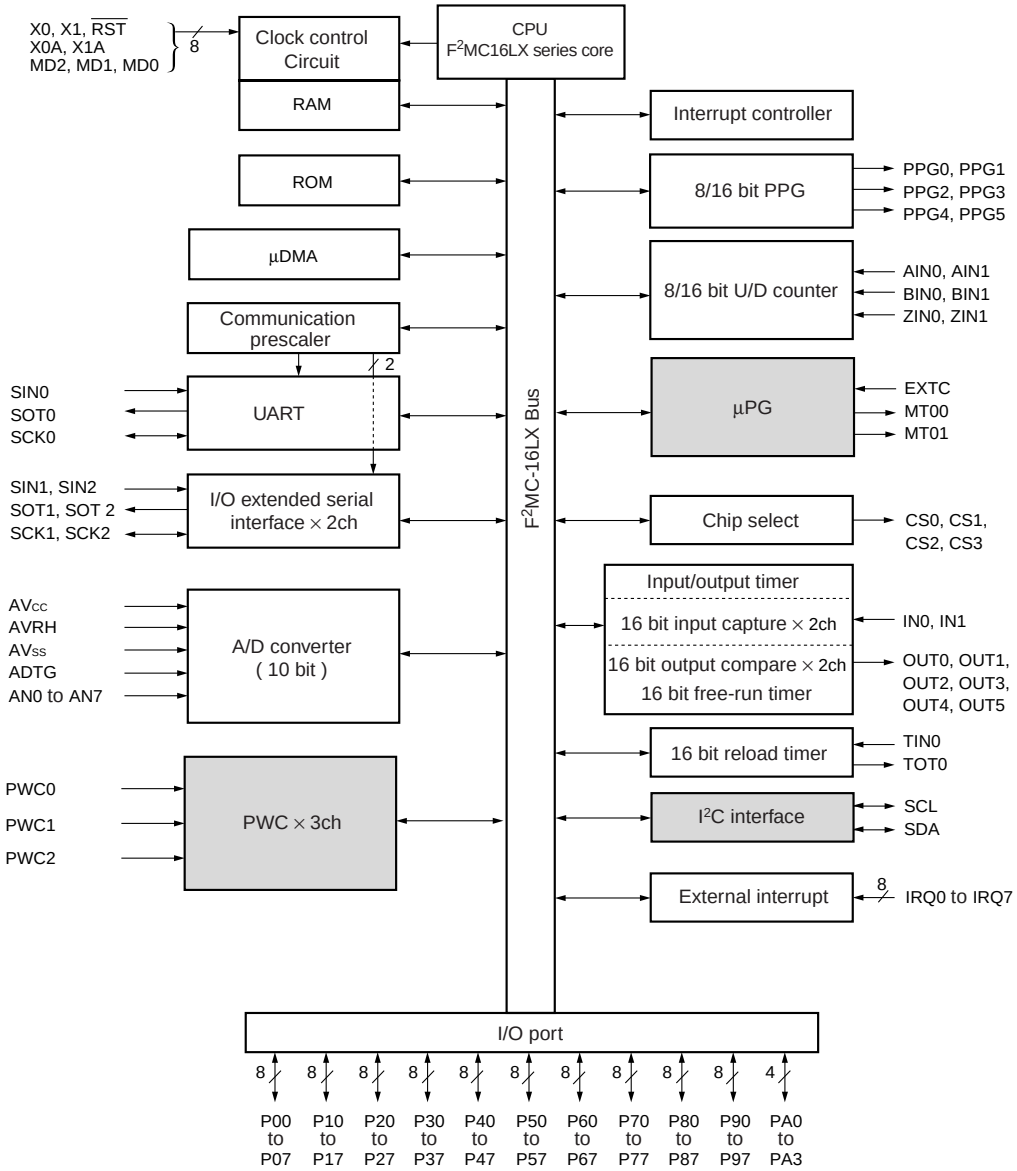
■ BLOCK DIAGRAM



P00 to P07 (8 pins) : with an input pull-up resistance setting register.
P10 to P17 (8 pins) : with an input pull-up resistance setting register.
P40 to P47 (8 pins) : with an open drain setting register.
P70 to P75 (6 pins) : with an open drain setting register.

MB90485 series only

- I²C pin P77 and P76 are Nch open drain pin (without Pch) . However, MB90V485 uses the Nch open drain pin (with Pch) .
- P20 to P27, P30 to P37, P40 to P47 and P70 to P77 also used as 3 V/5 V I/F pin.
- As for MB90V485, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/µPG/I²C become CMOS input.

Note : In the above diagram, I/O ports share internal function blocks and pins. However, when a set of pins is used with an internal module, it cannot also be used as an I/O port.

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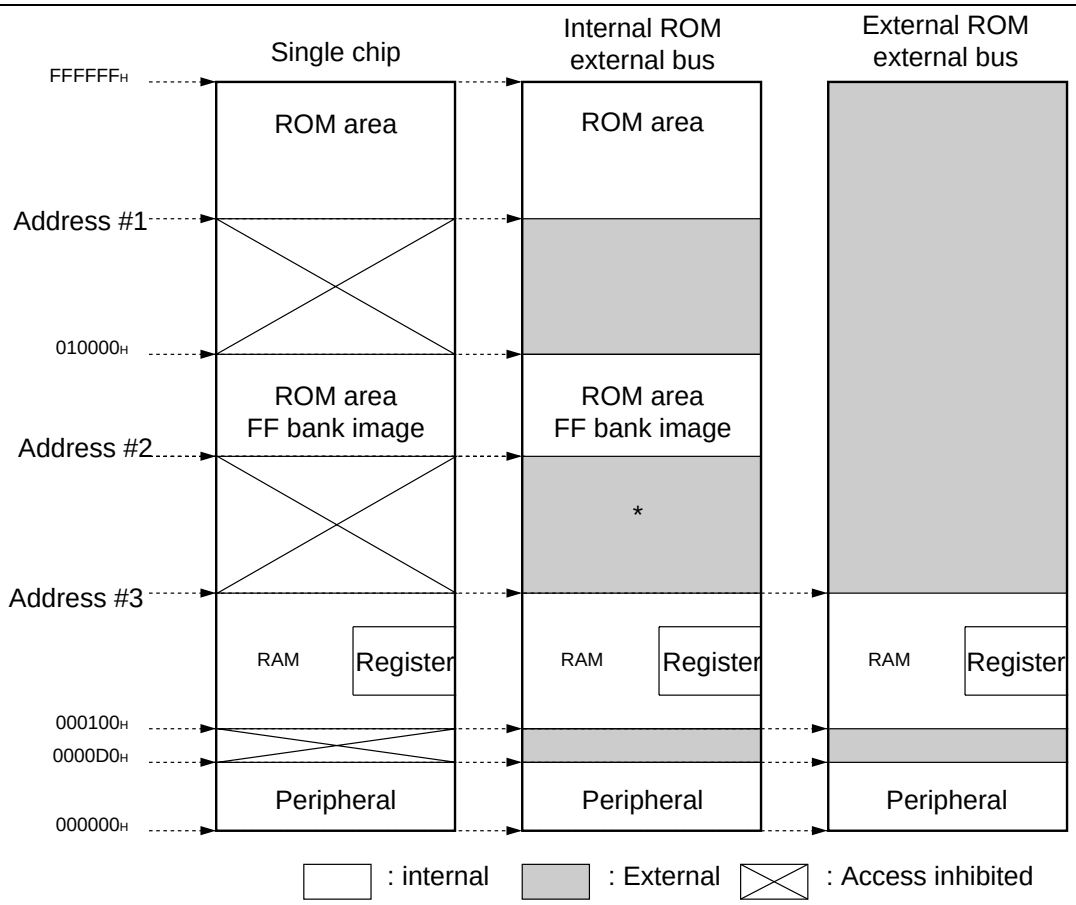
■ MEMORY MAP



* : In models where address #3 overlaps with address #2, this external area does not exist.

Model	Address #1	Address #2	Address #3
MB90F481	FC0000H *	004000H or 008000H, selected by the MS bit in the ROMM register	001100H
MB90F482	FC0000H		001900H
MB90487	FD0000H		002900H
MB90F488	FC0000H		002900H
MB90V480	(FC0000H)		004000H
MB90V485	(FC0000H)		004000H

* : No memory cells from FC0000H to FC7FFFH and FE0000H to FE7FFFH.

The upper part of the 00 bank is set up to mirror the image of FF bank ROM, to enable efficient use of small model C compilers. Because the lower 16-bit address of the FF bank and the lower 16-bit address of the 00 bank is the same, enabling reference to tables in ROM without the “far” pointer declaration.
For example, in accessing address 00C000H it is actually the contents of ROM at FFC000H that are accessed. If the MS bit in the ROMM register is set to “0”, the ROM area in the FF bank will exceed 48 K bytes and it is not possible to reflect the entire area in the image in the 00 bank. Therefore the image from FF4000H to FFFFFFH is reflected in the 00 bank and the area from FF0000H to FF3FFFH can be seen in the FF bank only.

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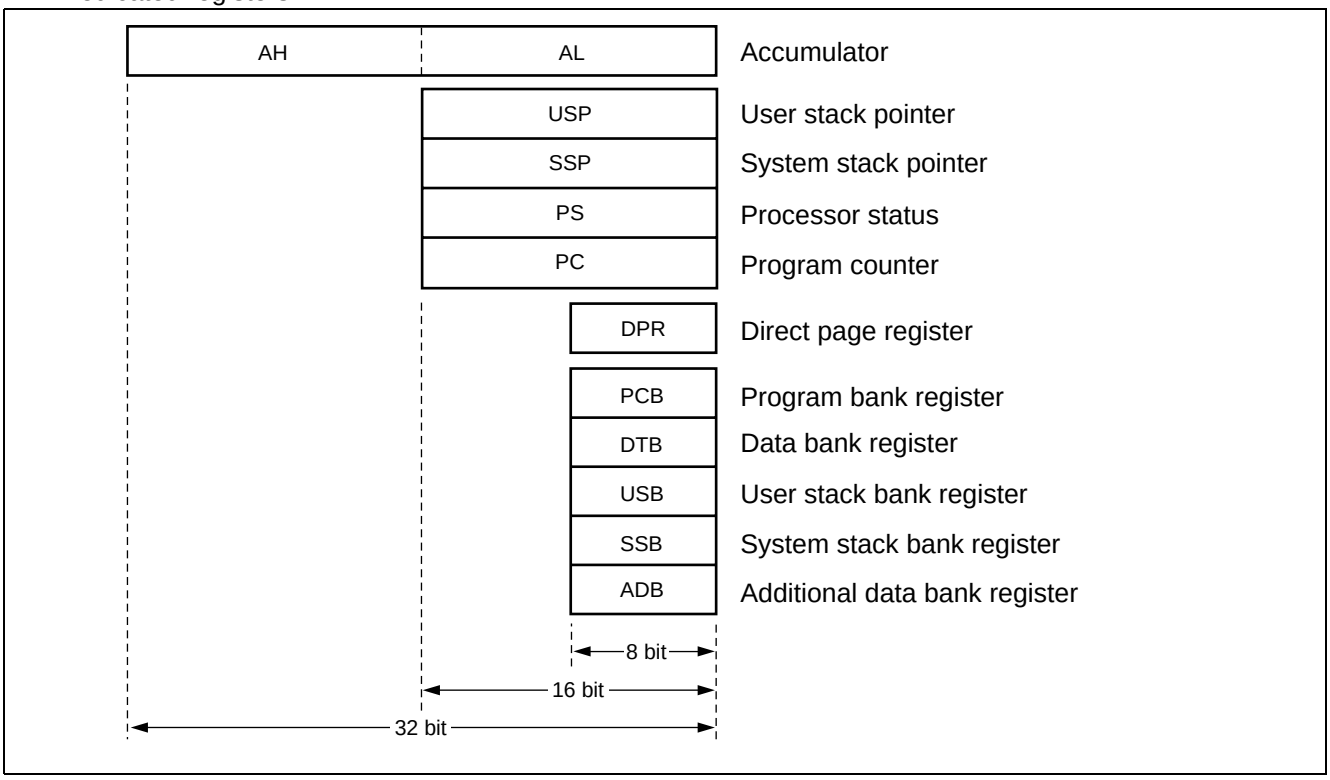
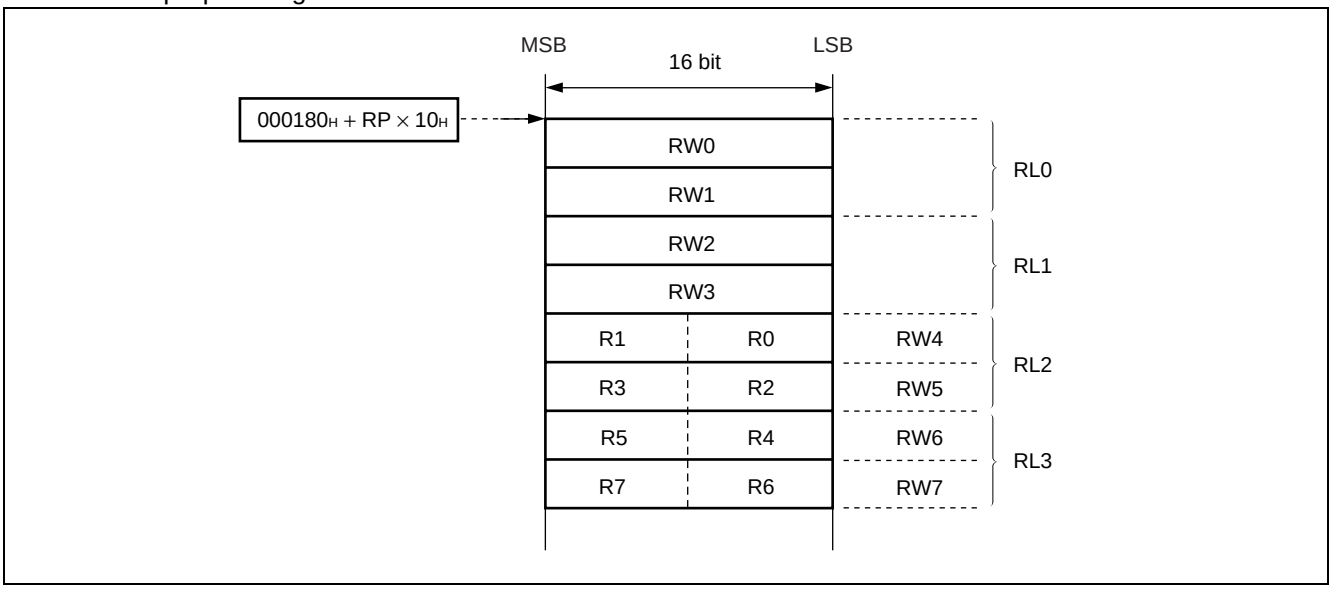
■ F²MC-16L CPU PROGRAMMING MODEL

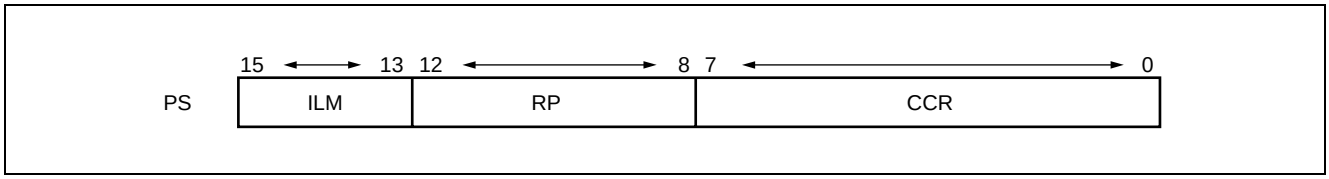
- Dedicated registers



- General purpose registers



- Processor status



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■ I/O MAP

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
00H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
01H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
02H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
03H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
04H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
05H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
06H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
07H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB (MB90480 series) 11XXXXXXB (MB90485 series)
08H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
09H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
0AH	Port A data register	PDRA	R/W	Port A	- - - - XXXXB
0BH	Up/down timer input enable register	UDRE	R/W	U/D timer input control	XX 0 0 0 0 0 0B
0CH	Interrupt/DTP enable register	ENIR	R/W	DTP/external interrupts	0 0 0 0 0 0 0 0B
0DH	Interrupt/DTP source register	EIRR	R/W		XXXXXXXXB
0EH	Request level setting register	ELVR	R/W		0 0 0 0 0 0 0 0B
0FH	Request level setting register		R/W		0 0 0 0 0 0 0 0B
10H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0B
11H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0B
12H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0B
13H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0B
14H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0B
15H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0B
16H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0B
17H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0B (MB90480 series) XX0 0 0 0 0 0B (MB90485 series)
18H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0B
19H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0B
1AH	Port A direction register	DDRA	R/W	Port A	- - - - 0 0 0 0B
1BH	Port 4 output pin register	ODR4	R/W	Port 4 (OD control)	0 0 0 0 0 0 0 0B
1CH	Port 0 input resistance register	RDR0	R/W	Port 0 (Pull-up)	0 0 0 0 0 0 0 0B
1DH	Port 1 input resistance register	RDR1	R/W	Port 1 (Pull-up)	0 0 0 0 0 0 0 0B
1EH	Port 7 output pin register	ODR7	R/W	Port 7 (OD control)	0 0 0 0 0 0 0 0B (MB90480 series) XX0 0 0 0 0 0B (MB90485 series)
1FH	Analog input enable register	ADER	R/W	Port 5, A/D	1 1 1 1 1 1 1 1B

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Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
20_H	Serial mode register	SMR	R/W	UART	0 0 0 0 0 X 0 0_B
21_H	Serial control register	SCR	R/W		0 0 0 0 0 1 0 0_B
22_H	Serial input/output register	SIDR/SODR	R/W		XXXXXXXX$_B$
23_H	Serial data register	SSR	R/W		0 0 0 0 1 0 0 0_B
24_H	(Reserved area)				
25_H	Communication prescaler control register	CDCR	R/W	Communication prescaler (UART)	0 0 - - 0 0 0 0_B
26_H	Serial mode control status register	SMCS	R/W	SCI1 (ch0)	- - - - 0 0 0 0_B
27_H	Serial mode control status register	SMCS	R/W		0 0 0 0 0 0 1 0_B
28_H	Serial data register	SDR0	R/W		XXXXXXXX$_B$
29_H	Communication prescaler control register	SDCR0	R/W	Communication prescaler (SCI1)	0 - - - 0 0 0 0_B
$2A_H$	Serial mode control status register	SMCS	R/W	SCI2 (ch1)	- - - - 0 0 0 0_B
$2B_H$	Serial mode control status register	SMCS	R/W		0 0 0 0 0 0 1 0_B
$2C_H$	Serial data register	SDR1	R/W		XXXXXXXX$_B$
$2D_H$	Communication prescaler control register	SDCR1	R/W	Communication prescaler (SCI2)	0 - - - 0 0 0 0_B
$2E_H$	Reload register L	PPLL0	R/W	8/16-bit PPG (ch0 to ch5)	XXXXXXXX$_B$
$2F_H$	Reload register H	PPLH0	R/W		XXXXXXXX$_B$
30_H	Reload register L	PPLL1	R/W		XXXXXXXX$_B$
31_H	Reload resister H	PPLH1	R/W		XXXXXXXX$_B$
32_H	Reload register L	PPLL2	R/W		XXXXXXXX$_B$
33_H	Reload register H	PPLH2	R/W		XXXXXXXX$_B$
34_H	Reload register L	PPLL3	R/W		XXXXXXXX$_B$
35_H	Reload register H	PPLH3	R/W		XXXXXXXX$_B$
36_H	Reload register L	PPLL4	R/W		XXXXXXXX$_B$
37_H	Reload register H	PPLH4	R/W		XXXXXXXX$_B$
38_H	Reload register L	PPLL5	R/W		XXXXXXXX$_B$
39_H	Reload register H	PPLH5	R/W		XXXXXXXX$_B$
$3A_H$	PPG0 operating mode control register	PPGC0	R/W		0 X 0 0 0XX 1_B
$3B_H$	PPG1 operating mode control register	PPGC1	R/W		0 X 0 0 0 0 0 1_B
$3C_H$	PPG2 operating mode control register	PPGC2	R/W		0 X 0 0 0XX 1_B
$3D_H$	PPG3 operating mode control register	PPGC3	R/W		0 X 0 0 0 0 0 1_B
$3E_H$	PPG4 operating mode control register	PPGC4	R/W		0 X 0 0 0XX 1_B
$3F_H$	PPG5 operating mode control register	PPGC5	R/W		0 X 0 0 0 0 0 1_B
40_H	PPG0, 1 output control register	PPG01	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0_B
41_H	(Reserved area)				
42_H	PPG2, 3 output control register	PPG23	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0_B
43_H	(Reserved area)				

(Continued)

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Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
44H	PPG4, 5 output control register	PPG45	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0B
45H	(Reserved area)				
46H	Control status register	ADCS1	R/W	A/Dconverter	0 0 0 0 0 0 0 0B
47H		ADCS2	R/W		0 0 0 0 0 0 0 0B
48H	Data register	ADCR1	R		XXXXXXXXB
49H		ADCR2	R		0 0 0 0 0 XXXB
4AH	Output compare register (ch0) lower digits	OCCP0	R/W	16-bit output timer output compare (ch0 to ch5)	0 0 0 0 0 0 0 0B
4BH	Output compare register (ch0) upper digits				0 0 0 0 0 0 0 0B
4CH	Output compare register (ch1) lower digits	OCCP1	R/W		0 0 0 0 0 0 0 0B
4DH	Output compare register (ch1) upper digits				0 0 0 0 0 0 0 0B
4EH	Output compare register (ch2) lower digits	OCCP2	R/W		0 0 0 0 0 0 0 0B
4FH	Output compare register (ch2) upper digits				0 0 0 0 0 0 0 0B
50H	Output compare register (ch3) lower digits	OCCP3	R/W		0 0 0 0 0 0 0 0B
51H	Output compare register (ch3) upper digits				0 0 0 0 0 0 0 0B
52H	Output compare register (ch4) lower digits	OCCP4	R/W		0 0 0 0 0 0 0 0B
53H	Output compare register (ch4) upper digits				0 0 0 0 0 0 0 0B
54H	Output compare register (ch5) lower digits	OCCP5	R/W		0 0 0 0 0 0 0 0B
55H	Output compare register (ch5) upper digits				0 0 0 0 0 0 0 0B
56H	Output compare control register (ch0)	OCS0	R/W		0 0 0 0 - - 0 0B
57H	Output compare control register (ch1)	OCS1	R/W		- - - 0 0 0 0 0B
58H	Output compare control register (ch2)	OCS2	R/W		0 0 0 0 - - 0 0B
59H	Output compare control register (ch3)	OCS3	R/W		- - - 0 0 0 0 0B
5AH	Output compare control register (ch4)	OCS4	R/W		0 0 0 0 - - 0 0B
5BH	Output compare control register (ch5)	OCS5	R/W		- - - 0 0 0 0 0B
5CH	Input capture data register (ch0) lower digits	IPCP0	R	16-bit output timer input capture (ch0, ch1)	XXXXXXXXB
5DH	Input capture data register (ch0) upper digits		R		XXXXXXXXB
5EH	Input capture data register (ch1) lower digits	IPCP1	R		XXXXXXXXB
5FH	Input capture data register (ch1) upper digits		R		XXXXXXXXB
60H	Input capture control register	ICS01	R/W		0 0 0 0 0 0 0 0B
61H	(Reserved area)				
62H	Timer counter data register lower digits	TCDT	R/W	16-bit output timer free run timer	0 0 0 0 0 0 0 0B
63H	Timer counter data register upper digits	TCDT	R/W		0 0 0 0 0 0 0 0B
64H	Timer control status register	TCCS	R/W		0 0 0 0 0 0 0 0B
65H	Timer control status register	TCCS	R/W		0 - - 0 0 0 0 0B
66H	Compare clear register lower digits	CPCLR	R/W		XXXXXXXXB
67H	Compare clear register upper digits				XXXXXXXXB

(Continued)

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Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
68H	Up/down count register ch0	UDCR0	R	8/16-bit up/down timer counter	0 0 0 0 0 0 0 0B
69H	Up/down count register ch1	UDCR1	R		0 0 0 0 0 0 0 0B
6AH	Reload/compare register ch0	RCR0	W		0 0 0 0 0 0 0 0B
6BH	Reload/compare register ch1	RCR1	W		0 0 0 0 0 0 0 0B
6CH	Counter control register lower digits ch0	CCRL0	R/W		0 X 0 0 X 0 0 0B
6DH	Counter control register upper digits ch0	CCRH0	R/W		0 0 0 0 0 0 0 0B
6EH	(Reserved area)				
6FH	ROM mirror function select register	ROMM	R/W	ROM mirroring function	- - - - - - 0 1 B
70H	Counter control register lower digits ch1	CCRL1	R/W	8/16-bit up/down timer counter	0 X 0 0 X 0 0 0B
71H	Counter control register upper digits ch1	CCRH1	R/W		- 0 0 0 0 0 0 0B
72H	Counter status register ch0	CSR0	R/W		0 0 0 0 0 0 0 0B
73H	(Reserved area)				
74H	Counter status register ch1	CSR1	R/W	8/16-bit UDC	0 0 0 0 0 0 0 0B
75H	(Reserved area)				
76H*	PWC control status register	PWCSR0	R/W	PWC timer (ch0)	0 0 0 0 0 0 0 0B
77H*					0 0 0 0 0 0 0 XB
78H*	PWC data buffer register	PWCR0	R/W		0 0 0 0 0 0 0 0B
79H*					0 0 0 0 0 0 0 0B
7AH*	PWC control status register	PWCSR1	R/W	PWC timer (ch 1)	0 0 0 0 0 0 0 0B
7BH*					0 0 0 0 0 0 0 XB
7CH*	PWC data buffer register	PWCR1	R/W		0 0 0 0 0 0 0 0B
7DH*					0 0 0 0 0 0 0 0B
7EH*	PWC control status register	PWCSR2	R/W	PWC timer (ch2)	0 0 0 0 0 0 0 0B
7FH*					0 0 0 0 0 0 0 XB
80H*	PWC data buffer register	PWCR2	R/W		0 0 0 0 0 0 0 0B
81H*					0 0 0 0 0 0 0 0B
82H*	Dividing ratio control register	DIVR0	R/W	PWC (ch0)	- - - - - - 0 0B
83H	(Reserved area)				
84H*	Dividing ratio control register	DIVR1	R/W	PWC (ch1)	- - - - - - 0 0B
85H	(Reserved area)				
86H*	Dividing ratio control register	DIVR2	R/W	PWC (ch2)	- - - - - - 0 0B
87H	(Reserved area)				
88H*	Bus status register	IBSR	R	I²C	0 0 0 0 0 0 0 0B
89H*	Bus control register	IBCR	R/W		0 0 0 0 0 0 0 0B
8AH*	Bus clock control register	ICCR	R/W		- - 0 X X X X XB
8BH*	Bus address register	IADR	R/W		- X X X X X X XB
8CH*	Bus data register	IDAR	R/W		XXXXXXXXB
8DH	(Reserved area)				
8EH*	µPG control status register	PGCSR	R/W	µPG	0 0 0 0 0 - - -B
8FH to 9BH	(Disabled)				
9CH	µDMA status register	DSRL	R/W	µDMA	0 0 0 0 0 0 0 0B

(Continued)

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Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
9D$_H$	µDMA status register	DSRH	R/W	µDMA	0 0 0 0 0 0 0 0$_B$
9E$_H$	Program address detection control status resister	PACSR	R/W	Address match detection function	0 0 0 0 0 0 0 0$_B$
9F$_H$	Dilayed interrupt source general/ cancel register	DIRR	R/W	Delayed interruput generator module	- - - - - - - 0$_B$
A0$_H$	Low-power consumption mode control register	LPMCR	R/W	Low-power operation	0 0 0 1 1 0 0 0$_B$
A1$_H$	Clock select register	CKSCR	R/W	low-power operation	1 1 1 1 1 1 0 0$_B$
A2$_H$, A3$_H$	(Reserved area)				
A4$_H$	µDMA stop status register	DSSR	R/W	µDMA	0 0 0 0 0 0 0 0$_B$
A5$_H$	Automatic ready function select register	ARSR	W	External pins	0 0 1 1 - - 0 0$_B$
A6$_H$	External address output control register	HACR	W	External pins	* * * * * * * *$_B$
A7$_H$	Bus control signal control register	EPCR	W	External pins	1 0 0 0 * 1 0 -$_B$
A8$_H$	Watchdog timer control register	WDTC	R/W	Watchdog timer	XXXXX 1 1 1$_B$
A9$_H$	Timebase timer control register	TBTC	R/W	Timebase timer	1 X X 0 0 1 0 0$_B$
AA$_H$	Watch timer control register	WTC	R/W	Watch timer	1 0 0 0 1 0 0 0$_B$
AB$_H$	(Reserved area)				
AC$_H$	µDMA enable area	DERL	R/W	µDMA	0 0 0 0 0 0 0 0$_B$
AD$_H$	µDMA enable area	DERH	R/W	µDMA	0 0 0 0 0 0 0 0$_B$
AE$_H$	Flash memory control status register	FMCR	R/W	Flash memory interface	0 0 0 X 0 0 0 0$_B$
AF$_H$	(Disabled)				
B0$_H$	Interrupt control register 00	ICR00	W, R/W	—	X X X X 0 1 1 1$_B$
B1$_H$	Interrupt control register 01	ICR01	W, R/W	—	X X X X 0 1 1 1$_B$
B2$_H$	Interrupt control register 02	ICR02	W, R/W	—	X X X X 0 1 1 1$_B$
B3$_H$	Interrupt control register 03	ICR03	W, R/W	—	X X X X 0 1 1 1$_B$
B4$_H$	Interrupt control register 04	ICR04	W, R/W	—	X X X X 0 1 1 1$_B$
B5$_H$	Interrupt control register 05	ICR05	W, R/W	—	X X X X 0 1 1 1$_B$
B6$_H$	Interrupt control register 06	ICR06	W, R/W	—	X X X X 0 1 1 1$_B$
B7$_H$	interrupt control register 07	ICR07	W, R/W	—	X X X X 0 1 1 1$_B$
B8$_H$	Interrput control register 08	ICR08	W, R/W	—	X X X X 0 1 1 1$_B$
B9$_H$	Interrupt control register 09	ICR09	W, R/W	—	X X X X 0 1 1 1$_B$
BA$_H$	Interrupt control register 10	ICR10	W, R/W	—	X X X X 0 1 1 1$_B$
BB$_H$	Interrupt control register 11	ICR11	W, R/W	—	X X X X 0 1 1 1$_B$
BC$_H$	Interrupt control register 12	ICR12	W, R/W	—	X X X X 0 1 1 1$_B$
BD$_H$	Interrupt control register 13	ICR13	W, R/W	—	X X X X 0 1 1 1$_B$
BE$_H$	Interrupt control register 14	ICR14	W, R/W	—	X X X X 0 1 1 1$_B$
BF$_H$	Interrupt control register 15	ICR15	W, R/W	—	X X X X 0 1 1 1$_B$
C0$_H$	Chip select area mask register	CMR0	R/W	Chip select function	0 0 0 0 1 1 1 1 $_B$

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(Continued)

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
C1H	Chip select area register	CAR0	R/W	—	1 1 1 1 1 1 1 1B
C2H	Chip select area mask register	CMR1	R/W	—	0 0 0 0 1 1 1 1 B
C3H	Chip select area register	CAR1	R/W	—	1 1 1 1 1 1 1 1B
C4H	Chip select area mask register	CMR2	R/W	—	0 0 0 0 1 1 1 1 B
C5H	Chip select area register	CAR2	R/W	—	1 1 1 1 1 1 1 1B
C6H	Chip select area mask register	CMR3	R/W	—	0 0 0 0 1 1 1 1 B
C7H	Chip select area register	CAR3	R/W	—	1 1 1 1 1 1 1 1B
C8H	Chip select control register	CSCR	R/W	—	- - - - 0 0 0 *B
C9H	Chip select active level register	CALR	R/W	—	- - - - 0 0 0 0B
CAH	Timer control status register	TMCSR	R/W	16-bit reload timer	0 0 0 0 0 0 0 0B
CBH					- - - - 0 0 0 0B
CCH	16-bit timer register/ 16-bit reload register	TMR/TMRLR	R/W		XXXXXXXXB
CDH					
CEH	(Reserved area)				
CFH	PLL output control register	PLLOS	W	Low-power operation	- - - - - - X 0B
D0H to FFH	(External area)				
100H to #H	(RAM area)				
1FF0H	Program address detection resister 0 (Low order address)	PADR0	R/W	Address match detection function	XXXXXXXXB
1FF1H	Program address detection resister 0 (Middle order address)				
1FF2H	Program address detection resister 0 (High order address)				
1FF3H	Program address detection resister 1 (Low order address)	PADR1	R/W	Address match detection function	XXXXXXXXB
1FF4H	Program address detection resister 1 (Middle order address)				
1FF5H	Program address detection resister 1 (High order address)				

* : These registers are only for MB90485 series.
They are used as the reserved area on MB90480 series.

Descriptions for read/write
R/W : Readable and writable
R : Read only
W : Write only

Descriptions for initial value
0 : The initila value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.
- : This bit is not used.
* : The initial value of this bit is “1” or “0”.
The value depends on the mode pin (MD2, MD1 and MD0) .

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■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	µDMA cnannel number	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	—	#08	FFFFDC$_H$	—	—
INT9 instruction	—	#09	FFFFD8$_H$	—	—
Exception	—	#10	FFFFD4$_H$	—	—
INT0	0	#11	FFFFD0$_H$	ICR00	0000B0$_H$
INT1	×	#12	FFFFCC$_H$		
INT2	×	#13	FFFFC8$_H$	ICR01	0000B1$_H$
INT3	×	#14	FFFFC4$_H$		
INT4	×	#15	FFFFC0$_H$	ICR02	0000B2$_H$
INT5	×	#16	FFFFBC$_H$		
INT6	×	#17	FFFFB8$_H$	ICR03	0000B3$_H$
INT7	×	#18	FFFFB4$_H$		
PWC1 (MB90485 series only)	×	#19	FFFFB0$_H$	ICR04	0000B4$_H$
PWC2 (MB90485 series only)	×	#20	FFFFAC$_H$		
PWC0 (MB90485 series only)	1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG0/PPG1 counter borrow	2	#22	FFFFA4$_H$		
PPG2/PPG3 counter borrow	3	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG4/PPG5 counter borrow	4	#24	FFFF9C$_H$		
8/16-bit up/down counter timer compare/underflow/overflow/ inversion (ch0, 1)	×	#25	FFFF98$_H$	ICR07	0000B7$_H$
Input capture (ch0) load	5	#26	FFFF94$_H$		
Input capture (ch1) load	6	#27	FFFF90$_H$	ICR08	0000B8$_H$
Output compare (ch0) match	8	#28	FFFF8C$_H$		
Output compare (ch1) match	9	#29	FFFF88$_H$	ICR09	0000B9$_H$
Output compare (ch2) match	10	#30	FFFF84$_H$		
Output compare (ch3) match	×	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output compare (ch4) match	×	#32	FFFF7C$_H$		
Output compare (ch5) match	×	#33	FFFF78$_H$	ICR11	0000BB$_H$
UART sending completed	11	#34	FFFF74$_H$		
16-bit free run timer overflow, 16-bit reload timer underflow	12	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART receiving compleated	7	#36	FFFF6C$_H$		
SIO1	13	#37	FFFF68$_H$	ICR13	0000BD$_H$
SIO2	14	#38	FFFF64$_H$		

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Interrupt source	µDMA channel number	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
I^2C interface (MB90485 series only)	×	#39	FFFF60H	ICR14	0000BEH
A/D conversion	15	#40	FFFF5CH		
FLASH write/erase, timebase timer,watch timer *	×	#41	FFFF58H	ICR15	0000BFH
Delay interrupt generator module	×	#42	FFFF54H		

×: Interrupt request flag not cleared by the interrupt clear signal.

If there are two interrupt sources for the same interrupt number, the resource will clear both interrupt request flags at the DMAC interrupt clear signal. Therefore if either of the two sources uses the DMAC function, the other interrupt function cannot be used. The interrupt request enable bit for the corresponding resource should be set to “0” and interrupt requests from that resource should be handled by software polling.

* : Caution : The FLASH write/erase, timebase timer, and watch timer cannot be used at the same time.

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■ PERIPHERAL RESOURCES

1. I/O Ports

The I/O ports perform the functions of either sending data from the CPU to the I/O pins, or loading information from the I/O into the CPU, according to the setting of the corresponding port register (PDR) . The input/output direction of each I/O pin can be set in individual bit units by the port direction register (DDR) for each port. The MB90480/485 series has 84 input/output pins. The I/O ports are port 0 through port A.

(1) Port Data Registers

	7	6	5	4	3	2	1	0	Initial value	Access
PDR0 Address : 000000H	P07	P06	P05	P04	P03	P02	P01	P00	Undefined	R/W*1
PDR1 Address : 000001H	P17	P16	P15	P14	P13	P12	P11	P10	Undefined	R/W*1
PDR2 Address : 000002H	P27	P26	P25	P24	P23	P22	P21	P20	Undefined	R/W*1
PDR3 Address : 000003H	P37	P36	P35	P34	P33	P32	P31	P30	Undefined	R/W*1
PDR4 Address : 000004H	P47	P46	P45	P44	P43	P42	P41	P40	Undefined	R/W*1
PDR5 Address : 000005H	P57	P56	P55	P54	P53	P52	P51	P50	Undefined	R/W*1
PDR6 Address : 000006H	P67	P66	P65	P64	P63	P62	P61	P60	Undefined	R/W*1
PDR7 Address : 000007H	P77	P76	P75	P74	P73	P72	P71	P70	Undefined*2	R/W*1
PDR8 Address : 000008H	P87	P86	P85	P84	P83	P82	P81	P80	Undefined	R/W*1
PDR9 Address : 000009H	P97	P96	P95	P94	P93	P92	P91	P90	Undefined	R/W*1
PDRA Address : 00000AH	—	—	—	—	PA3	PA2	PA1	PA0	Undefined	R/W*1

*1 : The R/W indication for I/O ports is somewhat different than R/W access to memory, and involves the following operations.

- Input mode
  Read : Reads the corresponding siganl pin level.
  Write : Writes to the output latch.
- Output mode
  Read : Reads the value from the data register latch.
  Write : Outputs the value to the corresponding signal pin.

*2 : The initial value of this bit is “11XXXXXXB” on MB90485 series.

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(2) Port Direction Registers

	7	6	5	4	3	2	1	0	Initial value	Access
DDR0 Address : 000010_H	D07	D06	D05	D04	D03	D02	D01	D 00	00000000_B	R/W
DDR1 Address : 000011_H	D17	D16	D15	D14	D13	D12	D11	D10	00000000_B	R/W
DDR2 Address : 000012_H	D27	D26	D25	D24	D23	D22	D21	D20	00000000_B	R/W
DDR3 Address : 000013_H	D37	D36	D35	D34	D33	D32	D31	D30	00000000_B	R/W
DDR4 Address : 000014_H	D47	D46	D45	D44	D43	D42	D41	D40	00000000_B	R/W
DDR5 Address : 000015_H	D57	D56	D55	D54	D53	D52	D51	D50	00000000_B	R/W
DDR6 Address : 000016_H	D67	D66	D65	D64	D63	D62	D61	D60	00000000_B	R/W
DDR7 Address : 000017_H	D77*1	D76*1	D75	D74	D73	D72	D71	D70	00000000_B*2	R/W
DDR8 Address : 000018_H	D87	D86	D85	D84	D83	D82	D81	D80	00000000_B	R/W
DDR9 Address : 000019_H	D97	D96	D95	D94	D93	D92	D91	D90	00000000_B	R/W
DDRA Address : $00001A_H$	—	—	—	—	DA3	DA2	DA1	DA0	- - - - 0000_B	R/W

*1 : The value is set to "—" on MB90485 series only.

*2 : The initial value of this bit is "$XX000000_B$" on MB90485 series only.

- When a set of pins is functioning as a port, the corresponding signal pins are controlled as follows.
  0 : Input mode
  1 : Output mode Reset to "0".

Notes :
- When any of these register are accessed using a read-modify-write type instruction (such as a bit set instruction) , the bit specified in the instruction will be set to the indicated value. However, the contents of output registers corresponding to any other bits having input settings will be rewritten to the input values of those pins at that time.
  For this reason, when changing any pin that has been used for input to output, first write the desired value to the PDR register before setting the DDR register for output.
- P76, P77 (MB90485 series only)
  This port has no DDR. To use P77, P76 and I^2C pins, set the PDR value to "1" so that port data remains enabled (to use P77 adn P76 for general purposes, disable I^2C) . The port is an open drain output (with no Pch) .
  To use it as an input port, therefore, set the PDR to "1" to turn off the output trangistor and add a pull-up resistor to the external output.

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(3) Port Input Resistance Registers

	7	6	5	4	3	2	1	0	Initial value	Access
RDR0 Address : 00001C$_H$	RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	00000000$_B$	R/W
RDR1 Address : 00001D$_H$	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	00000000$_B$	R/W

These registers control the use of pull-up resistance in input mode.
0 : No pull-up resistance in input mode.
1 : With pull-up resistance in input mode.

In output mode, these registers have no significance (no pull-up resistance) . Input/output mode settings are controlled by the port direction (DDR) registers.
In case of a stop (SPL = 1) , no pull-up resistance is applied (high impedance) . This function is prohibited when an external bus is used. Do not write to these registers.

(4) Port Output Pin Registers

	7	6	5	4	3	2	1	0	Initial value	Access
ODR7 Address : 00001E$_H$	OD77*1	OD76*1	OD75	OD74	OD73	OD72	OD71	OD70	00000000$_B$*2	R/W
ODR4 Address : 00001B$_H$	OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40	00000000$_B$	R/W

*1 : The value is set to "—" on MB90485 series only.

*2 : The initial value of this bit is "XX000000$_B$" on MB90485 series only.

These registers control open drain settings in output mode.
0 : Standard output port functions in output mode.
1 : Open drain output port in output mode.

In input mode these registers have no significance (Hi-Z output) . Input/output mode settings are controlled by direction (DDR) registers. This function is prohibited when an exteral bus is used. Do not write to these registers.

(5) Analog Input Enable Register

	7	6	5	4	3	2	1	0	Initial value	Access
ADER Address : 00001F$_H$	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111$_B$	R/W

This resister controls the port 6 pins as follows.
0 : Port input/output mode.
1 : Analog input mode. The default value at reset is all "1".

(6) Up-down Timer Input Enable Register

	7	6	5	4	3	2	1	0	Initial value	Access
UDER Address : 00000B$_H$	—	—	UDE5	UDE4	UDE3	UDE2	UDE1	UDE0	XX000000$_B$	R/W

This register controls the port 3 pins as follows.
0 : Port input mode.
1 : Up/down timer input mode.The default value at reset is "0".

The MB90480/485 series uses the following setting values : UDE0 : P30/AIN0, UDE1 : P31/BIN0/UDE2 : P32/ZIN0,
UDE3 : P33/AIN1, UDE4 : P34/BIN1, UDE5 : P35/ZIN1

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2. UART

The UART is a serial I/O port for asynchronous (start-stop synchronized) communication as well as CLK synchronized communication.

- Full duplex double buffer
- Transfer modes : asynchronous (start-stop synchronized) , or CLK synchronized (no start bit or stop bit) .
- Multi-processor mode supported.
- Embedded proprietary baud rate generator
  Asynchronous : 76923/38461/19230/9615/500 K/250 Kbps
  CLK synchronized : 16 M/8 M/4 M/2 M/1 M/500 Kbps
- External clock setting available, allows use of any desired baud rate.
- Can use internal clock feed from PPG1.
- Data length : 7-bit (asynchronous normal mode only) or 8-bit.
- Master/slave type communication functions (in multi-processor mode) .
- Error detection functions (parity, framing, overrun)
- Transmission signals are NRZ encorded.
- DMAC supported (for receiving/sending)

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(1) Register List

15 … 8	7 … 0
CDCR	—
SCR	SMR
SSR	SIDR (R)/SODR (W)
← 8 bit →	← 8 bit →

Serial mode register (SMR)

	7	6	5	4	3	2	1	0	
000020H	MD1	MD0	CS2	CS1	CS0	Reserved	SCKE	SOE	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	X	0	0	Initial value

Serial control register (SCR)

	15	14	13	12	11	10	9	8	
000021H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	
	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W	
	0	0	0	0	0	1	0	0	Initial value

Serial I/O register (SIDR/SODR)

	7	6	5	4	3	2	1	0	
000022H	D7	D6	D5	D4	D3	D2	D1	D0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	X	X	X	X	X	X	X	X	Initial value

Serial data register (SSR)

	15	14	13	12	11	10	9	8	
000023H	PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE	
	R	R	R	R	R	R/W	R/W	R/W	
	0	0	0	0	1	0	0	0	Initial value

Communication prescaler control register (CDCR)

	15	14	13	12	11	10	9	8	
000025H	MD	SRST	—	—	DIV3	DIV2	DIV1	DIV0	
	R/W	R/W	—	—	R/W	R/W	R/W	R/W	
	0	0	—	—	0	0	0	0	Initial value

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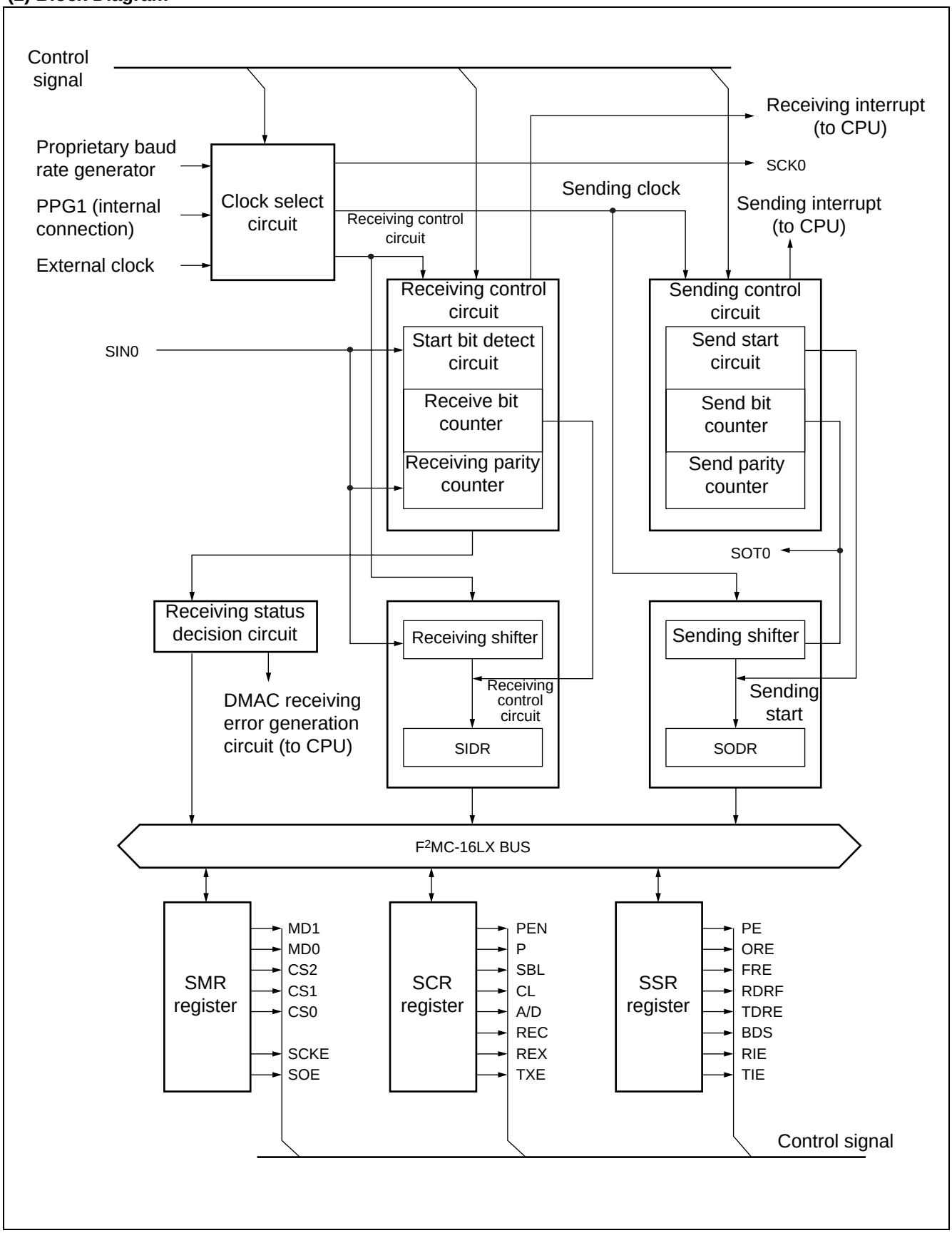
(2) Block Diagram



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3. Expanded I/O Serial Interface

The expanded I/O serial interface is an 8-bit × 1-channel serial I/O interface for clock synchronized data transmission. A selection of LSB-first or MSB-first data transmission is provided.

There are two serial I/O operation modes.

- Internal shift clock mode : Data transmission is synchronized with the internal clock siganl.
- External shift clock mode : Data transmission is synchronized with a clock signal input from the external clock signal pin (SCK) . In this mode the general-purpose port that shares the external clock signal pin (SCK) can be used for transmission according to CPU instructions.

(1) Register List

Serial mode control status register (SMCS)

Address : 000027_H / $00002B_H$

15	14	13	12	11	10	9	8	Initial value
SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	00000010_B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address : 000026_H / $00002A_H$

7	6	5	4	3	2	1	0	
—	—	—	—	MODE	BDS	SOE	SCOE	$----0000_B$
				R/W	R/W	R/W	R/W	

Serial data register (SDR)

Address : 000028_H / $00002C_H$

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX_B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Communication prescaler control register (SDCR0, SDCR1)

Address : 000029_H / $00002D_H$

15	14	13	12	11	10	9	8	
MD	—	—	—	DIV3	DIV2	DIV1	DIV0	$0---0000_B$
R/W	—	—	—	R/W	R/W	R/W	R/W	

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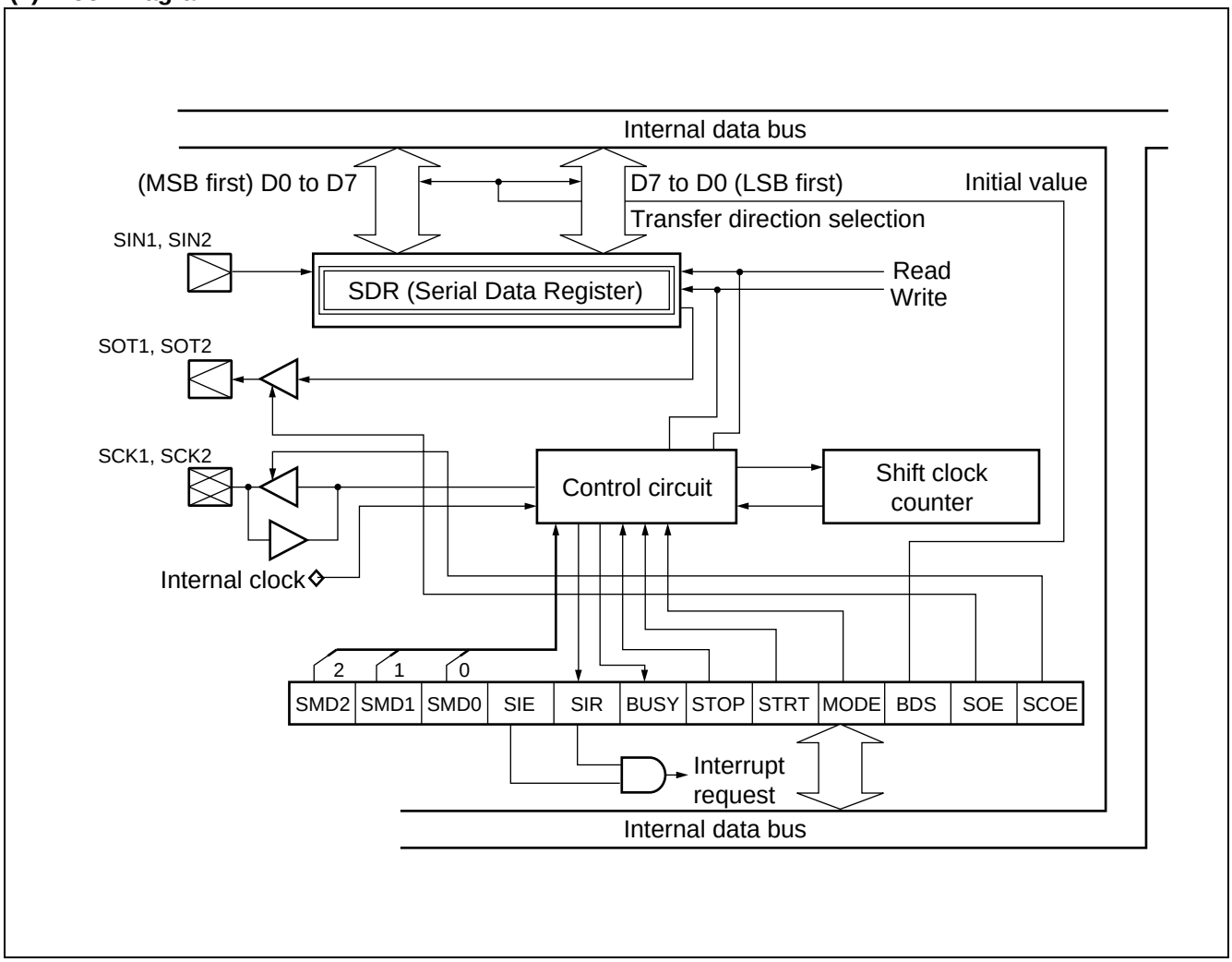
(2) Block Diagram



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4. 8/10-bit A/D Converter

The A/D converter converts analog input voltage input voltages to digital values, and provides the following features.

- Conversion time : minimum 3.68 µs per channel
  (92 machine cycles at 25 MHz machine clock, including sampling time)
- Sampling time : minimum 1.92 µs per channel
  (48 machine cycles at 25 MHz machine clock)
- RC sequential comparison conversion method, with sample & hold circuit.
- 8-bit or 10-bit resolution
- Analog input selection of 8 channels
  Single conversion mode : Conversion from one selected channel.
  Scan conversion mode : Conversion from multiple consecutive channels, programmable selection of up to 8 channels.
  Continuous conversion mode : Repeated conversion of specified channels.
  Stop conversion mode : Conversion from one channel followed by a pause until the next activation.
- At the end of A/D conversion, an A/D conversion completed interrupt request can be generated. The interrupt can be used activate the µDMA in order to transfer the results of A/D conversion to memory for efficient continuous processing.
- The starting factor conversion may be selected from software, external trigger (falling edge) , or timer (rising edge) .

(1) Register List

ADCS2, ADCS1 (Control status register)

ADCS1 bit
Address : 000046H

7	6	5	4	3	2	1	0	
MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	
0	0	0	0	0	0	0	0	←Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←Bit attributes

ADCS2 bit
Address : 000047H

15	14	13	12	11	10	9	8	
BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	
0	0	0	0	0	0	0	0	←Initial value
R/W	R/W	R/W	R/W	R/W	R/W	W	R/W	←Bit attributes

ADCR2, ADCR1 (Data register)

ADCR1 bit
Address : 000048H

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	X	X	←Initial value
R	R	R	R	R	R	R	R	←Bit attributes

ADCR2 bit
Address : 000049H

15	14	13	12	11	10	9	8	
S10	ST1	ST0	CT1	CT0	—	D9	D8	
0	0	0	0	0	X	X	X	←Initial value
R/W	W	W	W	W	R	R	R	←Bit attributes

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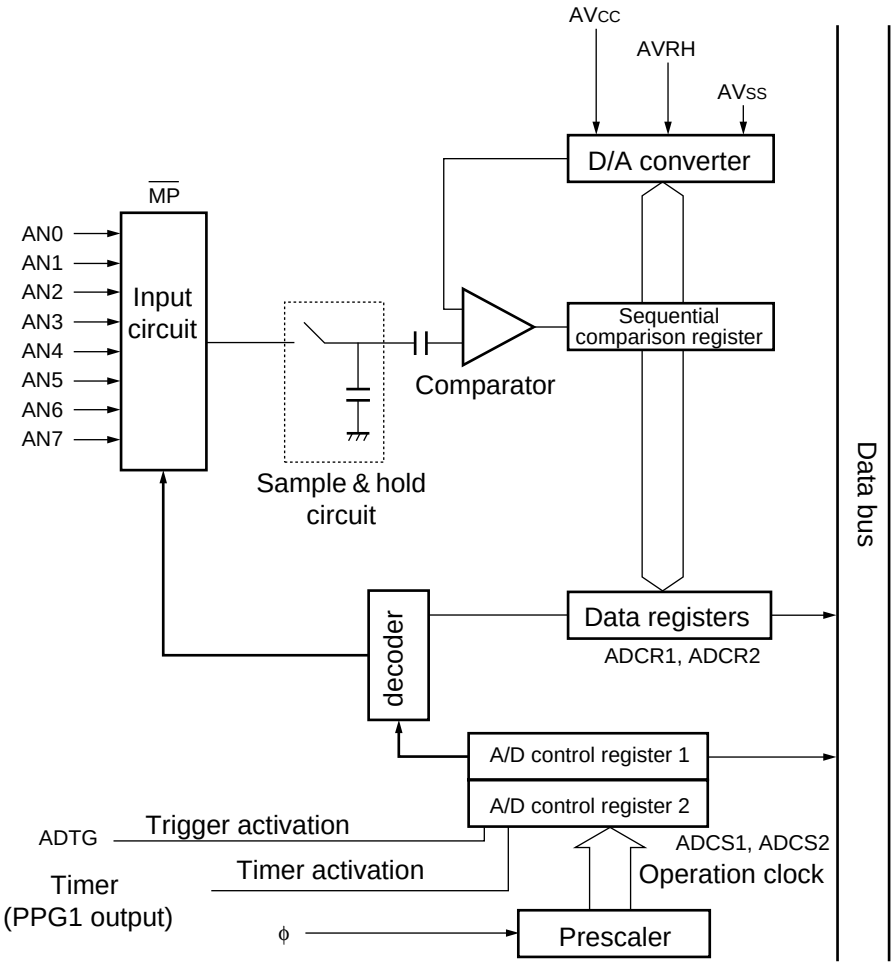
(2) Block Diagram



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5. 8/16-bit PPG

The 8/16-bit PPG is an 8-bit reload timer module that produces a PPG output using a pulse from the timer operation. Hardware resources include 6 × 8-bit down counters, 12 × 8-bit reload timers, 3 × 16-bit control registers, 6 external bus output pins, and 6 interrupt outputs. Note that MB90480/485 series has six channels for 8-bit PPG use, which can also be combined as PPG0 + PPG1, PPG2 + PPG3, and PPG4 + PPG5 to operate as a three-channel 16-bit PPG. The following is a summary of functions.

- 8-bit PPG output 6-channel independent mode : Provides PPG output operation on six independent channels.
- 16-bit PPG output operation mode : Provides 16-bit PPG output on three channels. The six original channels are used in combination as PPG0 + PPG1, PPG2 + PPG3, and PPG4 + PPG5.
- 8 + 8-bit PPG operation mode : Output from PPG0 (PPG2/PPG4) is used as clock input to PPG1 (PPG3/PPG5) to provide to 8-bit PPG output at any desired period length.
- PPG output operation : Produces pulse waves at any desired period and duty ratio. The PPG module can also be used with external cirsuits as a D/A converter.

(1) Register List

PPGC0/PPGC2/PPGC4 (PPG0/PPG2/PPG4 operation mode control register)

	7	6	5	4	3	2	1	0	
00003A$_H$ 00003C$_H$ 00003E$_H$	PEN0	—	PE00	PIE0	PUF0	—	—	Reserved	
	R/W	—	R/W	R/W	R/W	—	—	—	Read/write
	0	X	0	0	0	X	X	1	Initial value

PPGC1/PPGC3/PPGC5 (PPG1/PPG3/PPG5 operation mode control register)

	15	14	13	12	11	10	9	8	
00003B$_H$ 00003D$_H$ 00003F$_H$	PEN1	—	PE10	PIE1	PUF1	MD1	MD0	Reserved	
	R/W	—	R/W	R/W	R/W	R/W	R/W	—	Read/write
	0	X	0	0	0	0	0	1	Initial value

PPG01/PPG23/PPG45 (PPG0 to PPG5 output control register)

	7	6	5	4	3	2	1	0	
000040$_H$ 000042$_H$ 000044$_H$	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	Reserved	Reserved	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	0	0	0	0	0	0	0	0	Initial value

PPLL0 to PPLL5 (Reload register L)

	7	6	5	4	3	2	1	0	
00002E$_H$ 000030$_H$ 000032$_H$ 000034$_H$ 000036$_H$ 000038$_H$	D07	D06	D05	D04	D03	D02	D01	D00	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	X	X	X	X	X	X	X	X	Initial value

PPLH0 to PPLH5 (Reload register H)

	15	14	13	12	11	10	9	8	
00002F$_H$ 000031$_H$ 000033$_H$ 000035$_H$ 000037$_H$ 000039$_H$	D15	D14	D13	D12	D11	D10	D09	D08	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	X	X	X	X	X	X	X	X	Initial value

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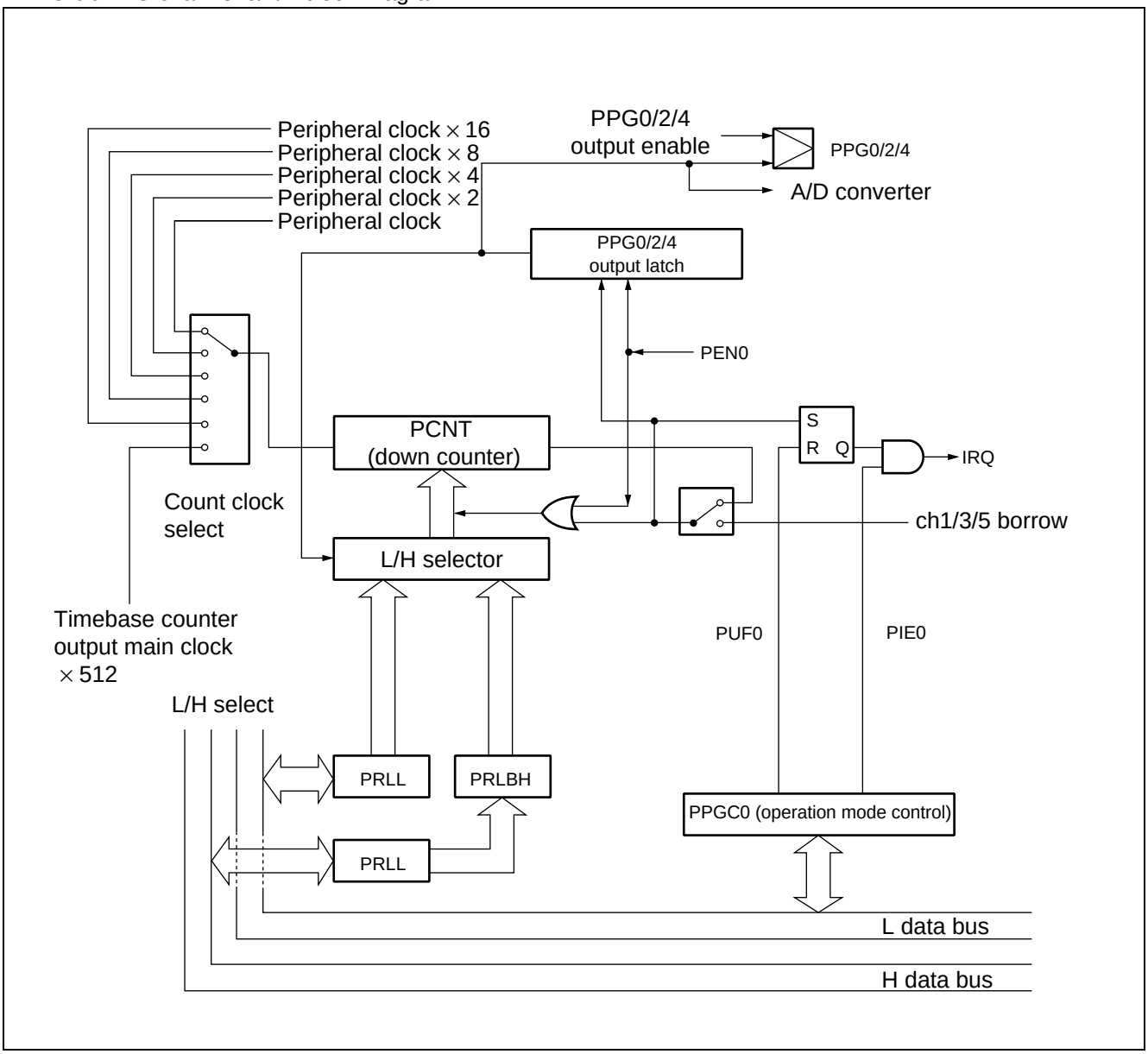
(2) Block Diagram

- 8-bit PPG channel 0/2/4 block Diagram



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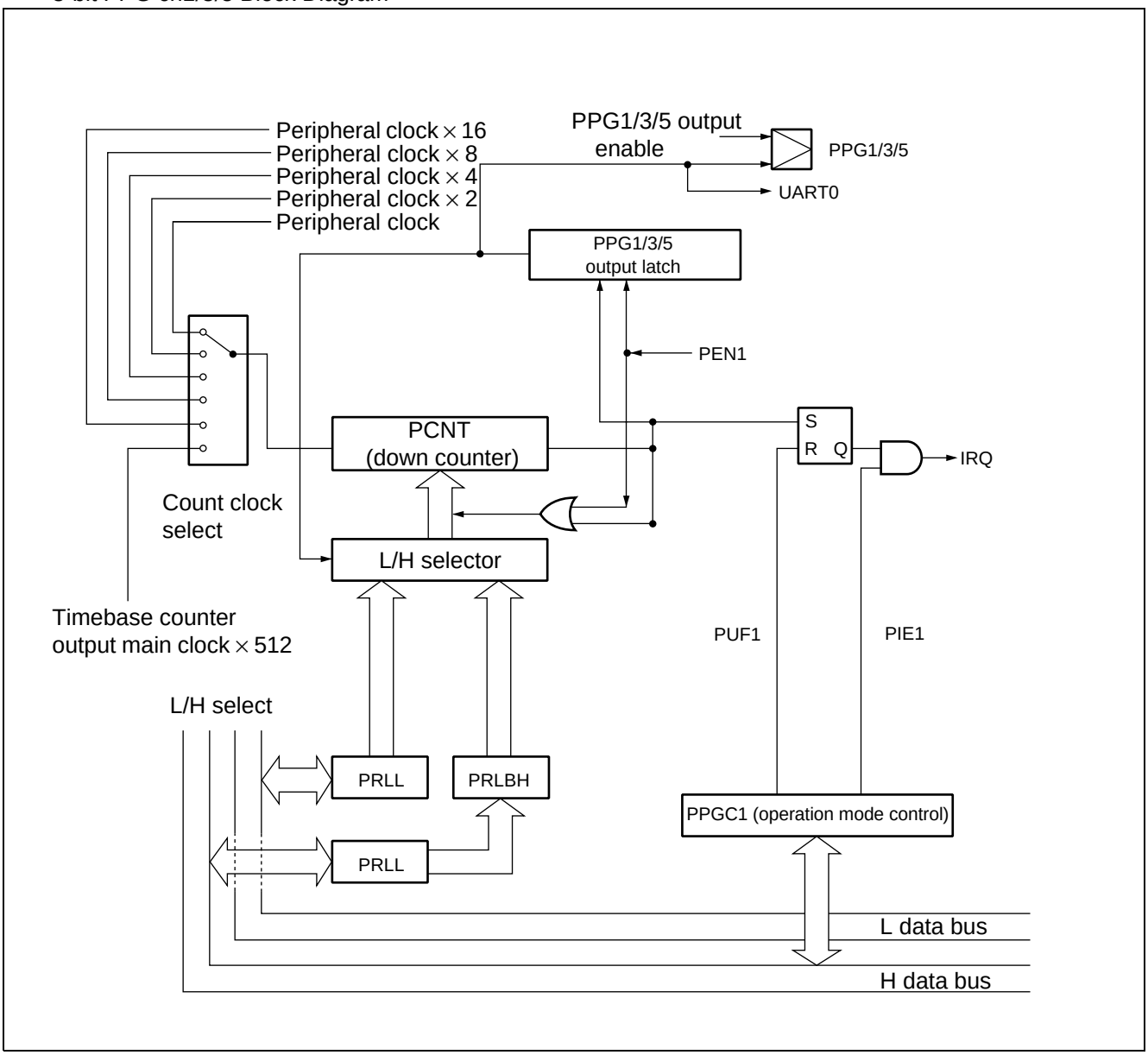
- 8-bit PPG ch1/3/5 Block Diagram



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6. 8/16-bit up/down Counter/Timer

8/16-bit up/down counter/timer consists of up/down counter/timer circuits including six event input pins, two 8-bit up/down counters, two 8-bit reload/compare registers, as well as the related control circuits.

(1) Principal Functions

- 8-bit count register enables counting in the range 0 to 256.
  (In 16-bit × 1 mode, counting is enabled in the range 0 to 65535)
- Count clock selection provides four count modes.

Count modes
- Timer mode
- Up down count mode
- Phase differential count mode (× 2)
- Phase differential count mode (× 8)

- In timer mode, there is a choice of two internal count clock signals.

Count clock (at 16 MHz operation)
- 125 ns (8 MHz : × 2)
- 0.5 µs (2 MHz : × 8)

- In up/down count mode there is a choice of trigger edge detection for the input signal from external pins.

Edge detection
- Falling edge detection
- Rising edge detection
- Both rising/falling edge detection
- Edge detection disabled

- In phase differential count mode, to handle encoder counting for mortors, the encode A-phase, B-phase, and Z-phase are each input, enabling easy and highly accurate counting of angle of rotation, speed of rotation, etc.
- The ZIN pin provides a selection of two functions

ZIN pin
- Counter clear function
- Gate functions

- A compare function and reload function are provided, each for use separately or in combination. Both functions can be activated together for up/down counting in any desired bandwidth.

Compare/reload function
- Compare function (output interrupt at compare events)
- Compare function (output interrupt and clear counter at compare events)
- Reload function (output interrupt and reload at underflow events)
- Compare/reload function (output interrupt and clear counter at compare events, output interrupt and reload at underflow events)
- Compare/reload disabled

- Individual control over interrupts at compare, reload (underflow) and overflow events.
- Count direction flag enables identification of the last previous count direction.
- Interrupt generated when count direction changes.

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(2) Register List

15 … 8	7 … 0
UDCR1	UDCR0
RCR1	RCR0
Reserved area	CSR0
CCRH0	CCRL0
Reserved area	CSR1
CCRH1	CCRL1
8 bit	8 bit

CCRH0 (Counter Control Register High ch0)

Address : 00006D$_H$

15	14	13	12	11	10	9	8
M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 00000000$_B$

CCRH1 (Counter Control Register High ch1)

Address : 000071$_H$

15	14	13	12	11	10	9	8
—	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value -0000000$_B$

CCRL0/1 (Counter Control Register Low ch0/ch1)

Address : 00006C$_H$
Address : 000070$_H$

7	6	5	4	3	2	1	0
UDMS	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0
R/W	W	R/W	R/W	W	R/W	R/W	R/W

Initial value 0X00X000$_B$

CSR0/1 (Counter Status Register ch0/ch1)

Address : 000072$_H$
Address : 000074$_H$

7	6	5	4	3	2	1	0
CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0
R/W	R/W	R/W	R/W	R/W	R/W	R	R

Initial value 00000000$_B$

UDCR0/1 (Up Down Count Register ch0/ch1)

Address : 000069$_H$

15	14	13	12	11	10	9	8
D17	D16	D15	D14	D13	D12	D11	D10
R	R	R	R	R	R	R	R

Initial value 00000000$_B$

Address : 000068$_H$

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00
R	R	R	R	R	R	R	R

Initial value 00000000$_B$

RCR0/1 (Reload/Compare Register ch0/ch1)

Address : 00006B$_H$

15	14	13	12	11	10	9	8
D17	D16	D15	D14	D13	D12	D11	D10
W	W	W	W	W	W	W	W

Initial value 00000000$_B$

Address : 00006A$_H$

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00
W	W	W	W	W	W	W	W

Initial value 00000000$_B$

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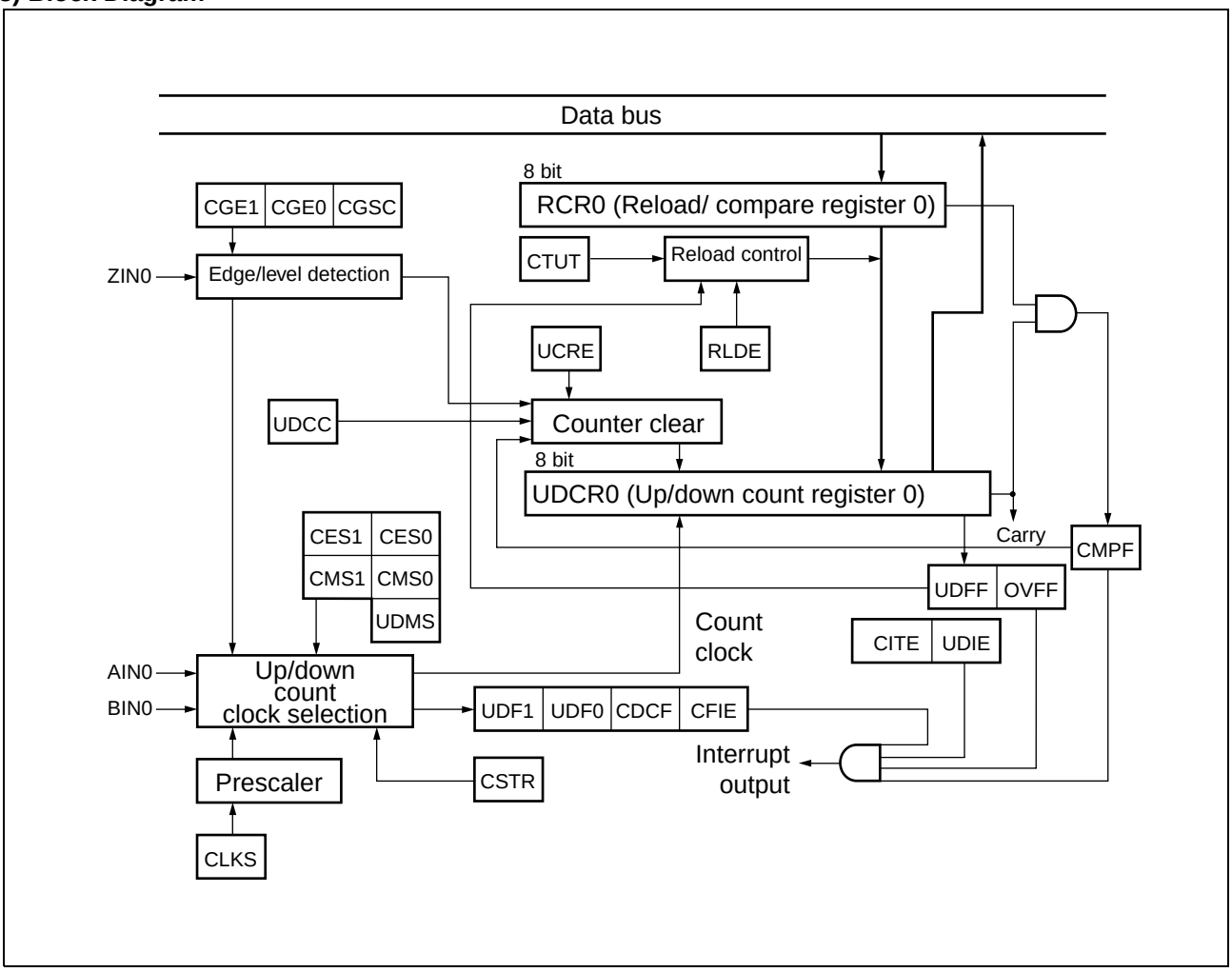
(3) Block Diagram



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7. DTP/External Interrupt

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F²MC-16LX CPU. The DTP receives DMA and interrupt processing requests from external peripherals and passes the requests to the F²MC-16LX CPU to activate the extended intelligent µDMA or interrupt processing.

(1) Detailed Register Descriptions

Interrupt/DTP Enable Register (ENIR : Enable Interrupt Request Register)

ENIR

Address : 00000C$_H$

7	6	5	4	3	2	1	0	Initial value
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000$_B$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Interrupt/DTP Source Register (EIRR : External Interrupt Request Register)

EIRR

Address : 00000D$_H$

15	14	13	12	11	10	9	8	Initial value
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	XXXXXXXX$_B$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Interrupt Level Setting Register (ELVR : External Level Register)

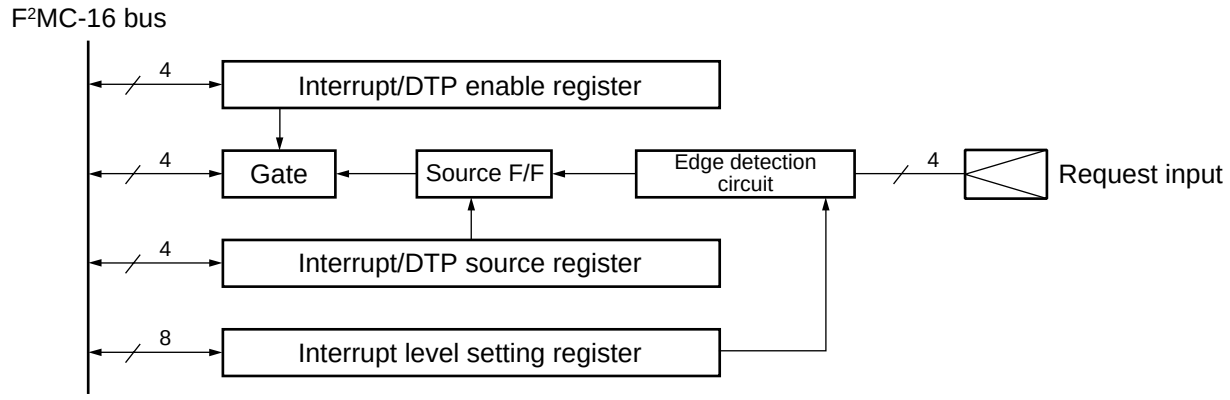
Address : 00000E$_H$

7	6	5	4	3	2	1	0	Initial value
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000$_B$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address : 00000F$_H$

15	14	13	12	11	10	9	8	Initial value
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	00000000$_B$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

(2) Block Diagram



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8. 16-bit Input/Output Timer

The 16-bit input/output timer module is composed of one 16-bit free run timer, six output compare and two input capture modules. These functions can be used to output six independent waveforms based on the 16-bit free run timer, enabling input pilse width measurement and external clock frequency measurement.

- Register List

- 16-bit free run timer

	15 … 0	
000066/67H	CPCLR	Compare-clear register
000062/63H	TCDT	Timer counter data register
000064/65H	TCCS	Control status register

- 16-bit output compare

	15 … 0	
00004A, 4C, 4E, 50, 52, 54H 00004B, 4D, 4F, 51, 53, 55H	OCCP0 to OCCP5	Output compare register
000056, 58, 5AH 000057, 59, 5BH	OCS1/3/5 | OCS0/2/4	Output compare control registers

- 16-bit input capture

	15 … 0	
00005C, 5EH 00005D, 5FH	IPCP0, IPCP1	Input capture data register
000060H	ICS	Input capture control register

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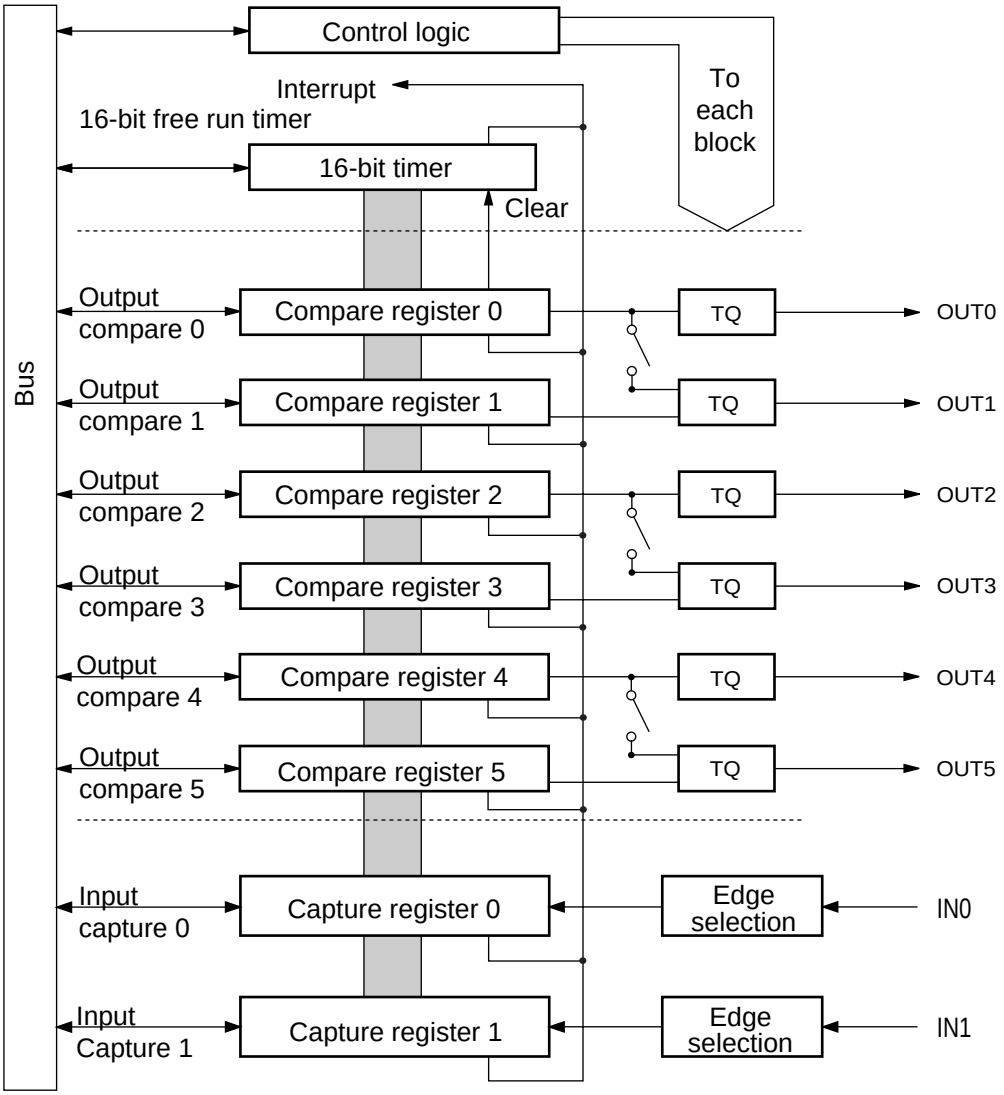
- Block Diagram



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(1) 16-bit Free Run Timer

The 16-bit free run timer is composed of a 16-bit up-down counter and control status register.
The counter value of this timer is used as the base timer for the input capture and output compare.

- The counter operation provides a choice of eight clock types.
- A counter overflow interrupt can be produced.
- A mode setting is available to initialize the counter value whenever the output compare value matches the value in the compare clear register.

- Register List

Compare clear register (CPCLR)

	15	14	13	12	11	10	9	8	Initial value
000067H	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	7	6	5	4	3	2	1	0	Initial value
000066H	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Timer counter data register (TCDT)

	15	14	13	12	11	10	9	8	Initial value
000063H	T15	T14	T13	T12	T11	T10	T09	T08	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	7	6	5	4	3	2	1	0	Initial value
000062H	T07	T06	T05	T04	T03	T02	T01	T00	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Timer control status register (TCCS)

	15	14	13	12	11	10	9	8	Initial value
000065H	ECKE	—	—	MSI2	MSI1	MSI0	ICLR	ICRE	0--00000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	7	6	5	4	3	2	1	0	Initial value
000064H	IVF	IVFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

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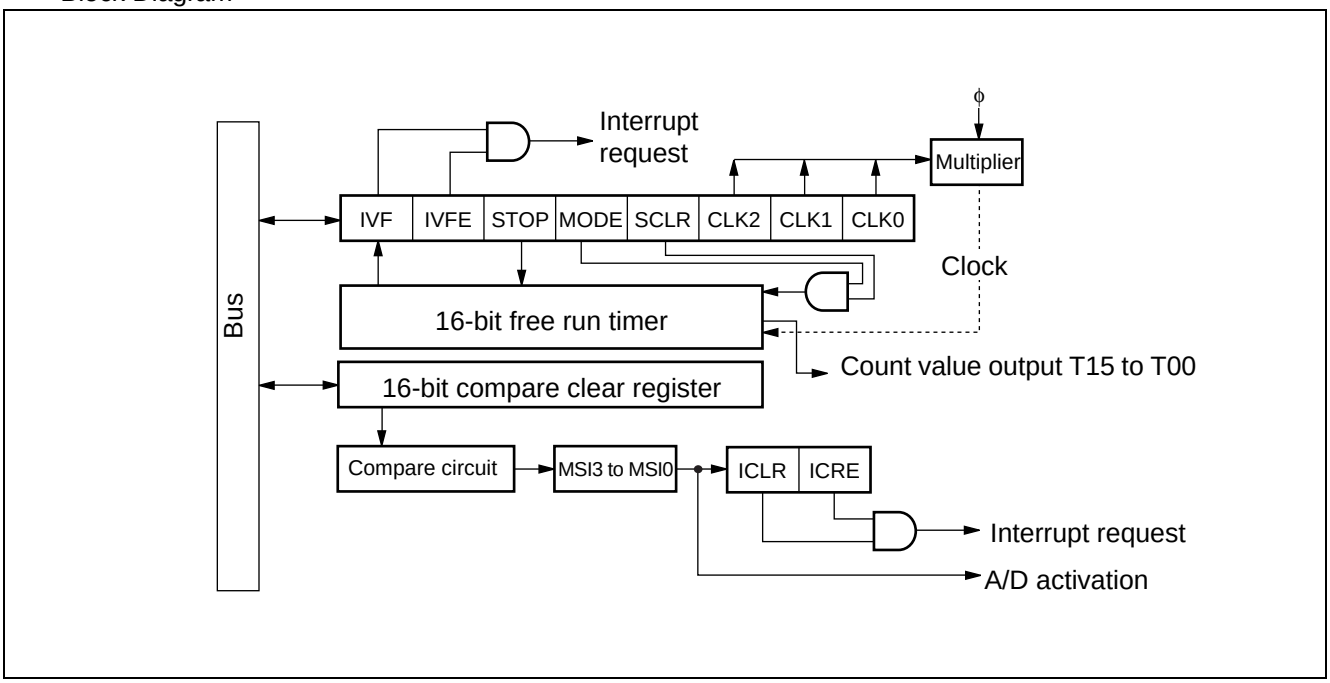
- Block Diagram



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(2) Output Compare

The output compare module is composed of a 16-bit compare register, compare output pin group, and control register. When the value in the compare register in this module matches the 16-bit free run timer, the pin output levels can be inverted and an interrupt generated.

- There are six compare registers in all, each operating independently. A setting is available to allow two compare registers to be used to control output.
- Interrupts can be set in terms of compare match events.

- Register List

Output compare registers (OCCP0 to OCCP5)

	15	14	13	12	11	10	9	8	Initial value
00004B$_H$ 00004D$_H$ 00004F$_H$ 000051$_H$ 000053$_H$ 000055$_H$	C15	C14	C13	C12	C11	C10	C09	C08	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	7	6	5	4	3	2	1	0	Initial value
00004A$_H$ 00004C$_H$ 00004E$_H$ 000050$_H$ 000052$_H$ 000054$_H$	C07	C06	C05	C04	C03	C02	C01	C00	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Output control registers (OCS1/OCS3/OCS5)

	15	14	13	12	11	10	9	8	Initial value
000057$_H$ 000059$_H$ 00005B$_H$	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	---00000$_B$
	—	—	—	R/W	R/W	R/W	R/W	R/W	

Output control registers (OCS0/OCS2/OCS4)

	7	6	5	4	3	2	1	0	Initial values
000056$_H$ 000058$_H$ 00005A$_H$	ICPIC	ICP0	ICE1	ICE0	—	—	CST1	CST0	0000--00$_B$
	R/W	R/W	R/W	R/W	—	—	R/W	R/W	

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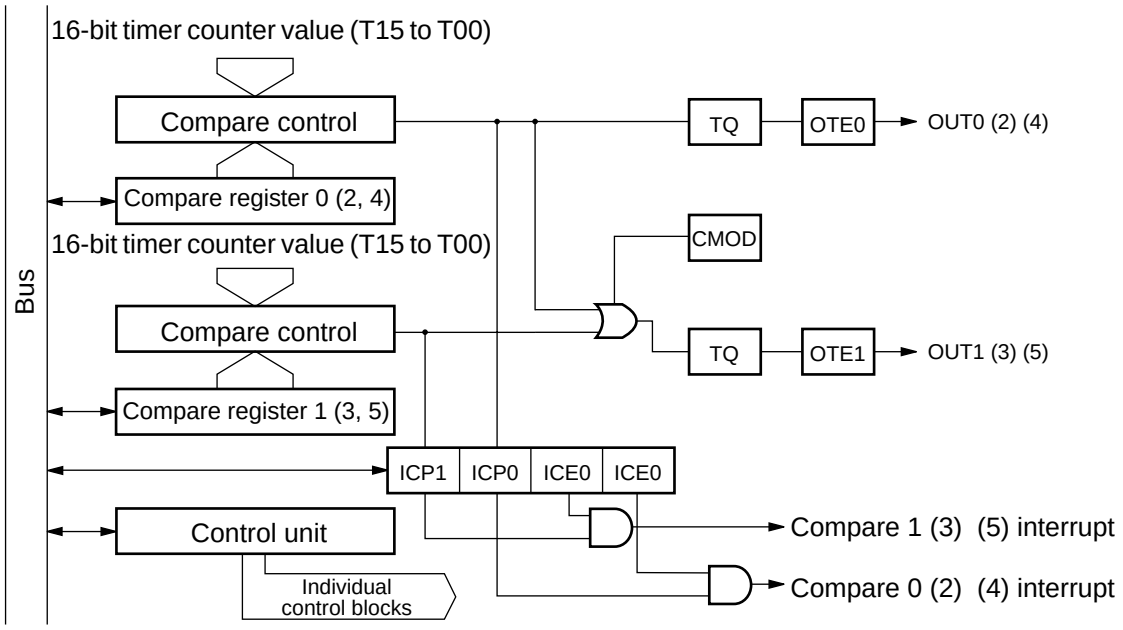
- Block Diagram



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(3) Input Capture

The input capture module performs the functions of detecting the rising edge, falling edge, or both edges of signal input from external circuits, and saving the 16-bit free run timer value at that moment to a register. An interrupt can also be generated at the instant of edge detection.

The input capture module consists of input capture registers and a control register. Each input capture module has its own external input pin.

- Section of three types of valid edge for external input signals.
  Rising edge, falling edge, both edges.
- An interrupt can be generated when a valid edge is detected in the external input signal.

- Register List

Input capture data register (IPCP0, IPCP1)

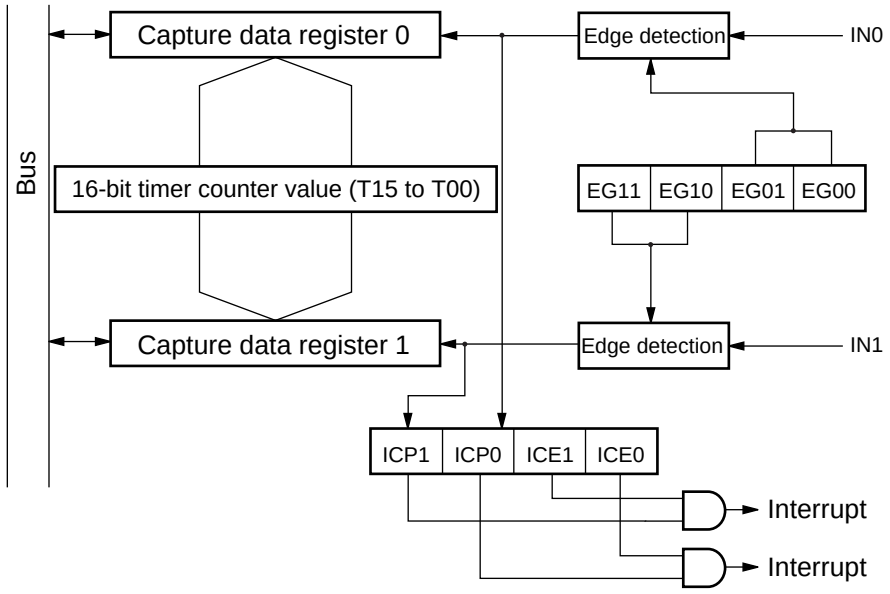
	15	14	13	12	11	10	9	8	Initial value
00005D$_H$ 00005F$_H$	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	XXXXXXXX$_B$
	R	R	R	R	R	R	R	R	

	7	6	5	4	3	2	1	0	Initial value
00005C$_H$ 00005E$_H$	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXX$_B$
	R	R	R	R	R	R	R	R	

Input capture control register (ICS0, ICS1)

	7	6	5	4	3	2	1	0	Initial value
000060$_H$	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Block Diagram



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9. I²C Interface (MB90485 series only)

The I²C interface is a serial I/O port supporting the Inter IC BUS. Serves as a master/slave device on the I²C bus. The I²C interface has the following functions.

- Master/slave transmit/receive
- Arbitration function
- Clock synchronization
- Slave address/general call address detection function
- Forwarding direction ditection function
- Start condition repeated generation and detection
- Bus error detection function

(1) Register List

Bus Status Register (IBSR)

000088H

7	6	5	4	3	2	1	0
BB	RSC	AL	LRB	TRX	AAS	GCA	FBT
R	R	R	R	R	R	R	R

Initial value
0 0 0 0 0 0 0 0B

Bus control register (IBCR)

000089H

15	14	13	12	11	10	9	8
BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
0 0 0 0 0 0 0 0B

Clock control register (ICCR)

00008AH

7	6	5	4	3	2	1	0
—	—	EN	CS4	CS3	CS2	CS1	CS0
—	—	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
- - 0 XXXXXB

Address register (IADR)

00008BH

15	14	13	12	11	10	9	8
—	A6	A5	A4	A3	A2	A1	A0
—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
- XXXXXXXB

Data register (IDAR)

00008CH

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
XXXXXXXXB

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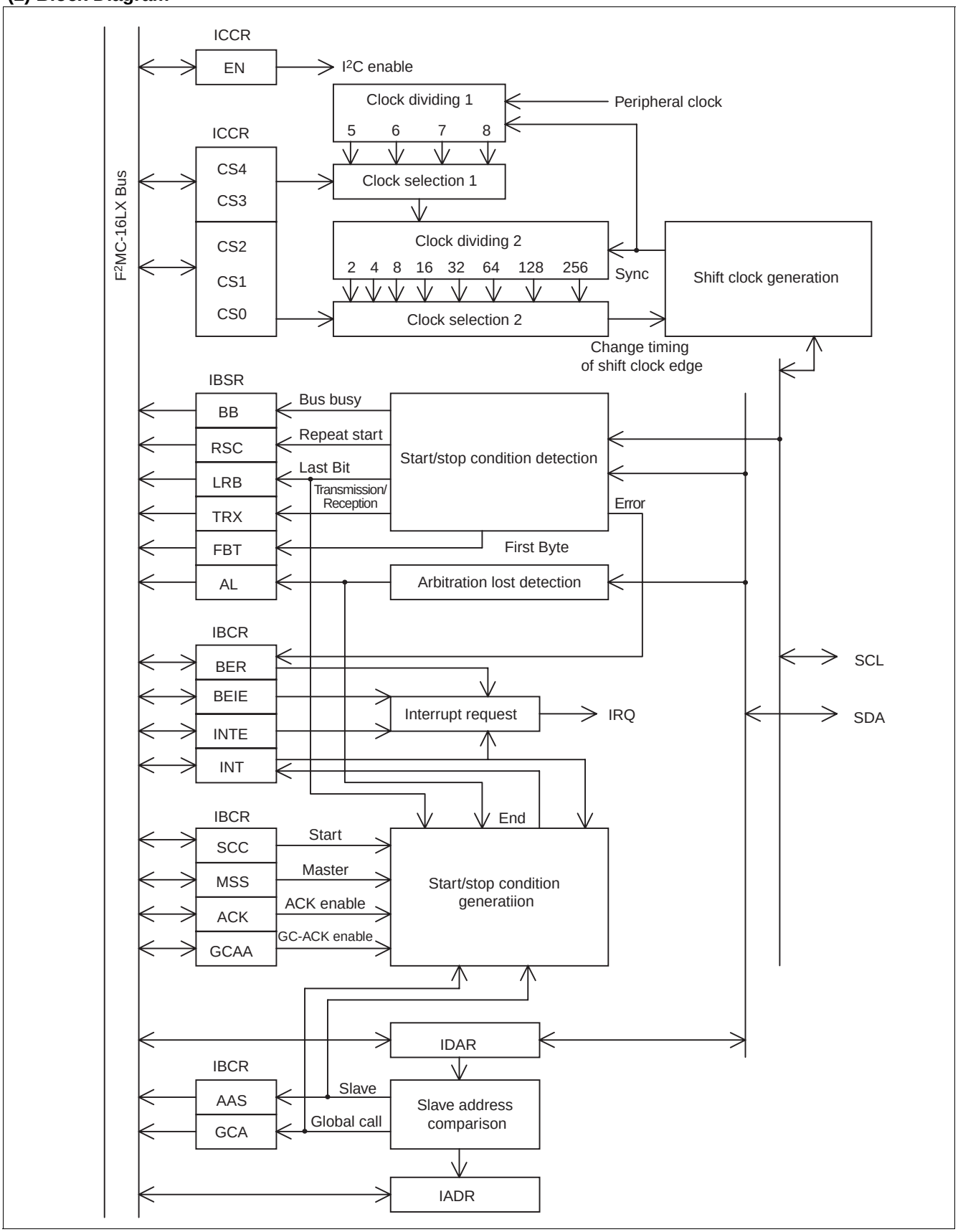
(2) Block Diagram



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10. 16-bit Reload Timer

The 16-bit reload timer provides a choice of functions, including internal clock signals that count down in synchronization with three types of internal clock, as well as an event count mode that counts down at specified edge detection events in pulse signals input from external pins. This timer defines an underflow as a change in count value from 0000_H to $FFFF_H$.Thus an underflow will occur when counting from the value “reload register setting value + 1”. The choice of counting operations includes reload mode, in which the count setting values is reload and counting continues following an underflow event, and one-shot mode, in which an underflow event causes counting to stop. An interrupt can be generated at counter underflow, and the timer is DTC compatible.

(1) Register List

- TMCSR (Timer control status register)

Timer control status register (high) (TMCSR)

	15	14	13	12	11	10	9	8	
$0000CB_H$	—	—	—	—	CSL1	CSL0	MOD2	MOD1	
	—	—	—	—	R/W	R/W	R/W	R/W	Read/Write
	—	—	—	—	0	0	0	0	Initial value

Timer control status register (low) (TMCSR)

	7	6	5	4	3	2	1	0	
$0000CA_H$	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write
	0	0	0	0	0	0	0	0	Initial value

- 16-bit timer register/16-bit reload register

TMR/TMRLR (high)

	15	14	13	12	11	10	9	8	
$0000CD_H$	D15	D14	D13	D12	D11	D10	D09	D08	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write
	X	X	X	X	X	X	X	X	Initial value

TMR/TMRLR (low)

	7	6	5	4	3	2	1	0	
$0000CC_H$	D07	D06	D05	D04	D03	D02	D01	D00	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write
	X	X	X	X	X	X	X	X	Initial value

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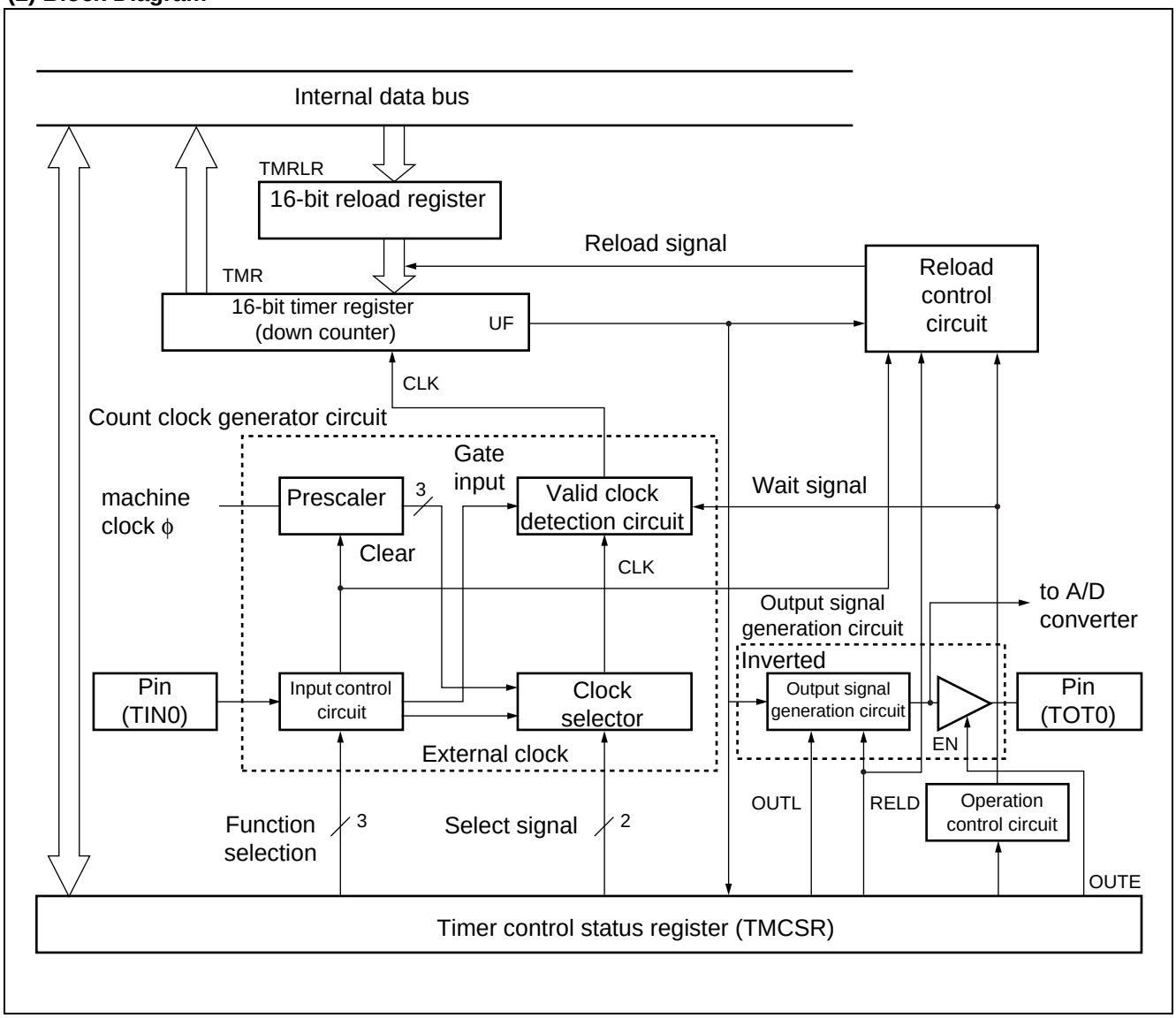
(2) Block Diagram



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11. µPG Timer (MB90485 only)

The µPG timer performs pulse output in response to the external input.

(1) Register List

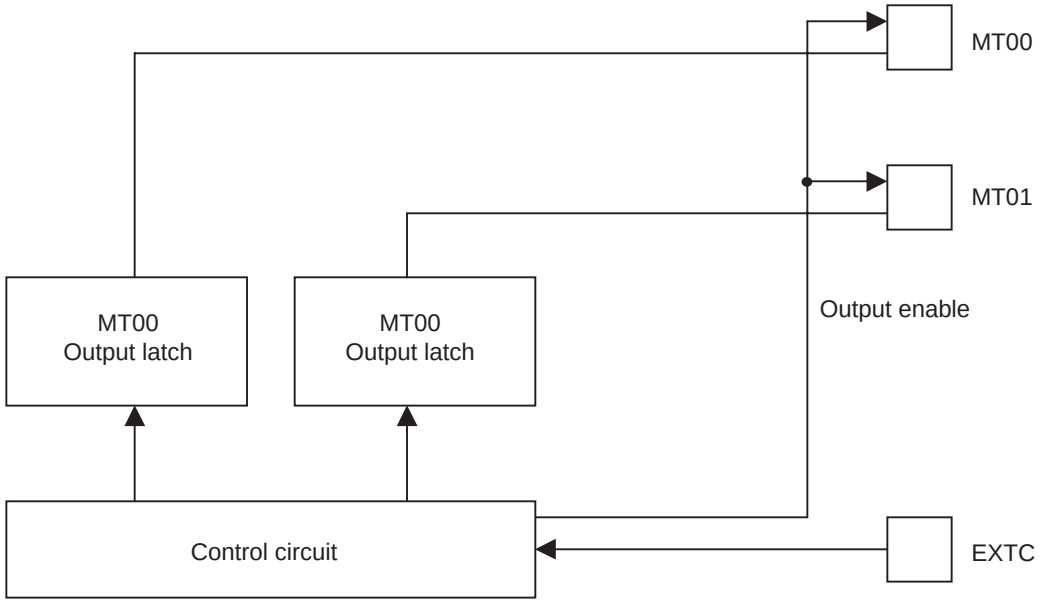
µPG control status register (PGCSR)

00008E$_H$

7	6	5	4	3	2	1	0
PEN0	PE1	PE0	PMT1	PMT0	–	–	–
R/W	R/W	R/W	R/W	R/W	–	–	–

Initial value
0 0 0 0 0 - - - $_B$

(2) Block Diagram



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12. PWC Timer (MB90485 only)

The PWC timer is a 16-bit multifunction up-count timer capable of measuring the pulse width of the input signal. A total of three channels are provided, each consisting of a 16-bit up-count timer, an input pulse divider & divide ratio control register, a measurement input pin, and a 16-bit control register. These components provide the following functions.

Timer function :
- Capable of generating an interrupt request at fixed intervals specified.
- The internal clock used as the reference clock can be selected from among three types.

Pulse width measurement function :
- Measures the time between arbitrary events based on external pulse inputs.
- The internal clock used as the reference clock can be selected from among three types.
- Measurement modes
  - H pulse width (↑ to ↓) /L pulse width (↑ to ↓)
  - Rising cycle (↑ to ↑) /Falling cycle (↓ to ↓)
  - Measurement between edges (↑ or ↓ to ↓ or ↑)
- The 8-bit input divider can be used for division measurement by dividing the input pulse by 22 ns (n = 1, 2, 3, 4) .
- An interrupt can be generated upon completion of measurement.
- One-time measurement or fast measurement can be selected.

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(1) Register list

PWC control status register (PWCSR0 to PWCSR2)

000077H
00007BH
00007FH

15	14	13	12	11	10	9	8
STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	Reserved
R/W	R/W	R	R/W	R/W	R/W	R	–

Initial value
0 0 0 0 0 0 0 X B

PWC control status register (PWCSR0 to PWCSR2)

000076H
00007AH
00007EH

7	6	5	4	3	2	1	0
CKS1	CKS0	PIS1	PIS0	S/C	MOD2	MOD1	MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
0 0 0 0 0 0 0 0 B

PWC data buffer register (PWCR0 to PWCR2)

000079H
00007DH
000081H

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
0 0 0 0 0 0 0 0 B

PWC data buffer register (PWCR0 to PWCR2)

000078H
00007CH
000080H

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
0 0 0 0 0 0 0 0 B

Dividing ratio control register (DIVR0 to DIVR2)

000082H
000084H
000086H

7	6	5	4	3	2	1	0
–	–	–	–	–	–	DIV1	DIV0
–	–	–	–	–	–	R/W	R/W

Initial value
- - - - - - 0 0 B

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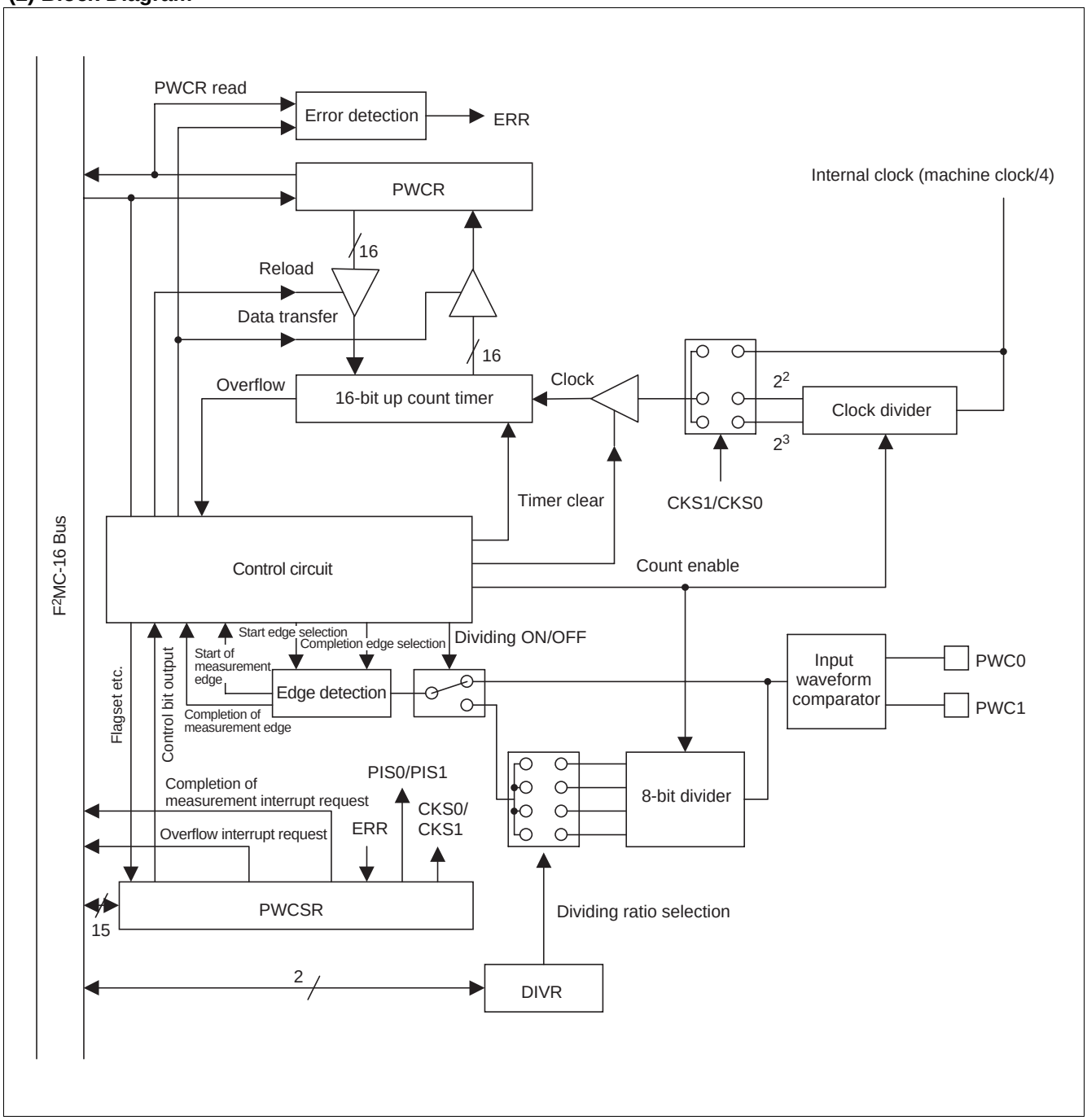
(2) Block Diagram



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13. Watch Timer

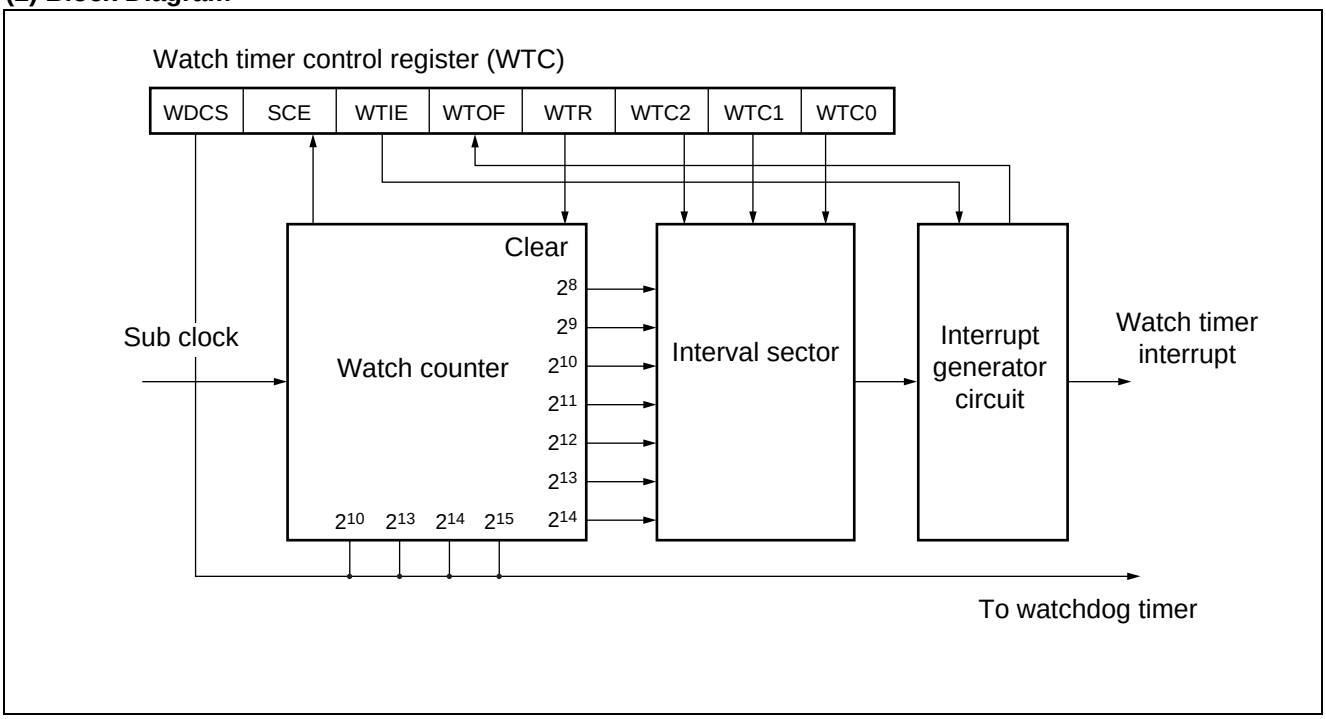
The watch timer is a 15-bit timer using the sub clock. This circuit can generate interrupts at predetermined intervals. Also a setting is available to enable it to be used as the clock source for the watchdog timer.

(1) Register List

Watch timer control register (WTC)

	7	6	5	4	3	2	1	0	
0000AA$_H$	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	1	0	0	0	1	0	0	0	Initial value

(2) Block Diagram



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14. Watchdog timer

The watchdog timer is a 2-bit counter that uses the output from the timebase timer or watch timer as acount clock signal, and will reset the CPU if not cleared within a predetermined time interval after it is activated.

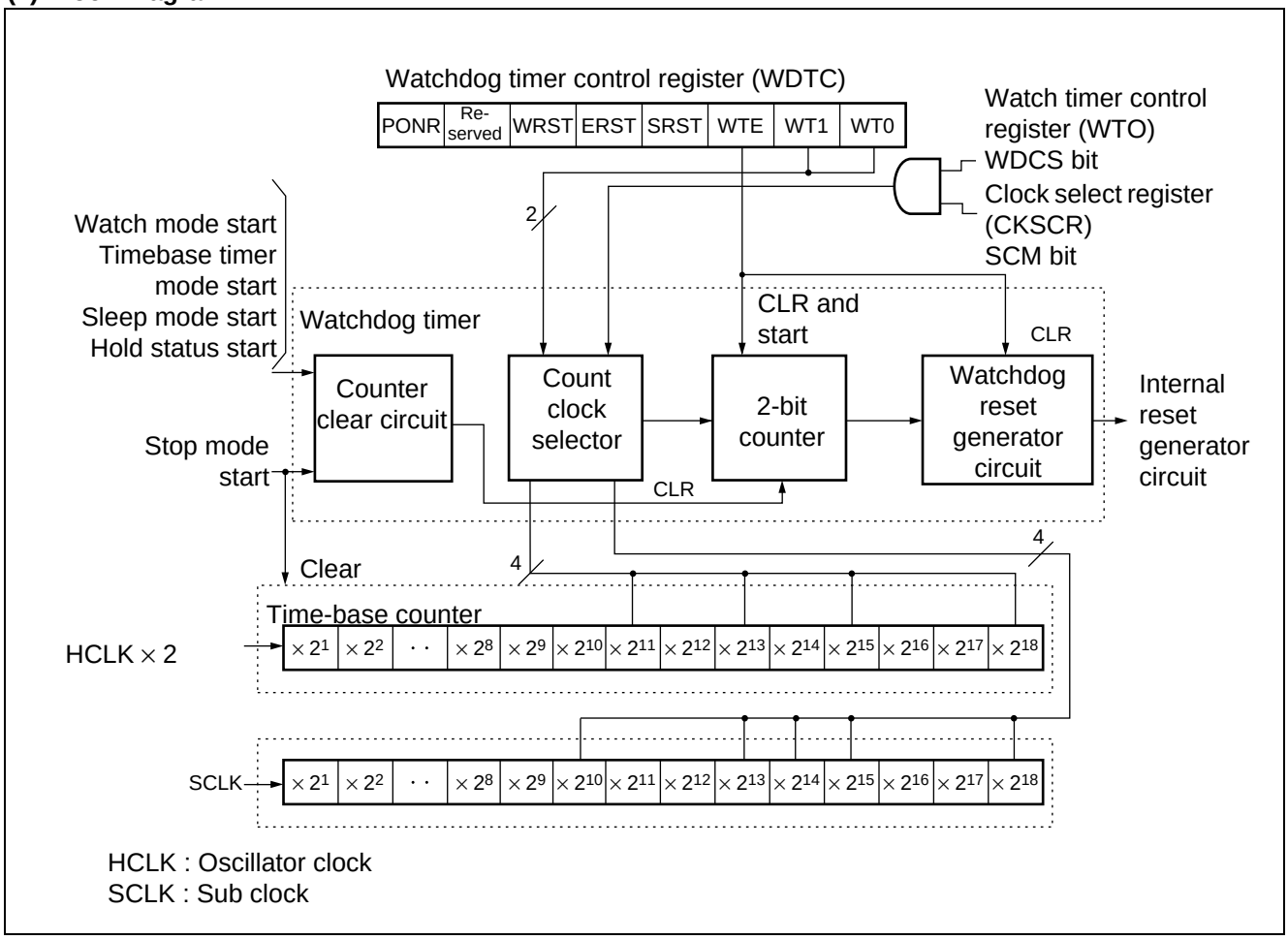
(1) Register List

Watchdog timer control register (WDTC)

0000A8H

7	6	5	4	3	2	1	0	
PONR	Reserved	WRST	ERST	SRST	WTE	WT1	WT0	
R	—	R	R	R	W	W	W	Read/write
X	X	X	X	X	1	1	1	Initial value

(2) Block Diagram



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15. Timebase Timer

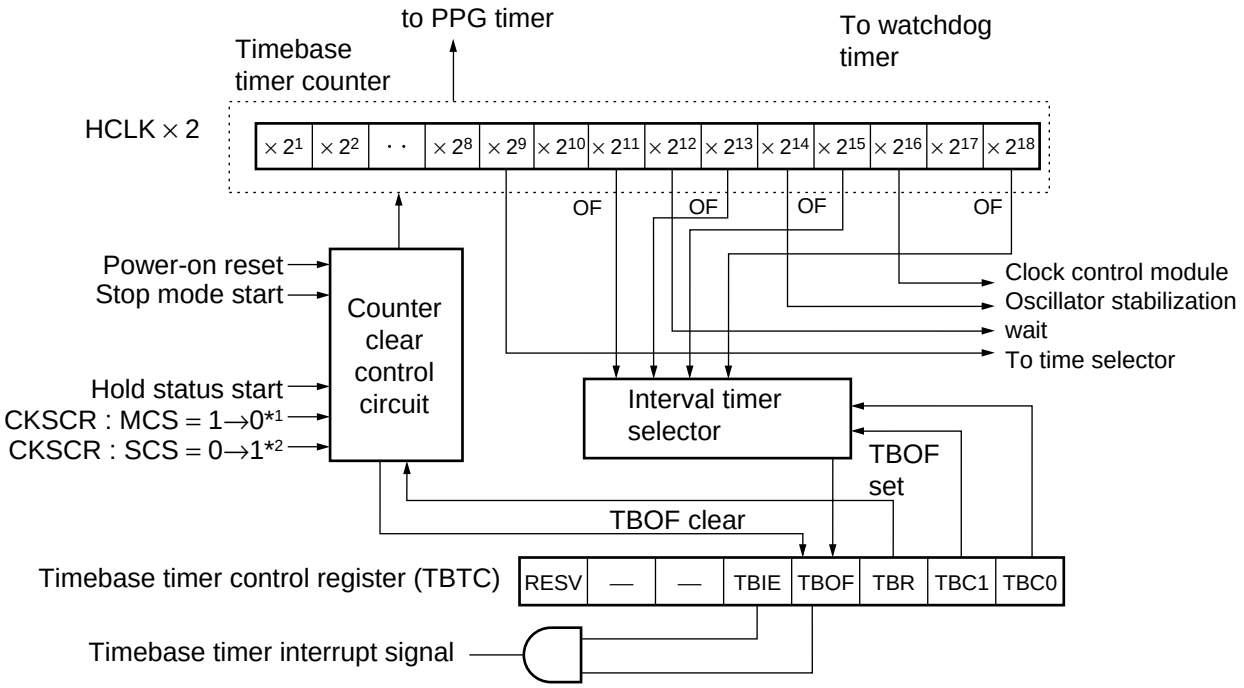
The timebase timer is an 18-bit free run counter (timebase counter) that counts up in synchronization with the internal count clock signal (base oscillator × 2) , and functions as an interval timer with a choice of four types of time intervals. Other functions provided by this module include timer output for the oscillator stabilization wait period, and operating clock signal feed for other timer circuits such as the watchdog timer.

(1) Register List

Timebase timer control register (TBTC)

	15	14	13	12	11	10	9	8	
0000A9H	RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0	
	R/W	—	—	R/W	R/W	W	R/W	R/W	Read/write
	1	X	X	0	0	1	0	0	Initial value

(2) Block Diagram



— : Not used
OF : Overflow
HCLK : Oscillator clock
*1 : Switch machine clock from main clock or sub clock to PLL clock.
*2 : Switch machine clock from sub clock to main clock.

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16. Clock

The clock generator module controls the operation of the internal clock circuits that serve as the operating clock for the CPU and peripheral devices. This internal clock is referred to as the machine clock, and one cycle os refferd to as a machine cycle. Also, the clock signals from the base oscillator are called the oscillator clock, and those from the PLL oscillator are called the PLL clock.

(1) Register List

Clock select register (CKSCR)

	15	14	13	12	11	10	9	8	
0000A1H	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	
	R	R	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	1	1	1	1	1	1	0	0	Initial value

PLL output select register (PLLOS)

	15	14	13	12	11	10	9	8	
0000CFH	—	—	—	—	—	—	—	PLL2	
	—	—	—	—	—	—	W	W	Read/write
	—	—	—	—	—	—	X	0	Initial value

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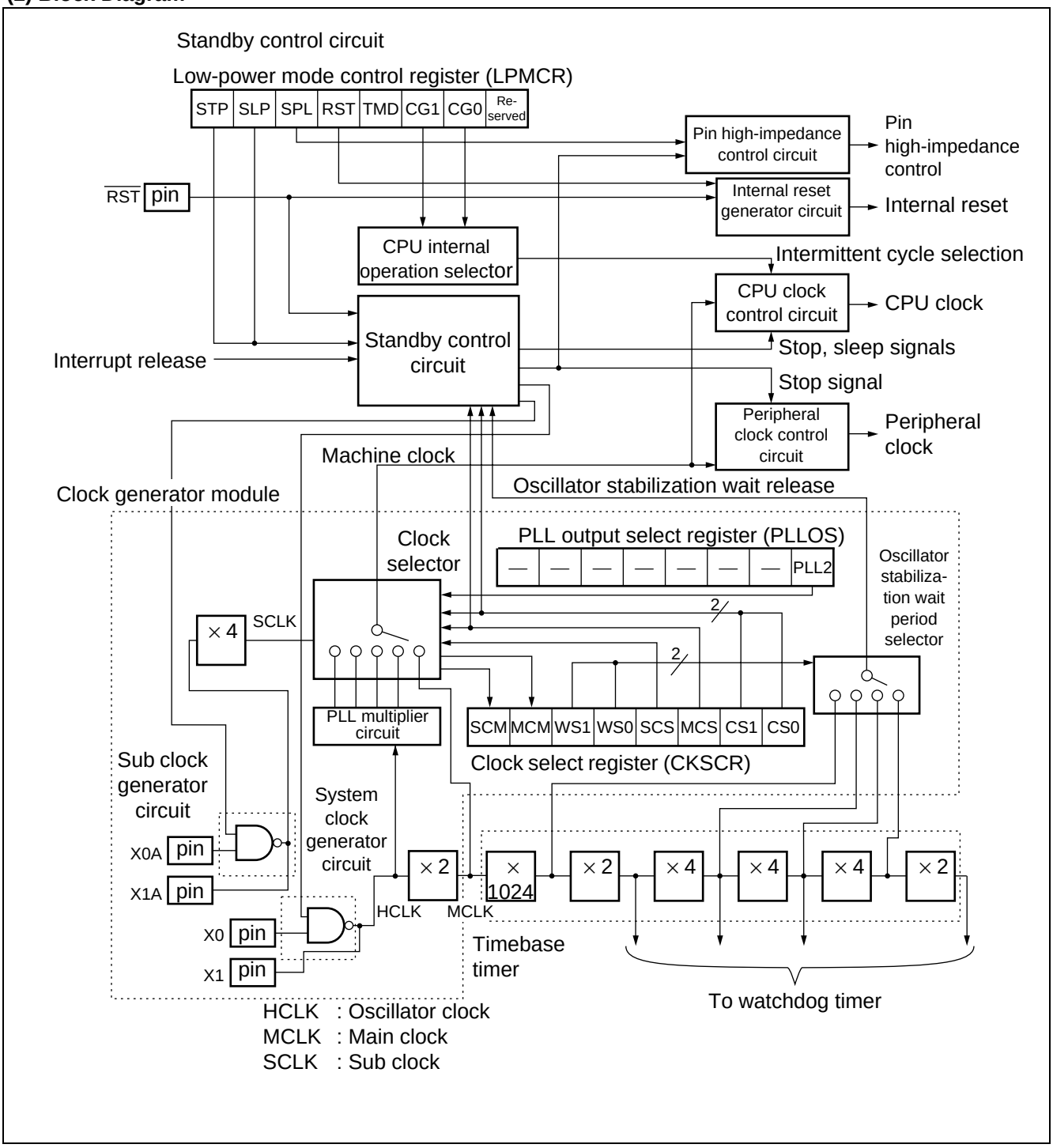
(2) Block Diagram



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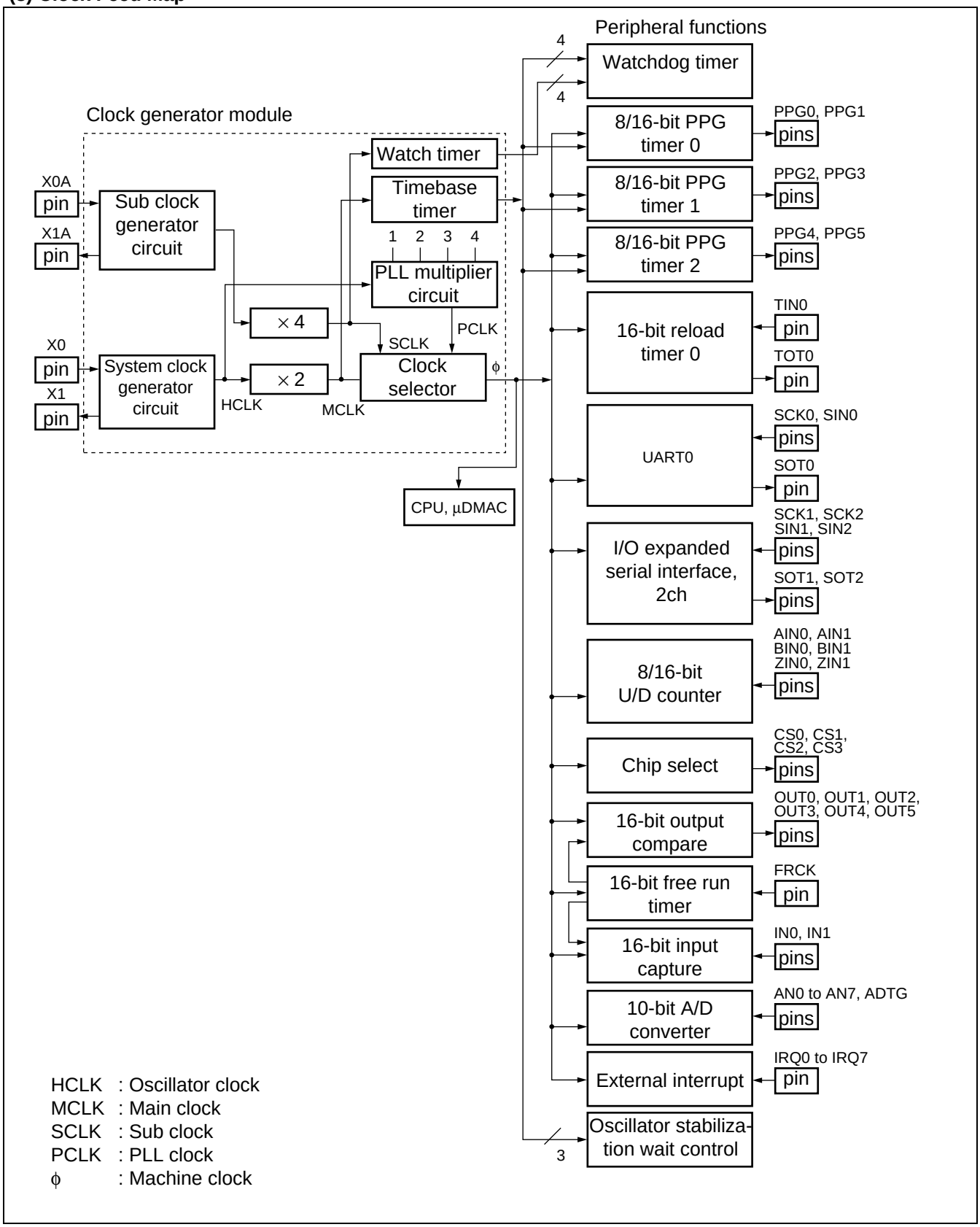
(3) Clock Feed Map



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17. Low-power Consumption Mode

The MB90480/485 series uses operating clock selection and clock operation controls to provide the following CPU operating modes :

- Clock modes
  (PLL clock mode, main clock mode, sub clock mode)
- CPU intermittent operating modes
  (PLL clock intermittent mode, main clock intermittent mode, sub clock intermittent mode)
- Standby modes
  (Sleep mode, timebase timer mode, stop mode, watch mode)

(1) Register List

Low-power mode control register (LPMCR)

	7	6	5	4	3	2	1	0	
0000A0H	STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved	
	W	W	R/W	W	R/W	R/W	R/W	R/W	Read/write
	0	0	0	1	1	0	0	0	Initial value

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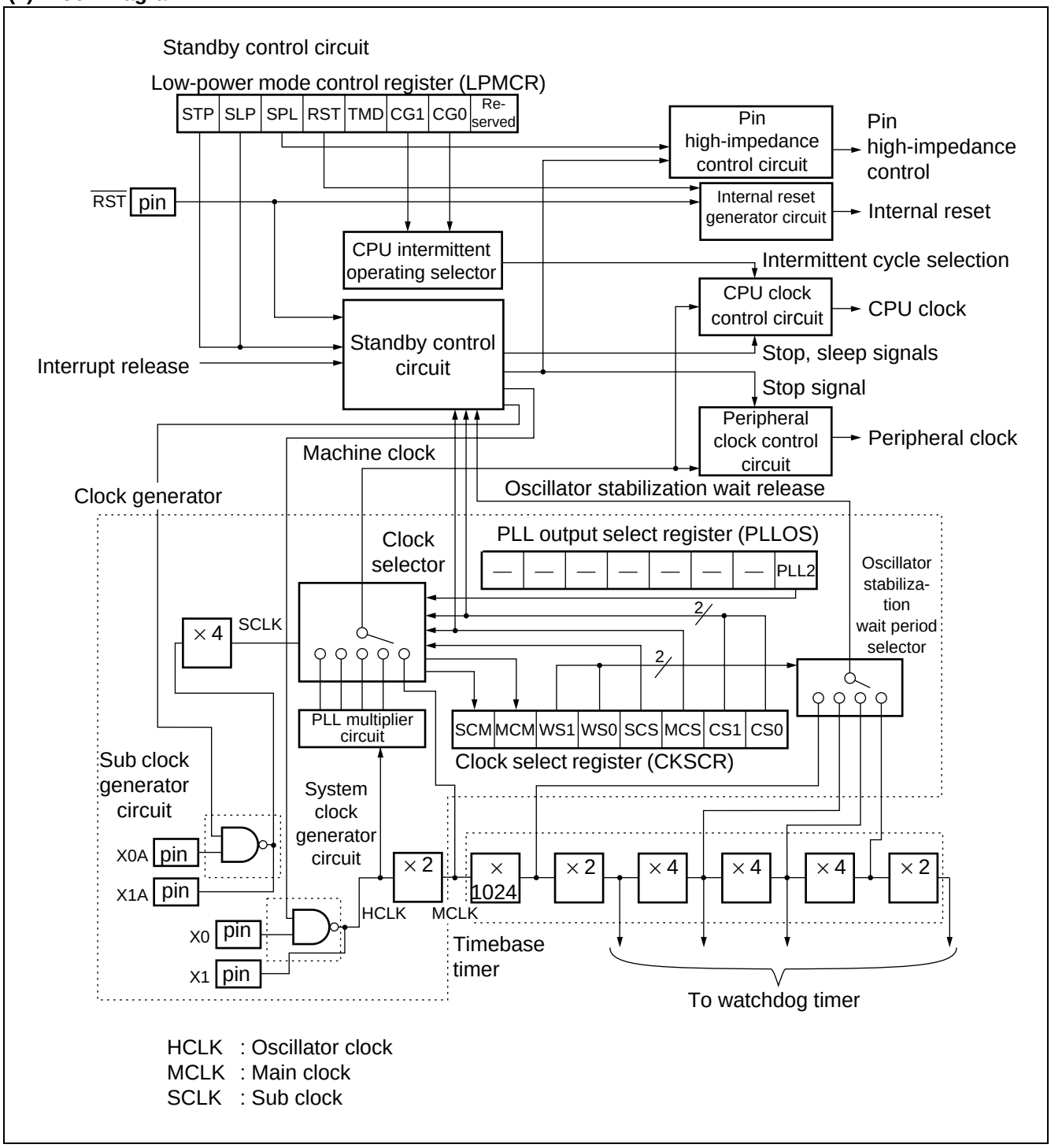
(2) Block Diagram



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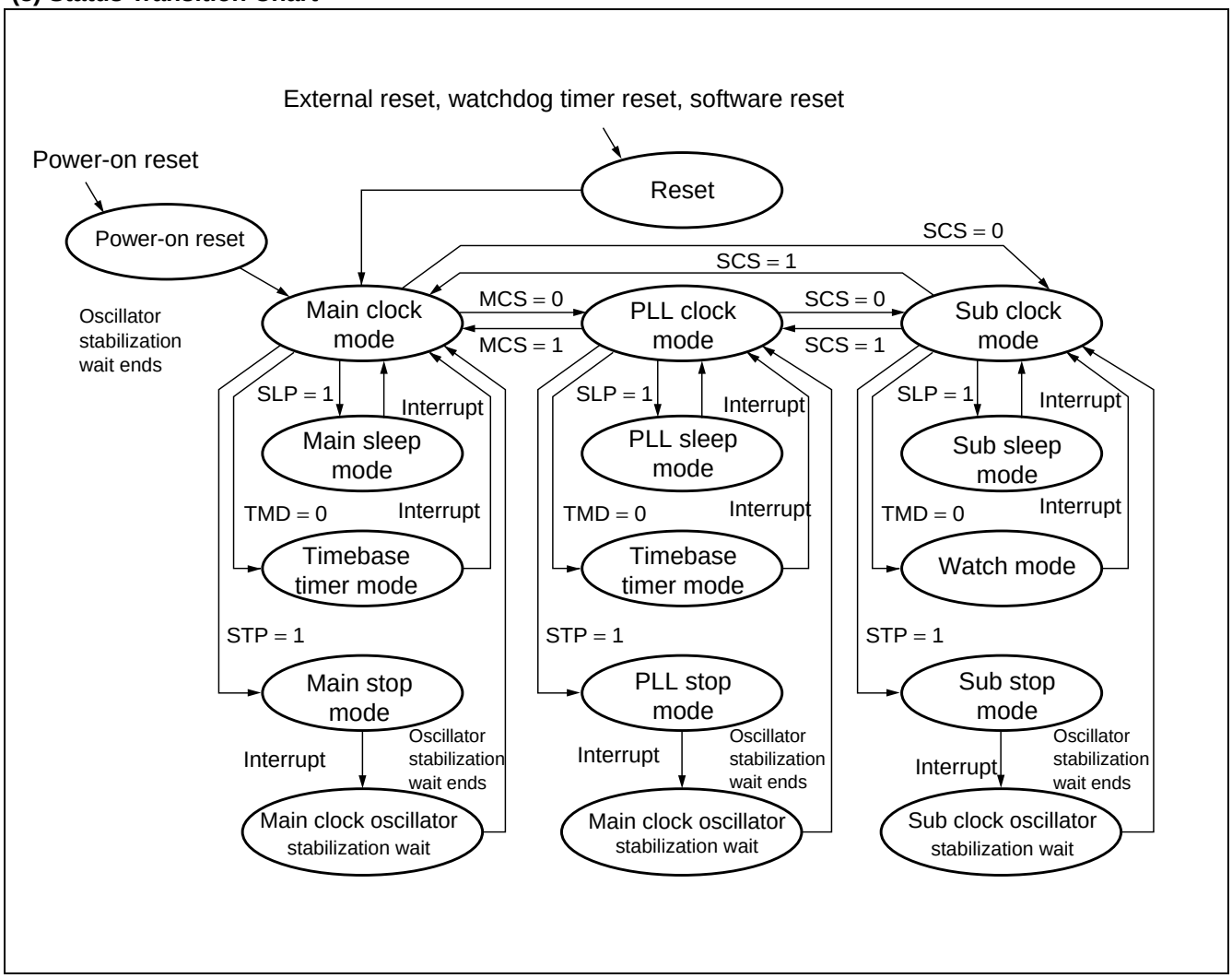
(3) Status Transition Chart



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18. External Bus Pin Control Circuit

The external bus pin control circuit controls the external bus pins used to expand the CPU address/data bus connections to external circuits.

(1) Register List

- Auto ready function select register (ARSR)

Address : 0000A5H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
IOR1	IOR0	HMR1	HMR0	—	—	LMR1	LMR0
W	W	W	W	—	—	W	W

Initial value 0011- - 00B

- External address output control register (HACR)

Address : 0000A6H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W

Initial value ********B

- Bus control signal select register (EPCR)

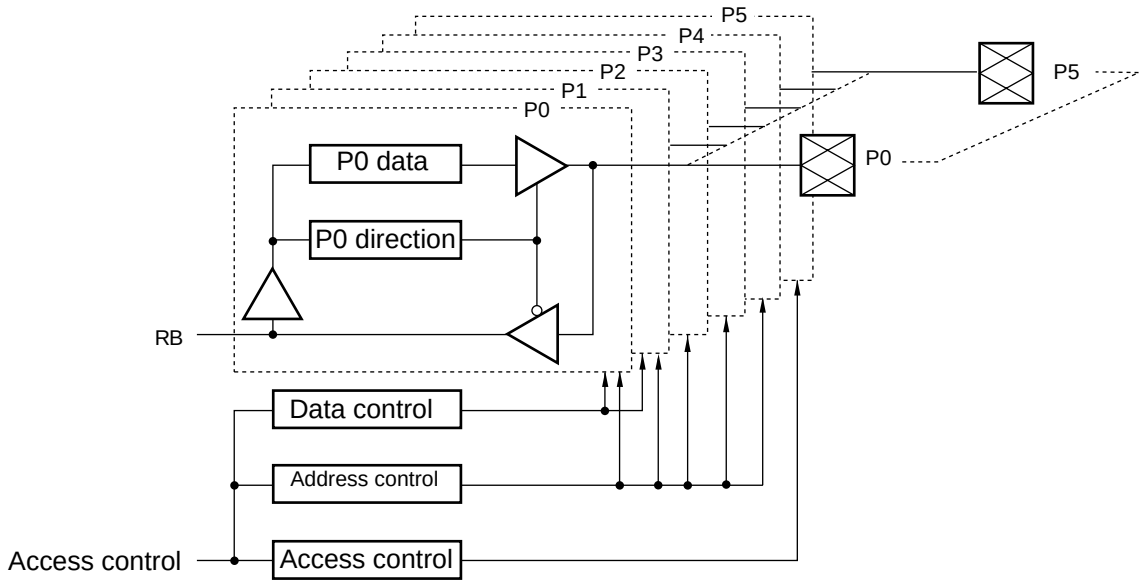
Address : 0000A7H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
CKE	RYE	HDE	IOBS	HMBS	WRE	LMBS	—
W	W	W	W	W	W	W	—

Initial value 1000*10 -B

W : Write only
– : Not used
* : May be either “1” or “0”

(2) Block Diagram



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19. Chip Select Function Description

The chip select module generators a chip select signals, which are used to facilitate connections to external memory devices. The MB90480/485 series has four chip select output pins, each having a chip select area register setting that specifies the corresponding hardware area and select signal that is output when access to the corresponding external address is detected.

- Chip select function features

The chip select function uses two 8-bit registers for each output pin. One of these registers (CARx) is able to detect memory areas in 64 Kbyte units by specifying the upper 8-bit of the address for match detection. The other register (CMRx) can be used to expand the detection area beyond 64 Kbytes by masking bits for match detection.
Note that during external bus holds, the CS output is set to high impedance.

(1) Register List

15 8	7 0	R/W
CAR0	CMR0	R/W
CAR1	CMR1	R/W
CAR2	CMR2	R/W
CAR3	CMR3	R/W
CALR	CSCR	R/W

Chip select area mask register (CMRx)

	7	6	5	4	3	2	1	0	
0000C0H 0000C2H 0000C4H 0000C6H	M7	M6	M5	M4	M3	M2	M1	M0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	0	0	0	0	1	1	1	1	initial value

Chip select area register (CARx)

	15	14	13	12	11	10	9	8	
0000C1H 0000C3H 0000C5H 0000C7H	A7	A6	A5	A4	A3	A2	A1	A0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	1	1	1	1	1	1	1	1	initial value

Chip select control register (CSCR)

	7	6	5	4	3	2	1	0	
0000C8H	—	—	—	—	OPL3	OPL2	OPL1	OPL0	
	—	—	—	—	R/W	R/W	R/W	R/W	Read/write
	—	—	—	—	0	0	0	*	initial value

Chip select active level register (CALR)

	15	14	13	12	11	10	9	8	
0000C9H	—	—	—	—	ACTL3	ACTL2	ACTL1	ACTL0	
	—	—	—	—	R/W	R/W	R/W	R/W	Read/write
	—	—	—	—	0	0	0	0	initial value

* : The initial value of this bit is “1” or “0”.
The value depends on the mode pin (MD2, MD1 and MD0) .

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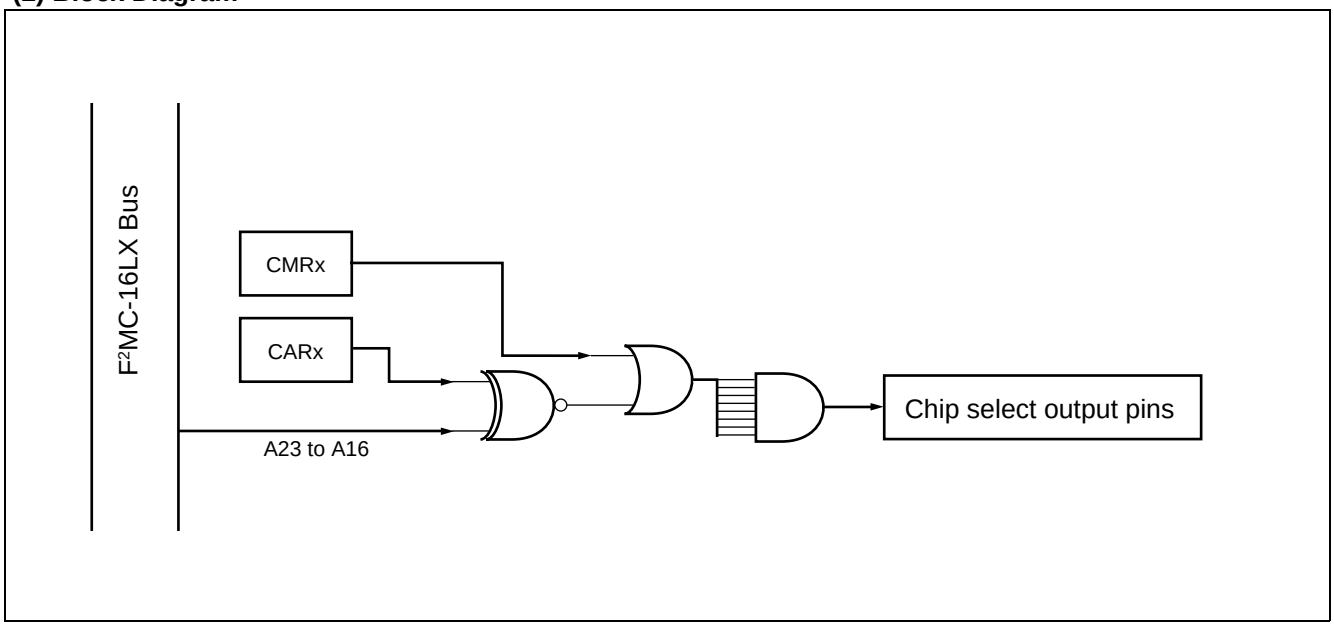
(2) Block Diagram



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20. ROM Mirror Function Select Module

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

(1) Register List

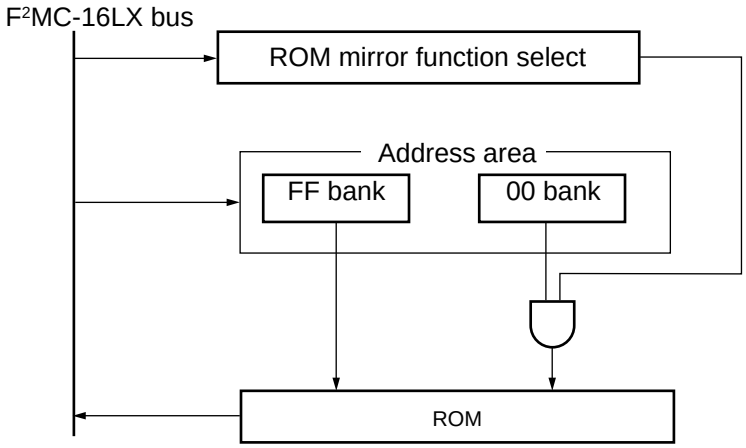
• ROM mirror function select register (ROMM)

Address : 00006F$_H$

bit	15	14	13	12	11	10	9	8	Initial value
	—	—	—	—	—	—	MS	MI	------01$_B$
							R/W	R/W	

- : Not used

(2) Block Diagram



Note : Do not access ROM mirror function selection register (ROMM) on using the area of address 004000$_H$ to 00FFFF$_H$ (008000$_H$ to 00FFFF$_H$) .

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21. Interrupt Controller

The interrupt control register is built in interrupt control, and is supported for all I/O of interrupt function. This register set corresponding peripheral interrupt level.

(1) Register List

Interrupt control registers

Address : ICR01 0000B1H
ICR03 0000B3H
ICR05 0000B5H
ICR07 0000B7H
ICR09 0000B9H
ICR11 0000BBH
ICR13 0000BDH
ICR15 0000BFH

bit	15	14	13	12	11	10	9	8	
	—	—	—	—	Reserved	IL2	IL1	IL0	ICR01, 03, 05, 07, 09, 11, 13, 15
Read/write→	W	W	W	W	R/W	R/W	R/W	R/W	
Initial value→	X	X	X	X	0	1	1	1	

Interrupt control registers

Address : ICR00 0000B0H
ICR02 0000B2H
ICR04 0000B4H
ICR06 0000B6H
ICR08 0000B8H
ICR10 0000BAH
ICR12 0000BCH
ICR14 0000BEH

bit	7	6	5	4	3	2	1	0	
	—	—	—	—	Reserved	IL2	IL1	IL0	ICR00, 02, 04, 06, 08, 10, 12, 14
Read/write→	W	W	W	W	R/W	R/W	R/W	R/W	
Initial value→	X	X	X	X	0	1	1	1	

Note : The use of access involving read-modify-write instructions may lead to abnormal operation, and should be avoided.

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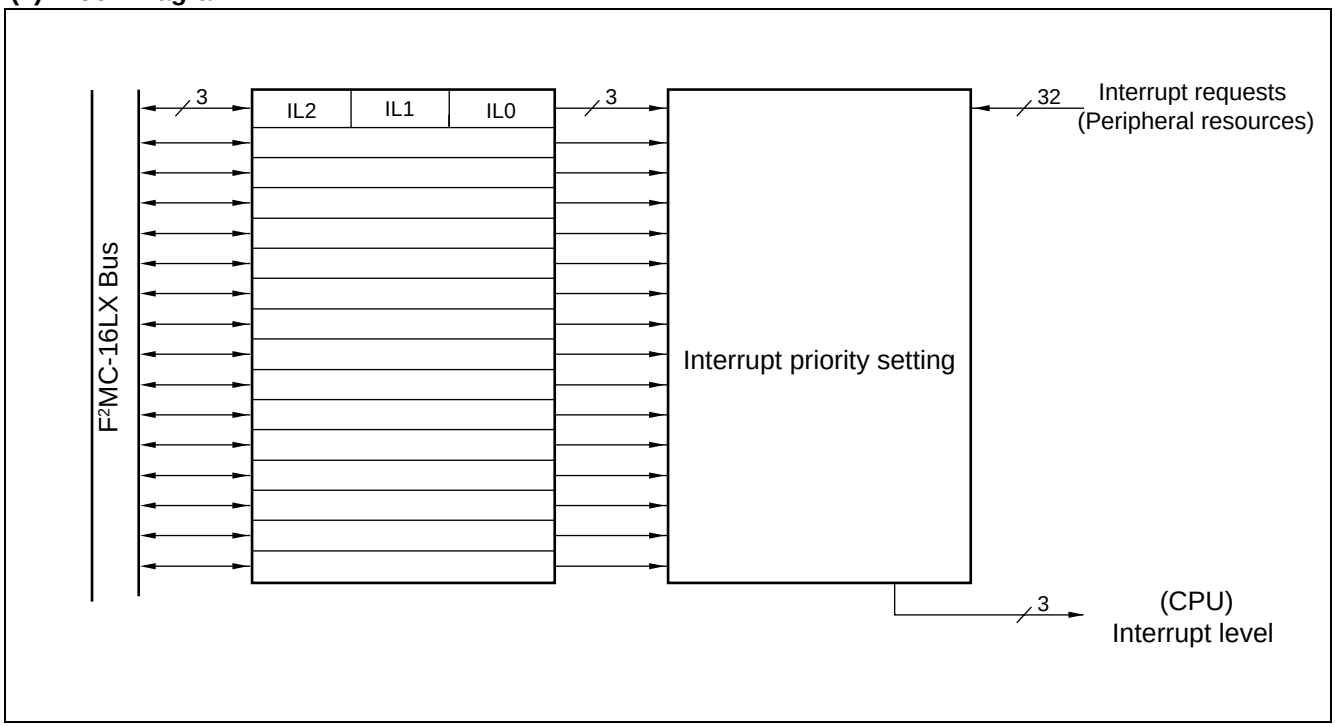
(2) Block Diagram



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22. µDMAC

The µDMAC is a simplified DMA module with functions equivalent to EI²OS. The µDMA has 16 DMA data transfer channels, and provides the following functions.

- Automatic data transfer between peripheral resources (I/O) and memory.
- CPU program execution stops during DMA operation.
- Incremental addressing for transfer source and destination can be turned on and off.
- DMA transfer control from the DMA enable register, DMA stop status register, DMA status register, and descriptor.
- Stop requests from resources can stop DMA transfer.
- When DMA transfer is completed, the DMA status register sets a flag in the bit for the corresponding channel on which transfer was completed, and outputs a completion interrupt to the interrupt controller.

(1) Register List

µDMA enable register

DERH : $0000AD_H$

bit	15	14	13	12	11	10	9	8	Initial value
	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	00000000_B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

µDMA enable register

DERL : $0000AC_H$

bit	7	6	5	4	3	2	1	0	Initial value
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000_B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

µDMA stop status register

DSSR : $0000A4_H$

bit	7	6	5	4	3	2	1	0	Initial value
	STP7	STP6	STP5	STP4	STP3	STP2	STP1	STP0	00000000_B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

µDMA status register

DSRH : $00009D_H$

bit	15	14	13	12	11	10	9	8	Initial value
	DE15	DE14	DE13	DE12	DE11	DE10	DE9	DE8	00000000_B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

µDMA status register

DSRL : $00009C_H$

bit	7	6	5	4	3	2	1	0	Initial value
	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0	00000000_B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

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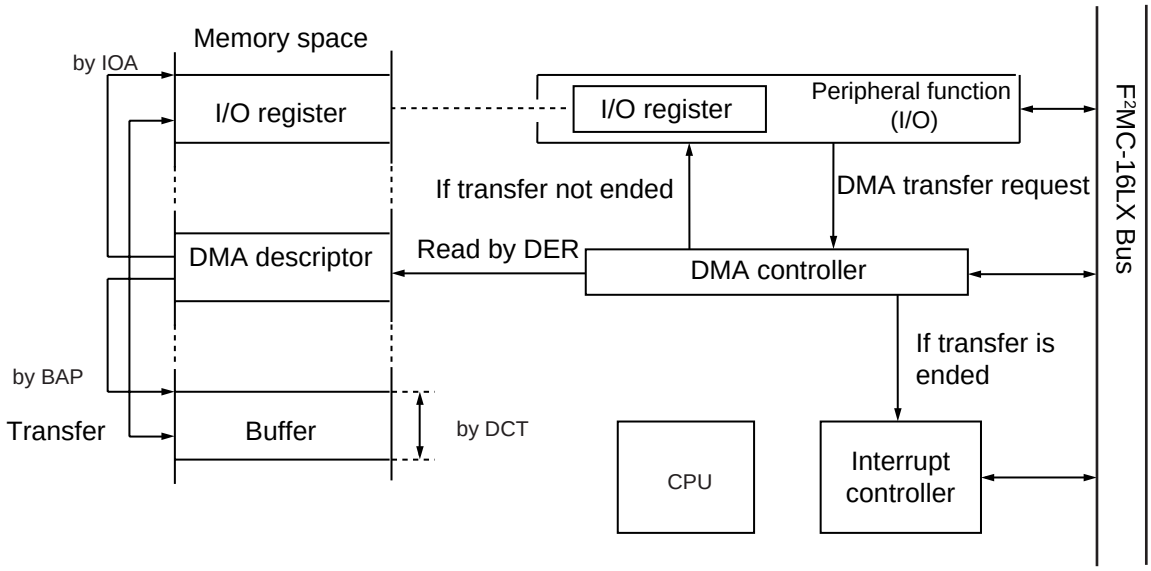
(2) Block Diagram



IOA : I/O address pointer
BAP : Buffer address pointer
DER : DMA enable register (ENx selection)
DCT : Data counter

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23. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT#9 interrupt routine allows the program patching function to be implemented.

Two address detection registers are supported. An interrupt enable bit is prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at “1”, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code.

(1) Register Configuration

- Program address detection register 0 (PADR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Low order address): 001FF0H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Middle order address): 001FF1H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (High order address): 001FF2H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection register 1 (PADR1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Low order address): 001FF3H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Middle order address): 001FF4H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (High order address): 001FF5H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection control status register (PACSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00009EH	RESV	RESV	RESV	RESV	AD1E	RESV	AD0E	RESV	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W :Readable and writable
X :Undefined
RESV:Reserved bit

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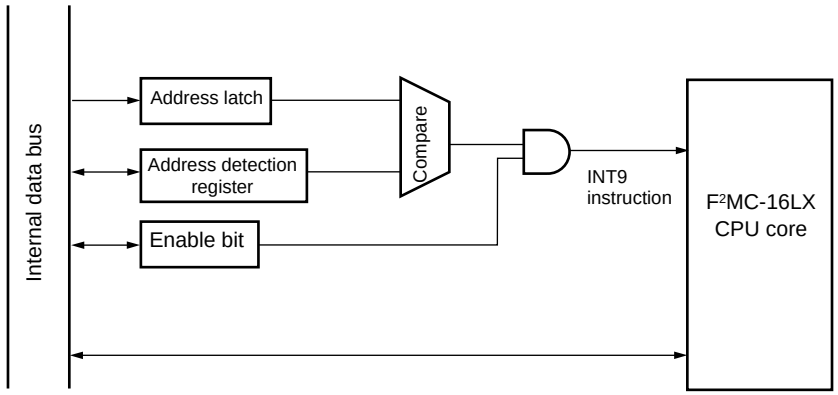
(2) Block Diagram



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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}3$	V_{SS} – 0.3	V_{SS} + 4.0	V	
	$V_{CC}5$	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
	AVRH	V_{SS} – 0.3	V_{SS} + 4.0	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8, *9
Output volatage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8, *9
Maximum clamp current	I_{CLAMP}	–2.0	+2.0	mA	*7
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	*7
“L” level maximum output current	I_{OL}	—	10	mA	*4
“L” level average output current	I_{OLAV}	—	3	mA	*5
“L” level maximum total output current	ΣI_{OL}	—	60	mA	
“L” level total average output current	ΣI_{OLAV}	—	30	mA	*6
“H” level maximum output current	I_{OH}	—	–10	mA	*4
“H” level average output current	I_{OHAV}	—	–3	mA	*5
“H” level maximum total output current	ΣI_{OH}	—	–60	mA	
“H” level total average output current	ΣI_{OHAV}	—	–30	mA	*6
Power consumption	P_D	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : AV_{CC} and AVRH must not exceed V_{CC}. Also, AVRH must not exceed AV_{CC}.

*3 : V_1 and V_0 must not exceed V_{CC} + 0.3 V. However, if the maximum current to/from and input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Maximum output current is defined as the peak value for one of the corresponding pins.

*5 : Average output current is defined as the average current flow in a 100 ms interval at one of the corresponding pins.

*6 : Average total output current is defined as the average current flow in a 100 ms interval at all corresponding pins.

*7 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA3
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

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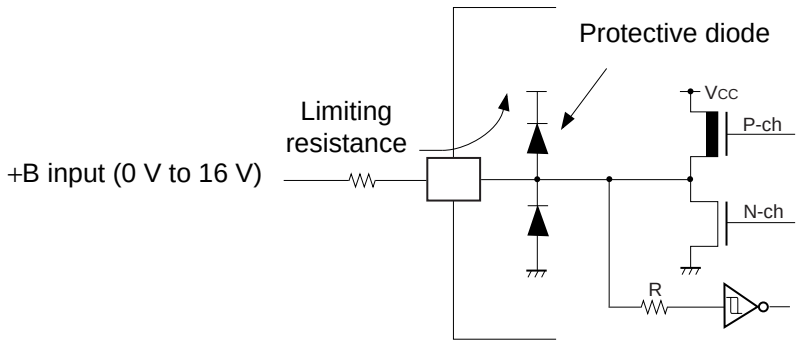
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:

- Input/Output Equivalent circuits



*8 : MB90485 series only
P20 to P27, P30 to P37, P40 to P47, P70 to P77 pins can be used as 5 V I/F pin on applied 5 V to $V_{CC}5$ pin.
P76 and P77 is Nch open drain pin.

*9 : As for P76 and P77 (Nch open drain pin) , even if using at 3 V simplicity ($V_{CC}3 = V_{CC}5$) , the ratings are applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	$V_{CC}3$	2.7	3.6	V	During normal operation
		1.8	3.6	V	To maintain RAM state in stop mode
	$V_{CC}5$	2.7	5.5	V	During normal operation*
		1.8	5.5	V	To maintain RAM state in stop mode*
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	All pins other than V_{IH2}, V_{IHS}, V_{IHM} and V_{IHX}
	V_{IH2}	0.7 V_{CC}	V_{SS} + 5.8	V	MB90485 series only P76, P77 pins (Nch open drain pins)
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
	V_{IHX}	0.8 V_{CC}	V_{CC} + 0.3	V	X0A pin, X1A pin
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	All pins other than V_{ILS}, V_{ILM} and V_{ILX}
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	Hysteresis input pins
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
	V_{ILX}	V_{SS} – 0.3	0.1	V	X0A pin, X1A pin
Operating temperature	T_A	–40	+85	°C	

* : MB90485 series only
P20 to P27, P30 to P37, P40 to P47, P70 to P77 pins can be used as 5 V I/F pin on applied 5 V to $V_{CC}5$ pin.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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3. DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 2.7 V, I_{OH} = –1.6 mA	$V_{CC}3$ – 0.3	—	—	V	
			V_{CC} = 4.5 V, I_{OH} = –4.0 mA	$V_{CC}5$ – 0.5	—	—	V	At using 5 V power supply
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 2.7 V, I_{OL} = 2.0 mA	—	—	0.4	V	
			V_{CC} = 4.5 V, I_{OH} = 4.0 mA	—	—	0.4	V	At using 5 V power supply
Input leakage current	I_{IL}	All input pins	V_{CC} = 3.3 V, $V_{SS} < V_I < V_{CC}$	–10	—	+10	µA	
Pull-up resistance	RPULL	—	V_{CC} = 3.0 V, at T_A = +25 °C	20	53	200	kΩ	
Open drain output current	I_{leak}	P40 to P47, P70 to P77	—	—	0.1	10	µA	
Power supply current	I_{CC}	—	At V_{CC} = 3.3 V, internal 25 MHz operation, normal operation	—	45	60	mA	
			At V_{CC} = 3.3 V, internal 25 MHz operation, FLASH programming	—	55	70	mA	
	I_{CCS}	—	At V_{CC} = 3.3 V, internal 25 MHz operation, sleep mode	—	17	35	mA	
	I_{CCL}	—	At V_{CC} = 3.3 V, external 32 kHz, internal 8 kHz operation, sub clock operation (T_A = +25 °C)	—	15	140	µA	
	I_{CCT}	—	At V_{CC} = 3.3 V, external 32 kHz, internal 8 kHz operation, watch mode (T_A = +25 °C)	—	1.8	40	µA	
	I_{CCH}	—	T_A = +25 °C, stop mode, At V_{CC} = 3.3 V	—	0.8	40	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	—	—	5	15	pF	

Notes :
- Pins P40 to P47, and P70 to P77 are controlled N-ch open drain pins, and should always be used at CMOS levels.
- MB90485 series only
- P40 to P47 and P70 to P77 are Nch open drain pins with control, which are usually used as CMOS.
- P76 and P77 are open drain pins without Pch.
- For use as a single 3 V power supply products, set V_{CC} = $V_{CC}3$ = $V_{CC}5$.
- When the device is used with dual power supplies, P20 to P27, P30 to P37, P40 to P47 and P70 to P77 serve as 5 V pins while the other pins serve as 3 V I/O pins.

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4. AC Characteristics

(1) Clock Timing Standards

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pinname	Condition	Value Min	Value Typ	Value Max	Unit	Remarks
Clock frequency	F_{CH}	X0, X1	—	3	—	25	MHz	External crystal oscillator
			—	3	—	50		External clock input
			—	4	—	25		1 multiplied PLL
			—	3	—	12.5		2 multiplied PLL
			—	3	—	6.66		3 multiplied PLL
			—	3	—	6.25		4 multiplied PLL
			—	3	—	4.16		6 multiplied PLL
			—	3	—	3.12		8 multiplied PLL
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t_C	X0, X1	—	20	—	333	ns	*1
	t_{CL}	X0A, X1A	—	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	—	5	—	—	ns	
	P_{WLH} P_{WLL}	X0A	—	—	15.2	—	µs	*2
Input clock rise, fall time	t_{cr} t_{cf}	X0	—	—	—	5	ns	With external clock
Internal operating clock frequency	f_{CP}	—	—	1.5	—	25	MHz	*1
	f_{CPL}	—	—	—	8.192	—	kHz	
Internal operating clock cycle time	t_{CP}	—	—	40.0	—	666	ns	*1
	t_{CPL}	—	—	—	122.1	—	µs	

*1 : Be careful of the operating voltage.

*2 : Duty raito should be 50 % ± 3 %.

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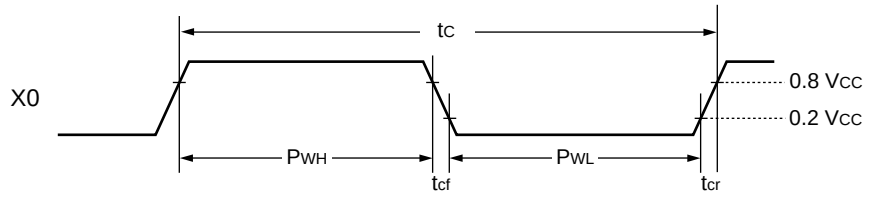
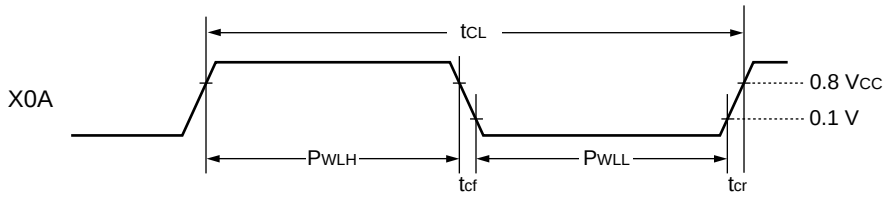
- X0, X1 clock timing



- X0A, X1A clock timing



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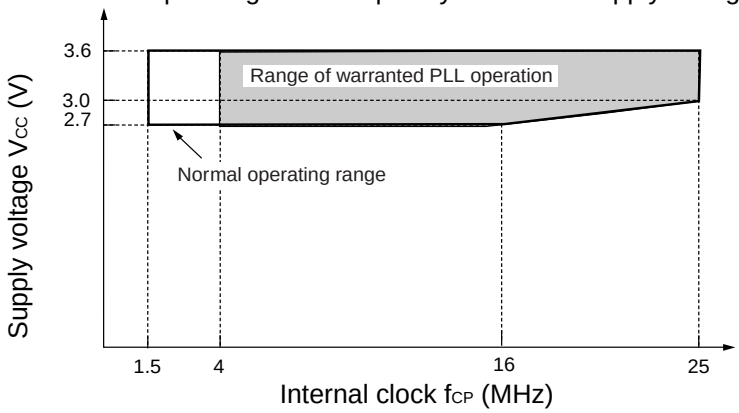
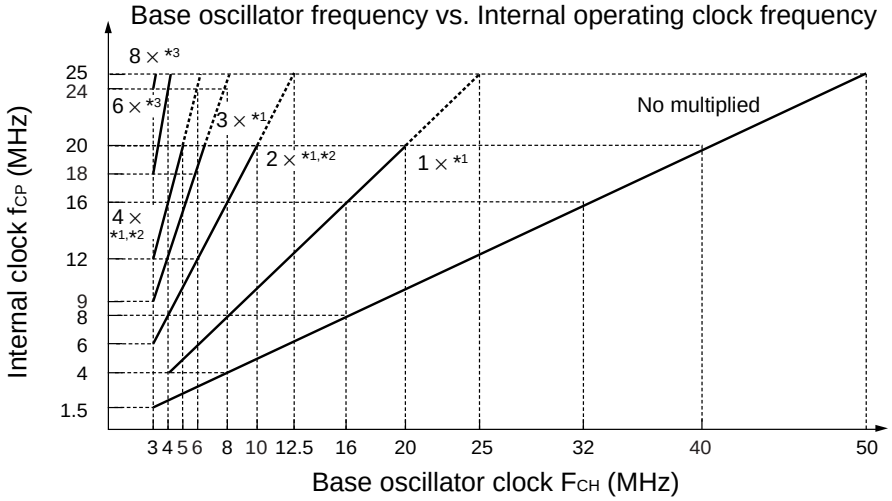
- Range of warranted PLL operation

Internal operating clock frequency vs. Power supply voltage



Notes:
- For A/D operating frequency, refer to "5. A/D Converter Electrical Characteristics"
- Only at 1 multiplied PLL, use with more than fcp = 4 MHz.

Base oscillator frequency vs. Internal operating clock frequency



*1 : In setting as 1, 2, 3 and 4 multiplied PLL, when the internal clock is used at 20 MHz < fcp ≤ 25 MHz, set the PLLOS register to "DIV2 bit = 1" and "PLL2 bit = 1".
[Example] When using the base oscillator frequency of 24 MHz at 1 multiplied PLL :
CKSCR register : CS1 bit = "0", CS0 bit = "0" PLLOS register : DIV2 bit = "1", PLL2 bit = "1"
[Example] When using the base oscillator frequency of 6 MHz at 3 multiplied PLL :
CKSCR register : CS1 bit = "1", CS0 bit = "0" PLLOS register : DIV2 bit = "1", PLL2 bit = "1"

*2 : In setting as 2 and 4 multiplied PLL, when the internal clock is used at 20 MHz < fcp ≤ 25 MHz, the following setting is also enabled.
2 multiplied PLL : CKSCR register : CS1 bit = "0", CS0 bit = "0"
PLLOS register : DIV2 bit = "0", PLL2 bit = "1"
4 multiplied PLL : CKSCR register : CS1 bit = "0", CS0 bit = "1"
PLLOS register : DIV2 bit = "0", PLL2 bit = "1"

*3 : When using in setting as 6 and 8 multiplied PLL, set the PLLOS register to "DIV2 bit = 0" and "PLL2 bit = 1".
[Example] When using the base oscillator frequency of 4 MHz at 6 multiplied PLL :
CKSCR register : CS1 bit = "1", CS0 bit = "0" PLLOS register : DIV2 bit = "0", PLL2 bit = "1"
[Example] When using the base oscillator frequency of 3 MHz at 8 multiplied PLL :
CKSCR register : CS1 bit = "1", CS0 bit = "1" PLLOS register : DIV2 bit = "0", PLL2 bit = "1"

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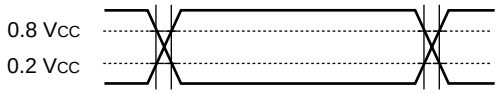
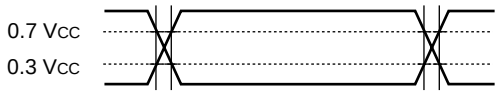
AC standards are set at the following measurement voltage values.

- Input signal waveform

Hysteresis input pins

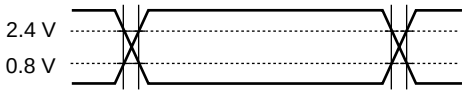


- Pins other than hysteresis input/MD input



- Output signal waveform

Output pins



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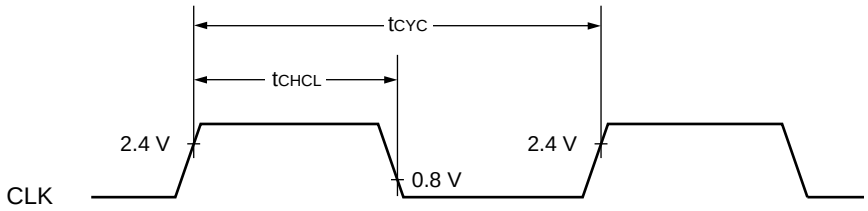
(2) Clock Output Timing

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}*	—	ns	
CLK↑→CLK↓	t_{CHCL}	CLK	V_{CC} = 3.0 V to 3.6 V	t_{CP}* / 2 – 15	t_{CP}* / 2 + 15	ns	at f_{cp} = 25 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP}* / 2 – 20	t_{CP}* / 2 + 20	ns	at f_{cp} = 16 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP}* / 2 – 64	t_{CP}* / 2 + 64	ns	at f_{cp} = 5 MHz

* : For t_{CP} see “ (1) Clock Timing Standards.”



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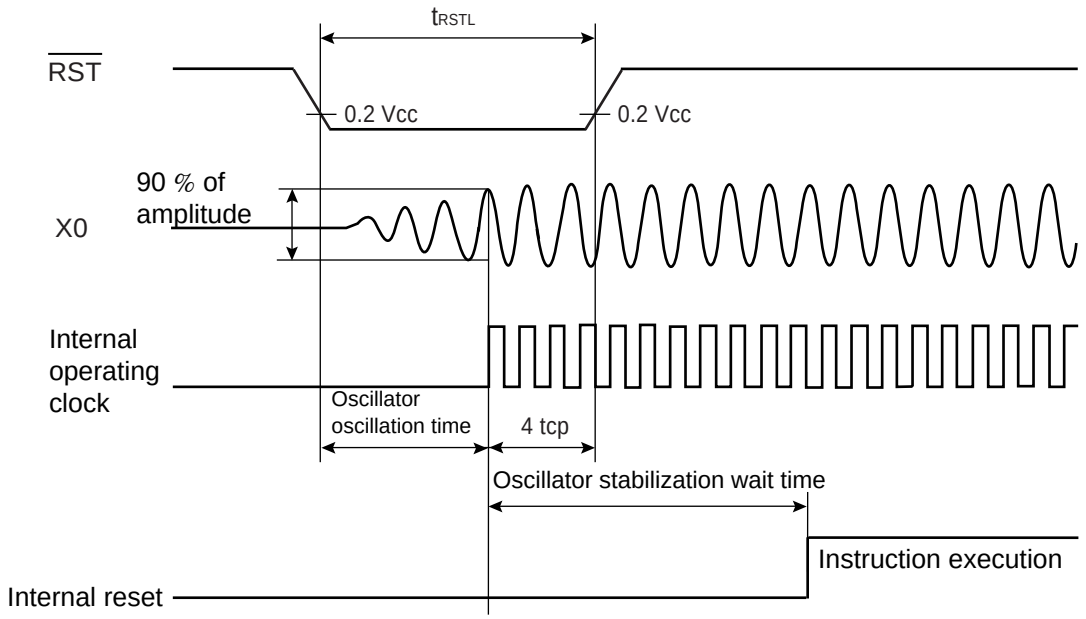
(3) Reset Input Standards

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

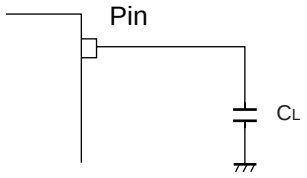
Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}	—	ns	Normal operation
				Oscillator oscillation time* + 4 t_{CP}	—	ms	Stop mode

* : Oscillator oscillation time is the time to 90 % of amplitude. For a crystal oscillator this is on the order of several milliseconds to tens of milliseconds. For a FAR/ceramic oscillator, this is several hundred microseconds to several milliseconds. For an external clock signal the value is 0 ms.

• In stop mode



• Condition for measurement of AC standards



C_L : Load capacitance applied during testing
CLK, ALE : C_L = 30 pF
AD15 to AD00 (address data bus) , $\overline{RD}$, $\overline{WR}$,
A23 to A00/D15 to D00 : C_L = 30 pF

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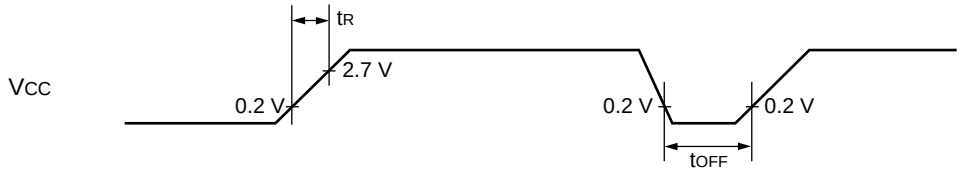
(4) Power-on Reset Standards

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

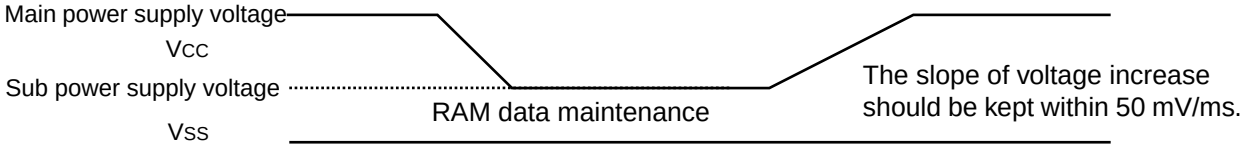
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power rise time	t_R	V_{CC}	—	—	30	ms	*
Power down time	t_{OFF}	V_{CC}		1	—	ms	In repeated operation

* : Power rise time requires V_{CC} < 0.2 V.

Notes:
- The above standards are for the application of a power-on reset.
- Within the device, the power-on reset should be applied by switching the power supply off and on again.



Rapid fluctuations in power supply voltage may trigger a power-on reset in some cases. As shown below, when changing supply voltage during operation, it is recommended that voltage changes be suppressed and a smooth restart be applied.



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(5) Bus Read Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	t_{CP}* / 2 – 15	—	ns	at f_{cp} = 25 MHz
				t_{CP}* / 2 – 20	—	ns	at f_{cp} = 16 MHz
				t_{CP}* / 2 – 35	—	ns	at f_{cp} = 8 MHz
Valid address→ ALE↓time	t_{AVLL}	Address, ALE	—	t_{CP}* / 2 – 17	—	ns	
				t_{CP}* / 2 – 40	—	ns	at f_{cp} = 8 MHz
ALE↓→ address valid time	t_{LLAX}	ALE, Address	—	t_{CP}* / 2 – 15	—	ns	
Valid address→ $\overline{RD}$↓time	t_{AVRL}	$\overline{RD}$, address	—	t_{CP}* – 25	—	ns	
Valid address→ valid data input	t_{AVDV}	Address, Data	—	—	5 t_{CP}* / 2 – 55	ns	
				—	5 t_{CP}* / 2 – 80	ns	at f_{cp} = 8 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	3 t_{CP}* / 2 – 25	—	ns	at f_{cp} = 25 MHz
				3 t_{CP}* / 2 – 20	—	ns	at f_{cp} = 16 MHz
$\overline{RD}$↓→ valid data input	t_{RLDV}	$\overline{RD}$, Data	—	—	3 t_{CP}* / 2 – 55	ns	
				—	3 t_{CP}* / 2 – 80	ns	at f_{cp} = 8 MHz
$\overline{RD}$↑→data hold time	t_{RHDX}	$\overline{RD}$, Data	—	0	—	ns	
$\overline{RD}$↑→ALE↑rise time	t_{RHLH}	$\overline{RD}$, ALE	—	t_{CP}* / 2 – 15	—	ns	
$\overline{RD}$↑→ address valid time	t_{RHAX}	Address, $\overline{RD}$	—	t_{CP}* / 2 – 10	—	ns	
Valid address→ CLK↑time	t_{AVCH}	Address, CLK	—	t_{CP}* / 2 – 17	—	ns	
$\overline{RD}$↓→CLK↑time	t_{RLCH}	$\overline{RD}$, CLK	—	t_{CP}* / 2 – 17	—	ns	
ALE↓→$\overline{RD}$↓time	t_{LLRL}	$\overline{RD}$, ALE	—	t_{CP}* / 2 – 15	—	ns	

* : t_{CP} : See “ (1) Clock Timing Standards”.

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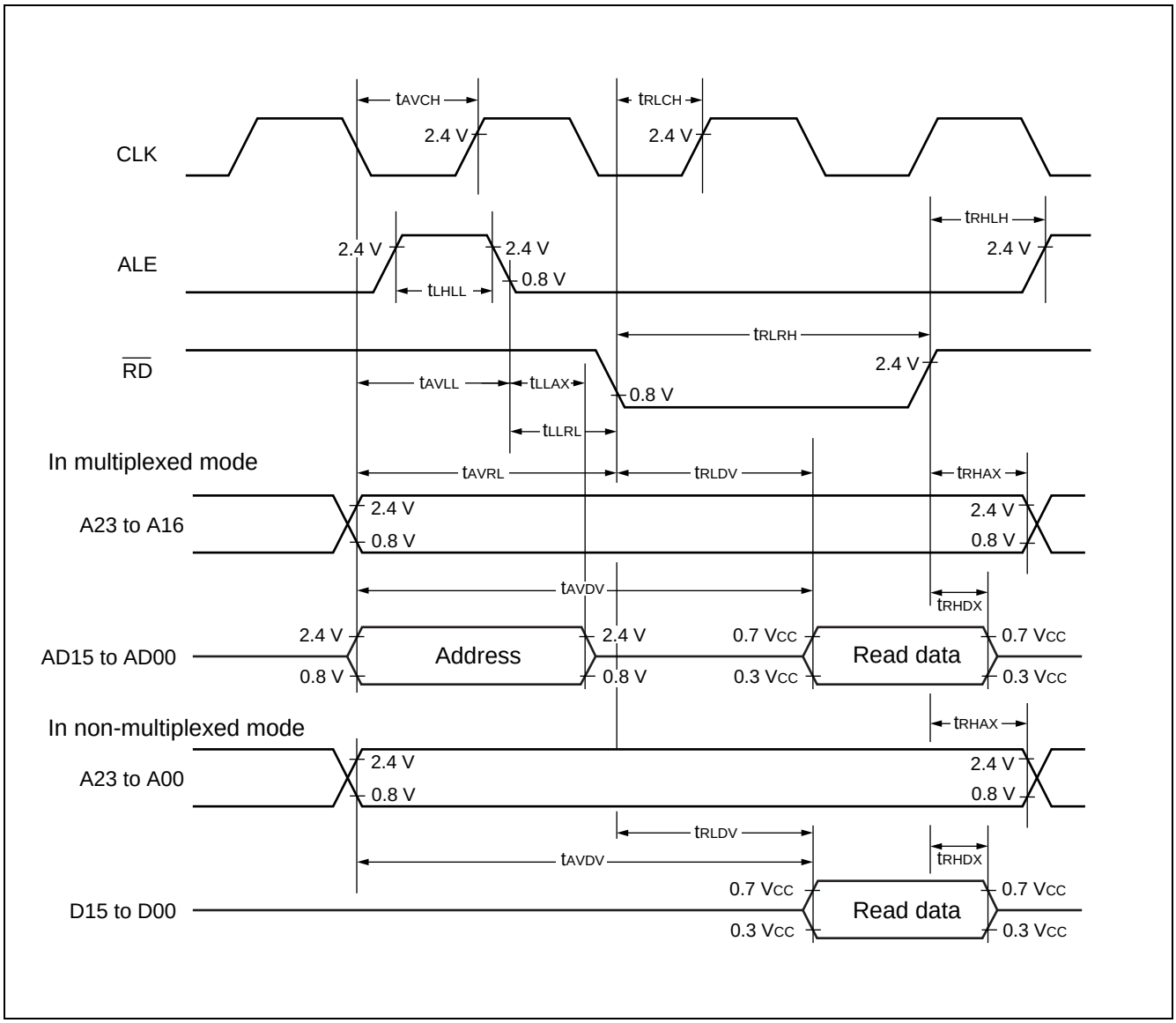

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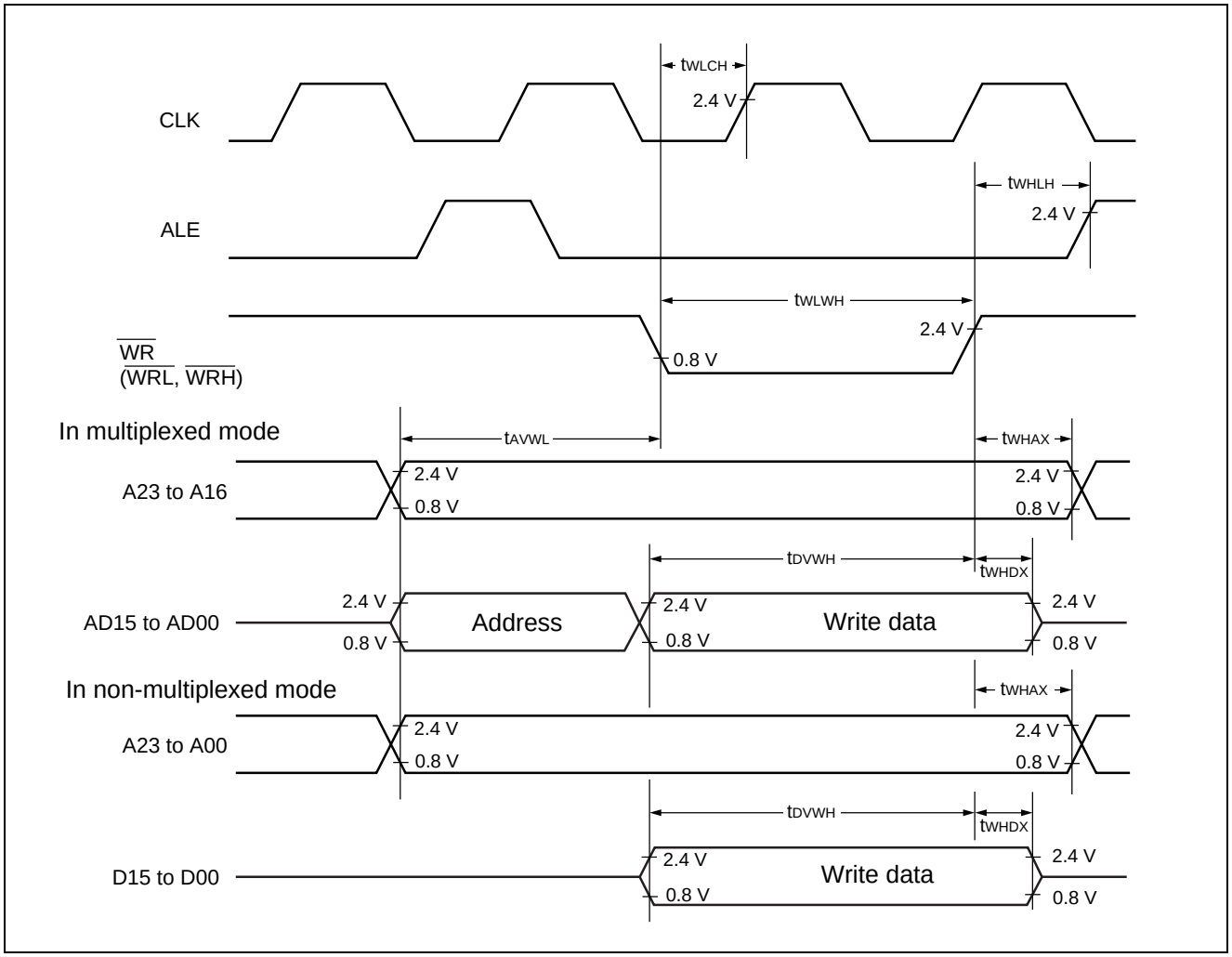
(6) Bus Write Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value Min	Value Max	Unit	Remarks
Valid address→$\overline{WR}$↓time	t_{AVWL}	Address, WR	—	t_{CP}* – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 t_{CP}* / 2 – 25	—	ns	at f_{cp} = 25 MHz
			—	3 t_{CP}* / 2 – 20	—	ns	at f_{cp} = 16 MHz
Valid data output →$\overline{WR}$↑time	t_{DVWH}	Data, $\overline{WR}$	—	3 t_{CP}* / 2 – 15	—	ns	
$\overline{WR}$↑→data hold time	t_{WHDX}	$\overline{WR}$, Data	—	10	—	ns	at f_{cp} = 25 MHz
			—	20	—	ns	at f_{cp} = 16 MHz
			—	30	—	ns	at f_{cp} = 8 MHz
$\overline{WR}$↑→address valid time	t_{WHAX}	$\overline{WR}$, Address	—	t_{CP}* / 2 – 10	—	ns	
$\overline{WR}$↑→ALE↑time	t_{WHLH}	$\overline{WR}$, ALE	—	t_{CP}* / 2 – 15	—	ns	
$\overline{WR}$↓→CLK↑time	t_{WLCH}	$\overline{WR}$, CLK	—	t_{CP}* / 2 – 17	—	ns	

* : t_{CP} : See “ (1) Clock Timing Standards”.



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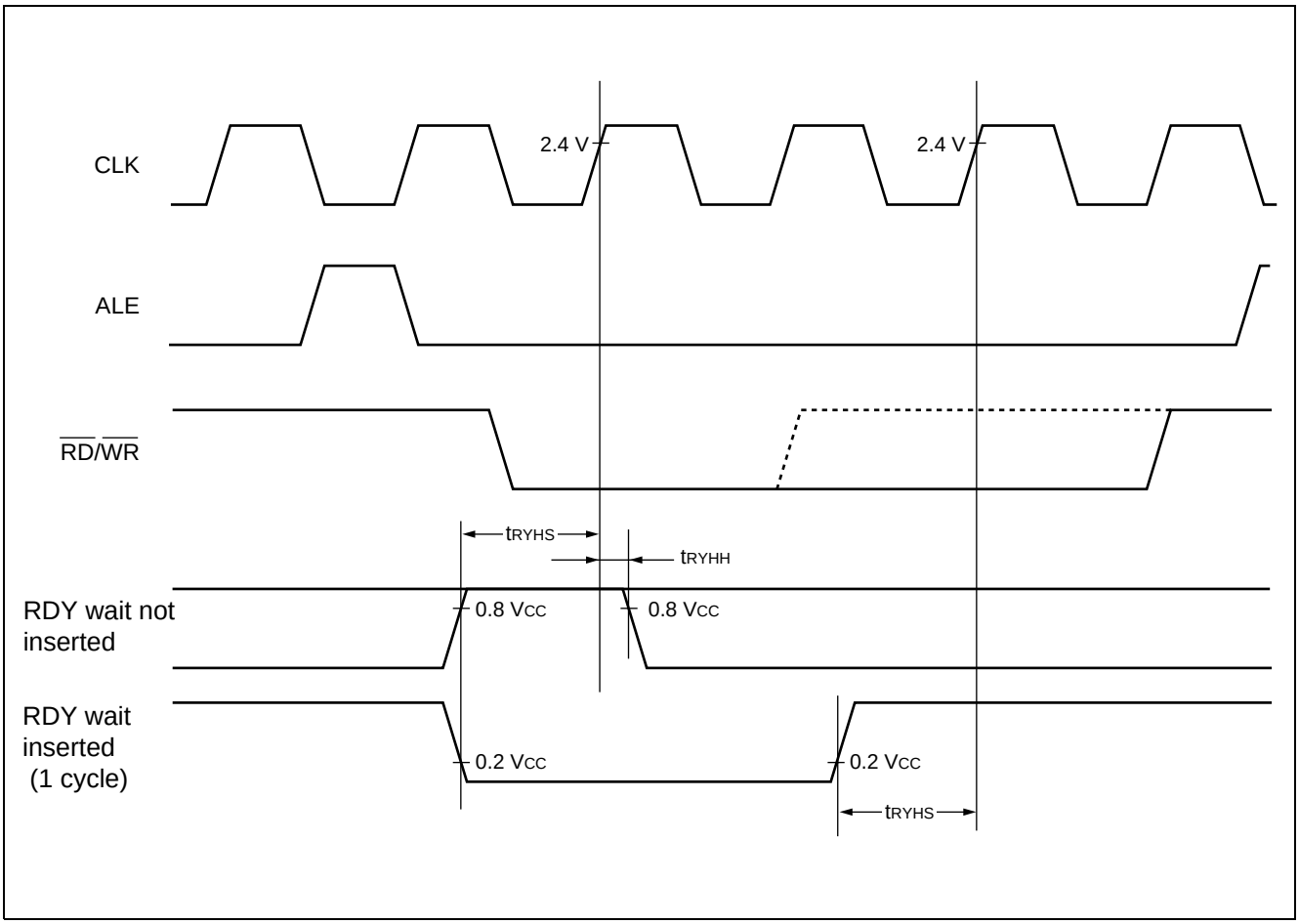
(7) Ready Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
			—	70	—	ns	at f_{cp} = 8 MHz
RDY hold time	t_{RYHH}		—	0	—	ns	

Notes: • If the RDY setup time is insufficient, use the auto ready function.
• Warning : For input from the RDY pin, if the AC ratings are not satisfied this device may unexpected operation.



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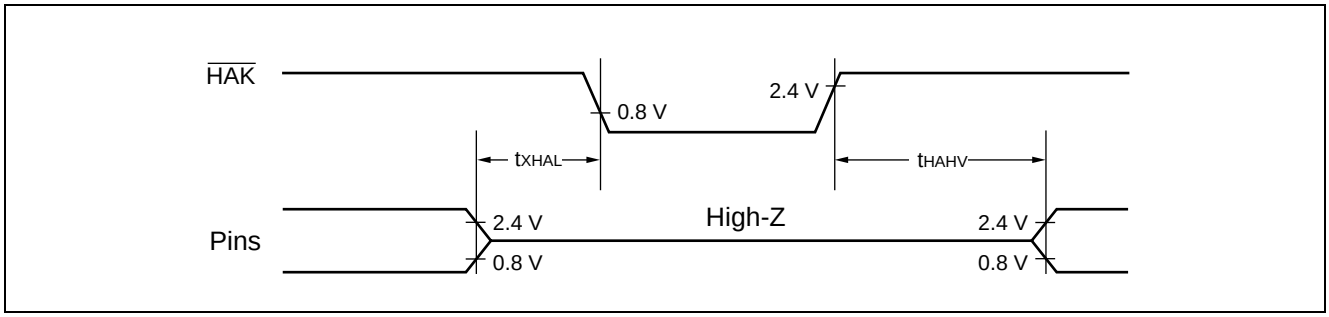
(8) Hold Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Pin floating→$\overline{HAK}$↓time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}*	ns	
$\overline{HAK}$↓→pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}*	ns	

* : t_{CP} : See " (1) Clock Timing Standards".

Note : One or more cycles are required from the time the HRQ pin is read until the $\overline{HAK}$ signal changes.



(9) UART Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	8 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		–80	+80	ns	
				–120	+120	ns	f_{cp} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{cp} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		t_{CP}*2	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	External shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	4 t_{CP}*2	—	ns	
Serial clock "L" pulse width	t_{SLSH}	—		4 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{cp} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz

*1 : C_L is the load capacitance applied to pins for testing.
*2 : t_{CP} : See " (1) Clock Timing Standards".

Note : AC ratings are for CLK synchronized mode.

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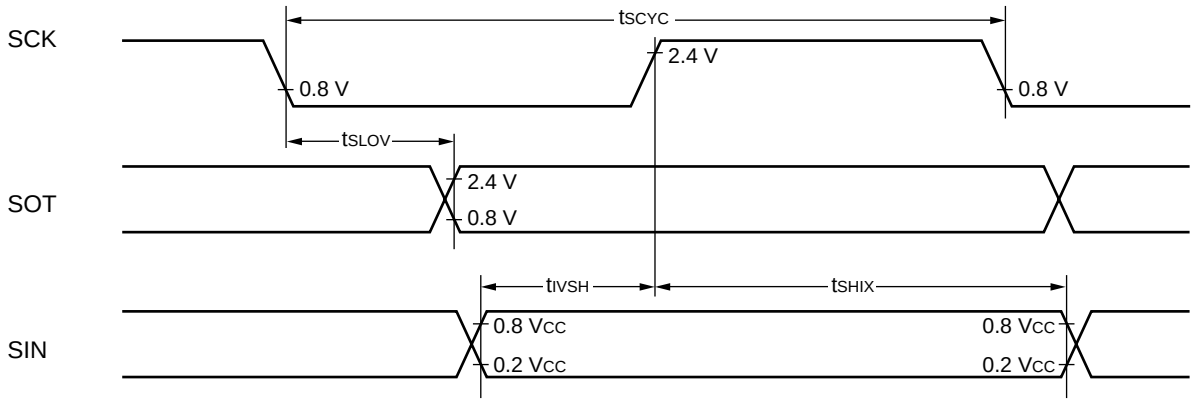
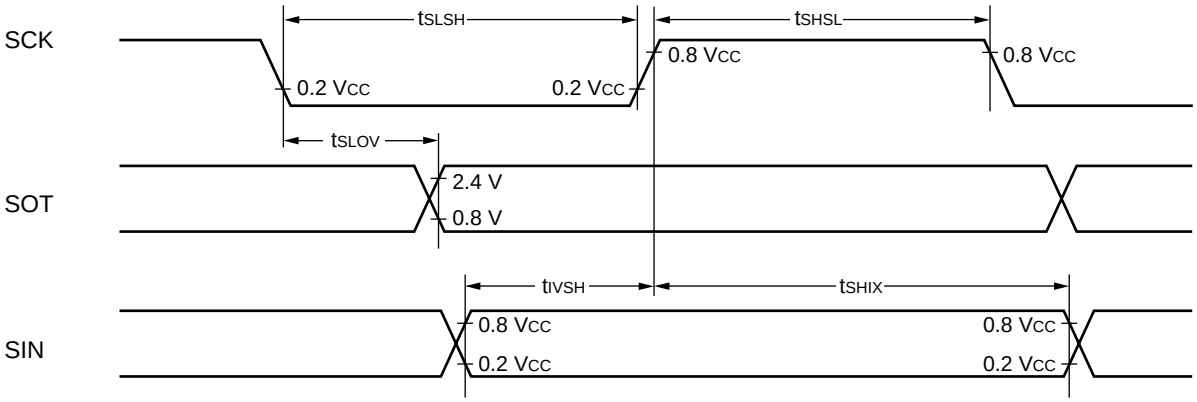
- Internal shift clock mode



- External shift clock mode



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(10) I/O Expanded Serial Interface Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	8 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		–80	+ 80	ns	
				–120	+ 120	ns	f_{cp} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{cp} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		t_{CP}*2	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	4 t_{CP}*2	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CP}*2	—	ns	
SCK↓→SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{cp} = 8 MHz
Valid SIN→SCK↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz
SCK↑→valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz

*1 : C_L is the load capacitance applied to pins for testing.

*2 : t_{CP} : See “ (1) Clock Timing Standards”.

Notes :
- AC ratings are for CLK synchronized mode.
- Values on this table are target values.

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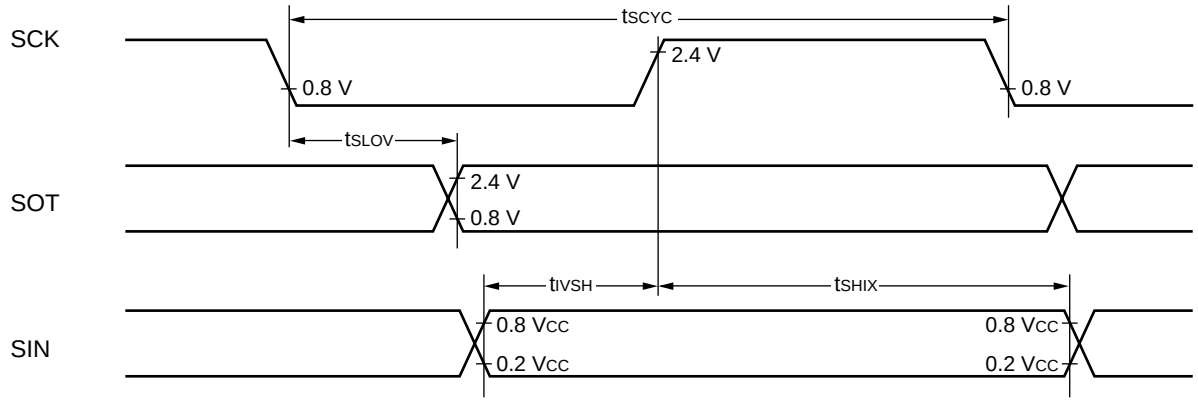
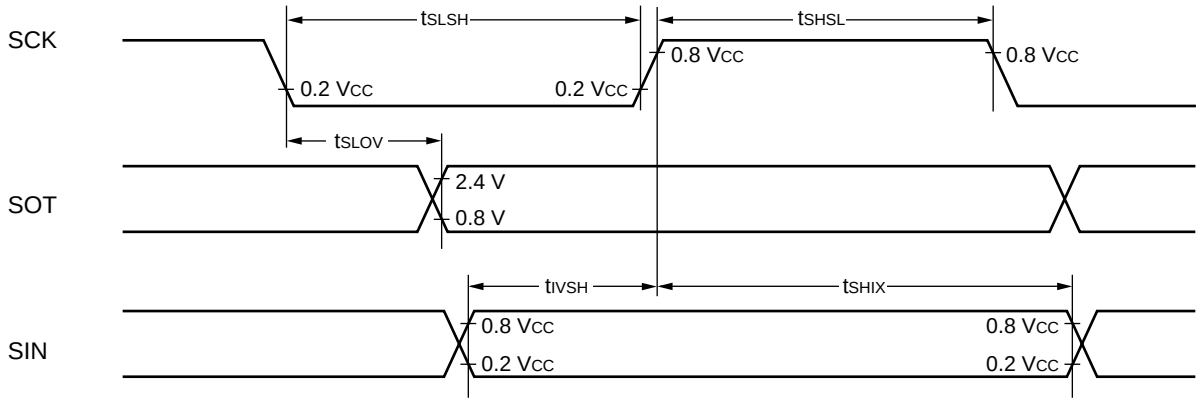
- Internal shift clock mode



- External shift clock mode



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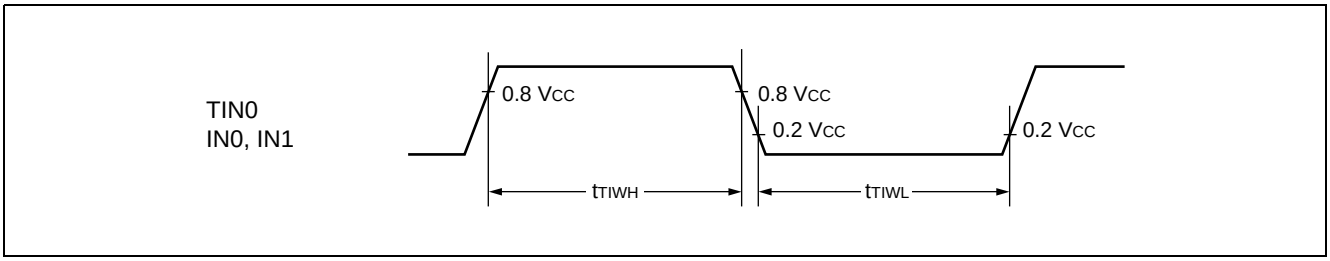
(11) Timer Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, IN0, IN1, PWC0 to PWC3	—	4 t_{CP}*	—	ns	

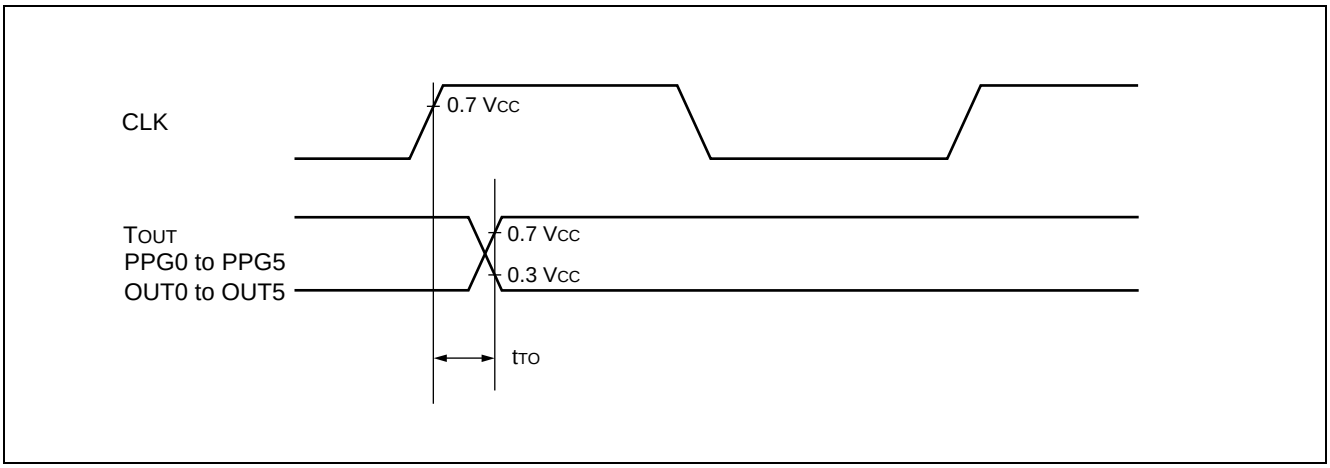
* : t_{CP} : See “ (1) Clock Timing Standards”.



(12) Timer Output Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
CLK↑→Tout change time PPG0 to PPG5 change time OUT0 to OUT5 change time	t_{TO}	TOT0, PPG0 to PPG5, OUT0 to OUT5	Load conditions 80 pF	30	—	ns	



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(13) I²C Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

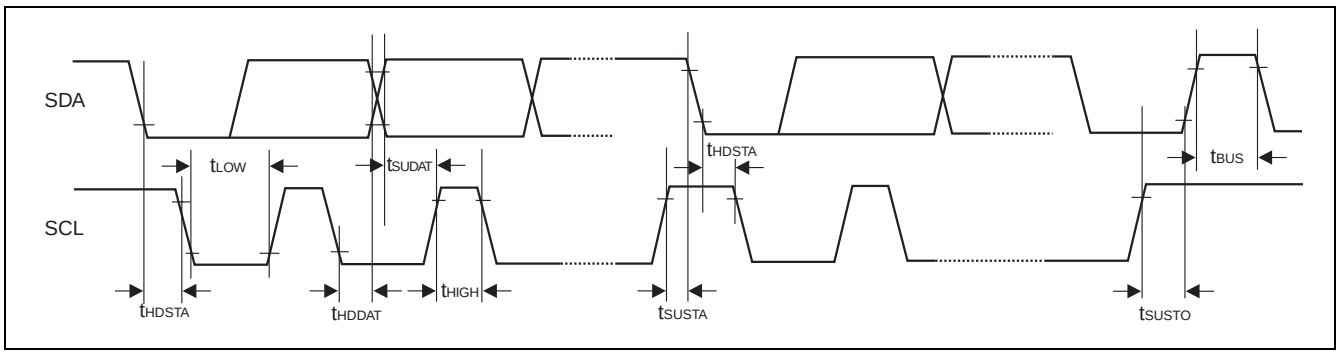
Parameter	Symbol	Condition	Standard-mode Min	Standard-mode Max	Unit
SCL clock frequency	f_{SCL}	When power supply voltage of external pull-up resistance is 5.5 V R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V R = 1.6 kΩ, C = 50 pF*2	0	100	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	µs
Set-up time (repeated) START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	When power supply voltage of external pull-up resistance is 5.5 V fcp*1 ≤ 20 MHz, R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V fcp*1 ≤ 20 MHz, R = 1.6 kΩ, C = 50 pF*2	250	—	ns
		When power supply voltage of external pull-up resistance is 5.5 V fcp*1 > 20 MHz, R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V fcp*1 > 20 MHz, R = 1.6 kΩ, C = 50 pF*2	200	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	When power supply voltage of external pull-up resistance is 5.5 V R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V R = 1.6 kΩ, C = 50 pF*2	4.0	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	µs

*1 : fcp is internal operation clock frequency. Refer to " (1) Clock Timing Standards".

*2 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*3 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

Note : V_{CC} = $V_{CC}3$ = $V_{CC}5$



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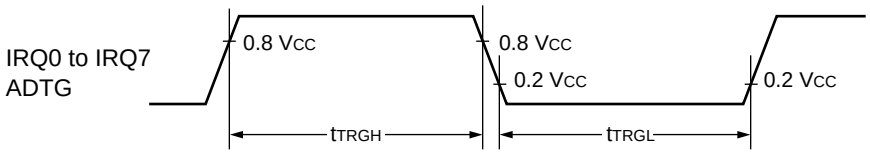
(14) Trigger Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	ADTG, IRQ0 to IRQ7	—	5 t_{CP}*	—	ns	Normal operation
				1	—	µs	Stop mode

* : t_{CP} : See “ (1) Clock Timing Standards”.



(15) Up-down Counter Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
AIN input “H” pulse width	t_{AHL}	AIN0, AIN1, BIN0, BIN1	Load conditions 80 pF	8 t_{CP}*	—	ns	
AIN input “L” pulse width	t_{ALL}			8 t_{CP}*	—	ns	
BIN input “H” pulse width	t_{BHL}			8 t_{CP}*	—	ns	
BIN input “L” pulse width	t_{BLL}			8 t_{CP}*	—	ns	
AIN↑→BIN↑ rise time	t_{AUBU}			4 t_{CP}*	—	ns	
BIN↑→AIN↓ fall time	t_{BUAD}			4 t_{CP}*	—	ns	
AIN↓→BIN↑ rise time	t_{ADBD}			4 t_{CP}*	—	ns	
BIN↓→AIN↑ rise tome	t_{BDAU}			4 t_{CP}*	—	ns	
BIN↑→AIN↑ rise time	t_{BUAU}			4 t_{CP}*	—	ns	
AIN↑→BIN↓ fall time	t_{AUBD}			4 t_{CP}*	—	ns	
BIN↓→AIN↑ rise time	t_{BDAD}			4 t_{CP}*	—	ns	
AIN↓→BIN↑ rise time	t_{ADBU}			4 t_{CP}*	—	ns	
ZIN input “H” pulse width	t_{ZHL}	ZIN0, ZIN1		4 t_{CP}*	—	ns	
ZIN input “L” pulse width	t_{ZLL}			4 t_{CP}*	—	ns	

* : t_{CP} : See “ (1) Clock Timing Standards”.

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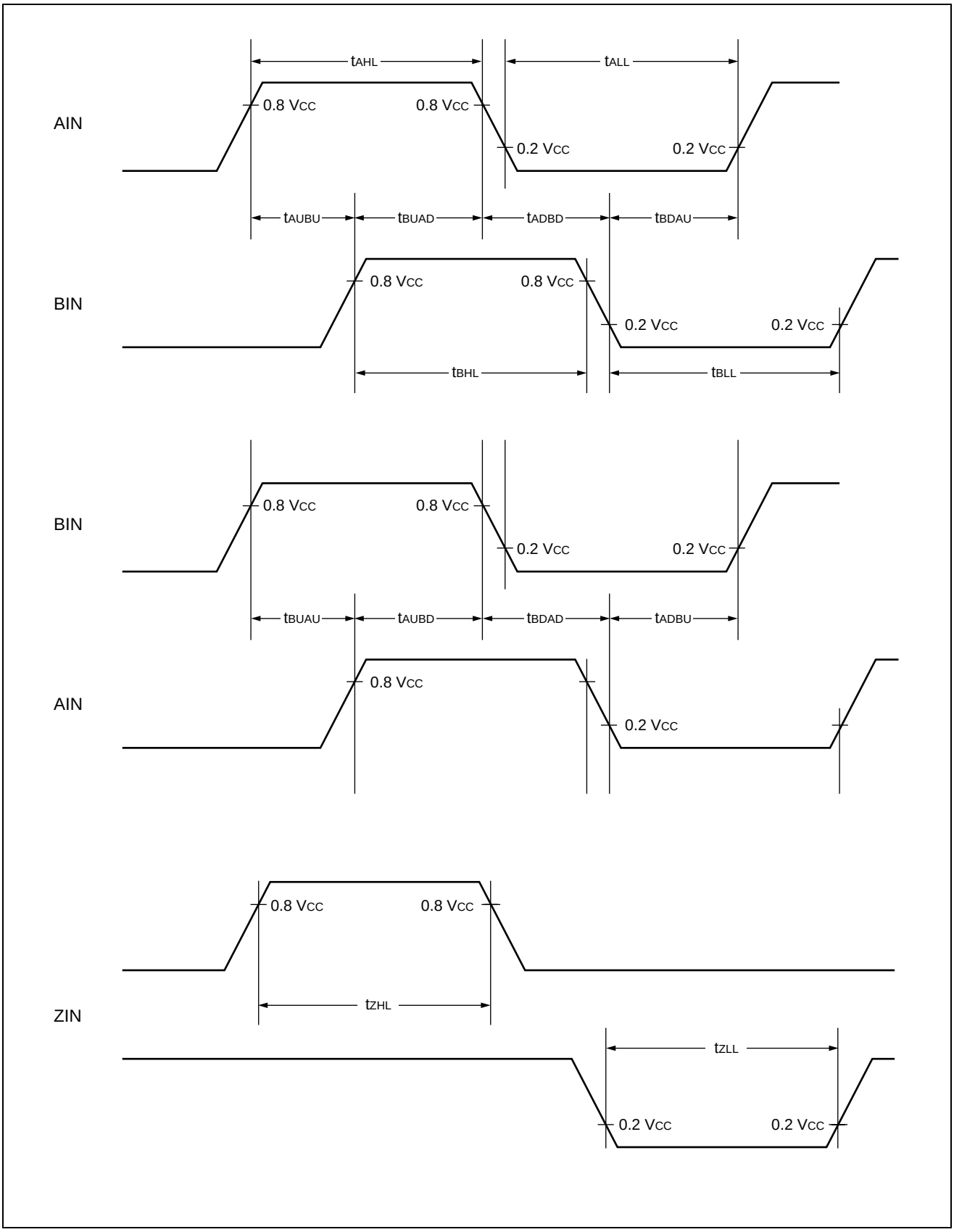

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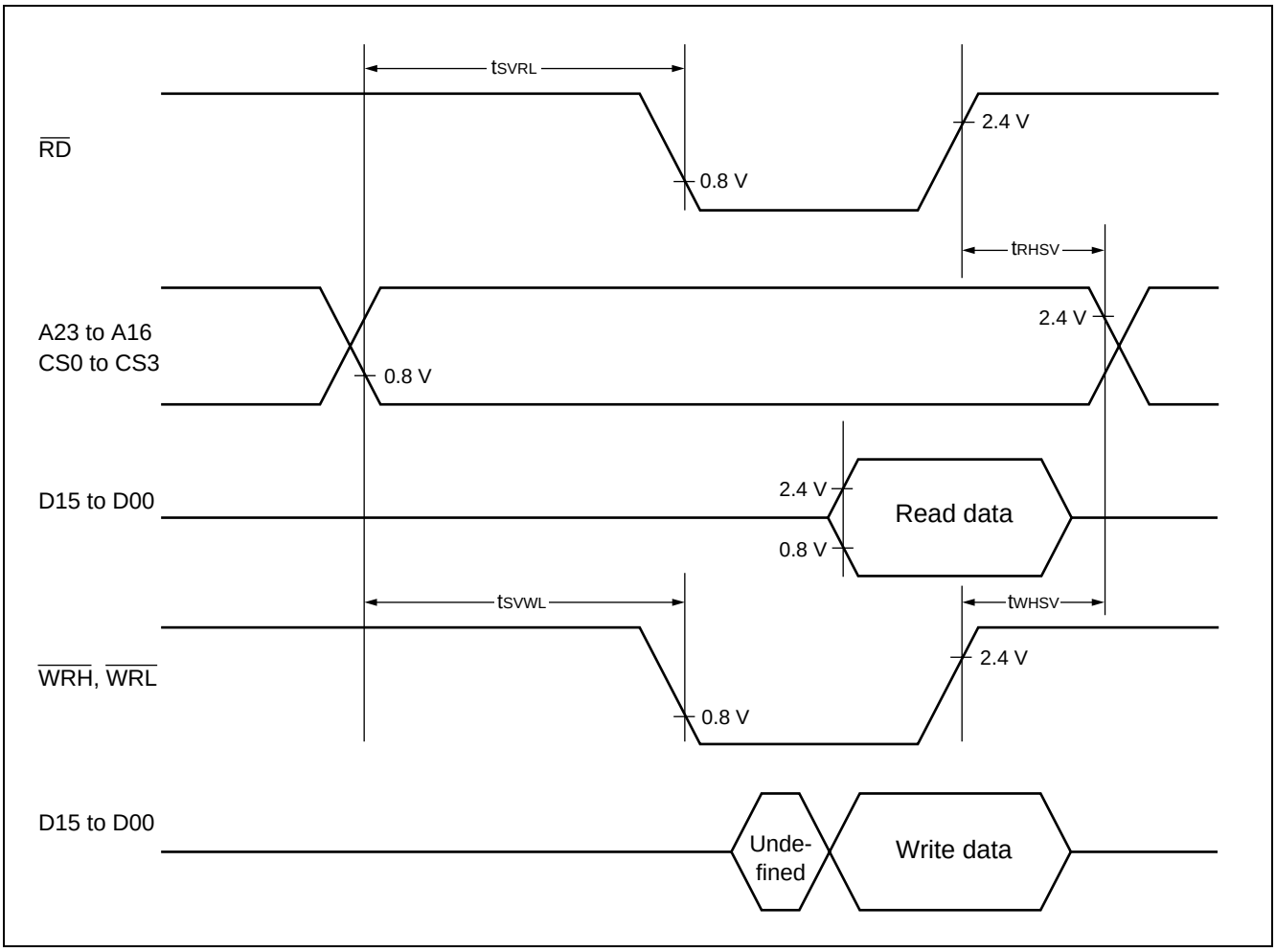
(16) Chip Select Output Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Chip select output valid time →$\overline{RD}$↓	t_{SVRL}	CS0 to CS3, $\overline{RD}$	—	t_{CP}* / 2 – 7	—	ns	
Chip select output valid time→$\overline{WR}$↓	t_{SVWL}	CS0 to CS3, $\overline{WRH}$, $\overline{WRL}$	—	t_{CP}* / 2 – 7	—	ns	
$\overline{RD}$↑→chip select output valid time	t_{RHSV}	$\overline{RD}$, CS0 to CS3	—	t_{CP}* / 2 – 17	—	ns	
$\overline{WR}$↑→chip select output valid time	t_{WHSV}	$\overline{WRH}$, $\overline{WRL}$, CS0 to CS3	—	t_{CP}* / 2 – 17	—	ns	

* : t_{CP} : See “ (1) Clock Timing Standards”.



Note : Due to the configuration of the internal bus, changes in the chip select output signal are clock synchronous and therefore may causes bus conflict conditions. AC cannot be warranted between the ALE output signal and the chip select output signal.

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5. A/D Converter Electrical Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, 2.7 V ≤ AVRH, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linear error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	mV	
Conversion time	—	—	3.68 *1	—	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVRH	V	
Reference voltage	—	AVRH	AV_{SS} + 2.2	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1.4	3.5	mA	
	I_{AH}	AV_{CC}	—	—	5 *2	µA	
Reference voltage supply current	I_R	AVRH	—	94	150	µA	
	I_{RH}	AVRH	—	—	5 *2	µA	
Offset between channels	—	AN0 to AN7	—	—	4	LSB	

*1 : At machine clock frequency of 25 MHz.

*2 : CPU stop mode current when A/D converter is not operating (at V_{CC} = AV_{CC} = AVRH = 3.0 V) .

(Continued)

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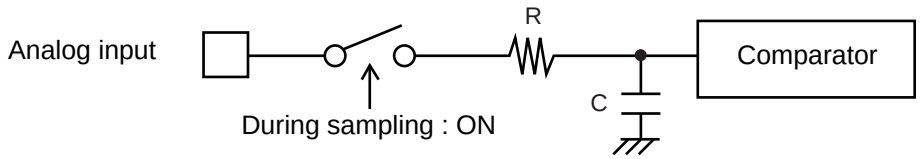
(Continued)

<About the external impedance of the analog input and its sampling time>

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

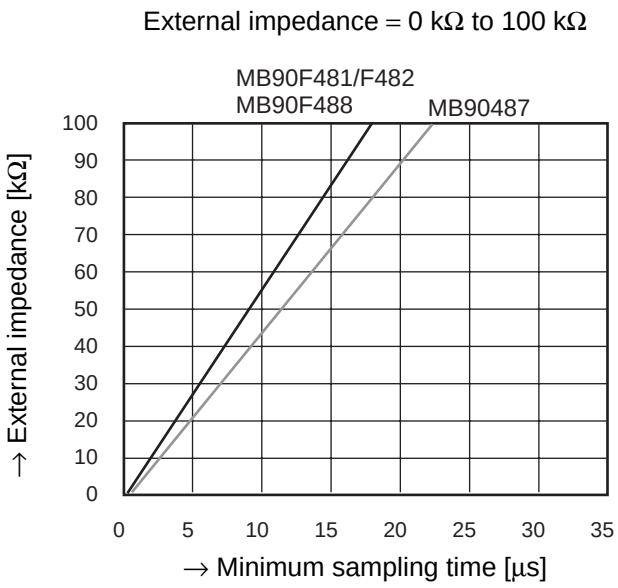
- Analog input circuit model

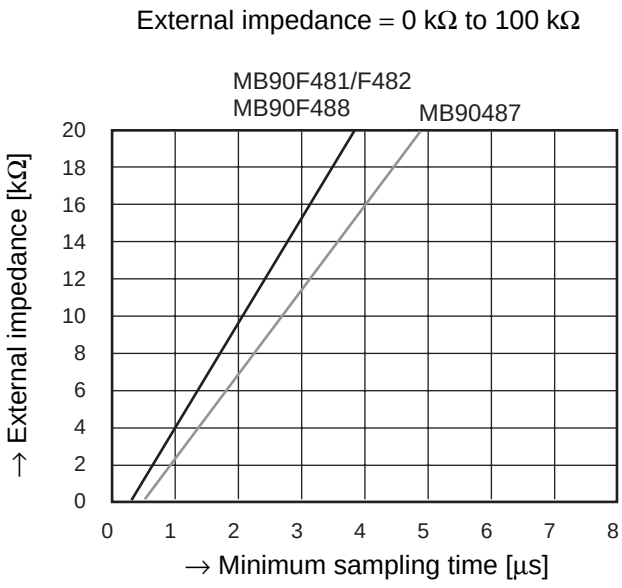


	R	C
MB90487	2.5 kΩ (Max)	31.0 pF (Max)
MB90F481/F482	1.9 kΩ (Max)	25.0 pF (Max)
MB90F488	1.9 kΩ (Max)	25.0 pF (Max)

Note: The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.





The relationship between external impedance and minimum sampling time

- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

<About errors>

As |AVRH – AV_{SS}| becomes smaller, values of relative errorsgrow larger.

Note : Concerning sampling time, and compare time When 3.6 V ≥ AV_{CC} ≥ 2.7 V, then

Sampling time : 1.92 µs, compare time : 1.1 µs

Settings should ensure that actual values do not go below these values due to operating frequency changes.

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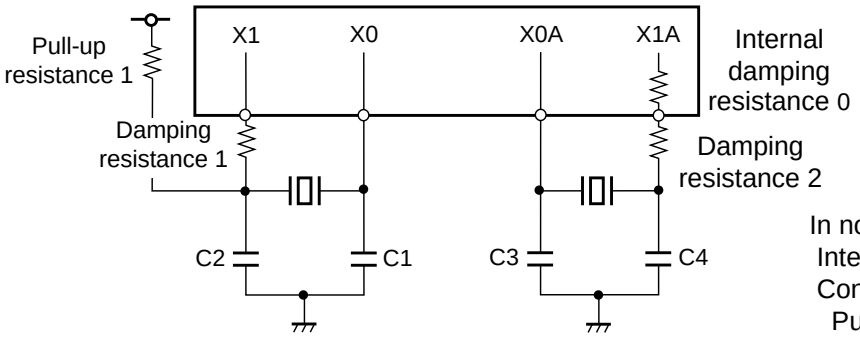
- Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C, V_{CC} = 3.0 V	—	1	15	s	Excludes 00_H programming prior erasure
Chip erase time		—	7	—	s	Excludes 00_H programming prior erasure
Word (16-bit) programming time		—	16	3,600	µs	Excludes system-level overhead
Program/Erase cycle	—	10,000	—	—	cycle	
Data hold time	—	100,000	—	—	h	

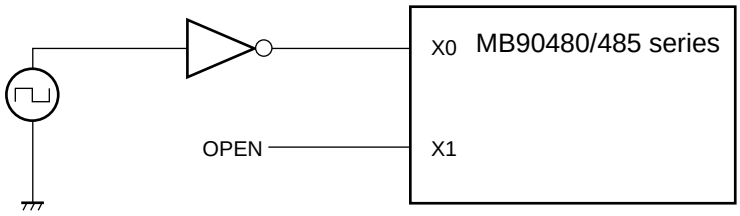
- Use of the X0/X1, X0A/X1A pins

When used with a crystal oscillator



In normal use :
Internal damping resistance 1 : Typ 600 Ω
Consult with the oscillator manufacturer.
Pull-up resistance 1,
Damping resistance 1, 2,
C1 to C4

- Sample use with external clock input



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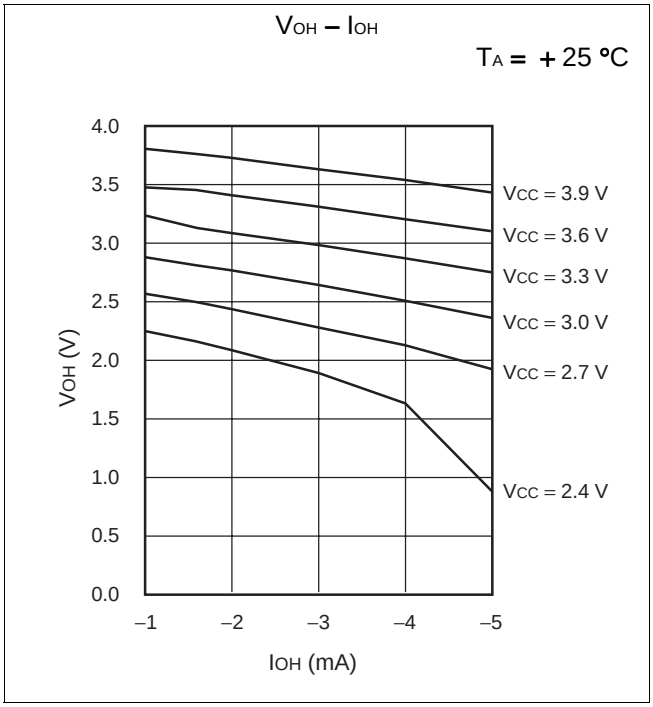
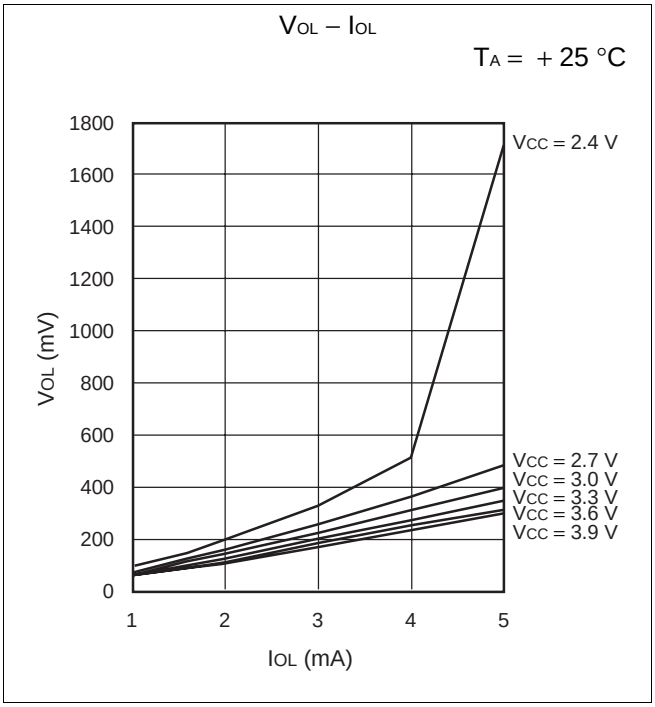
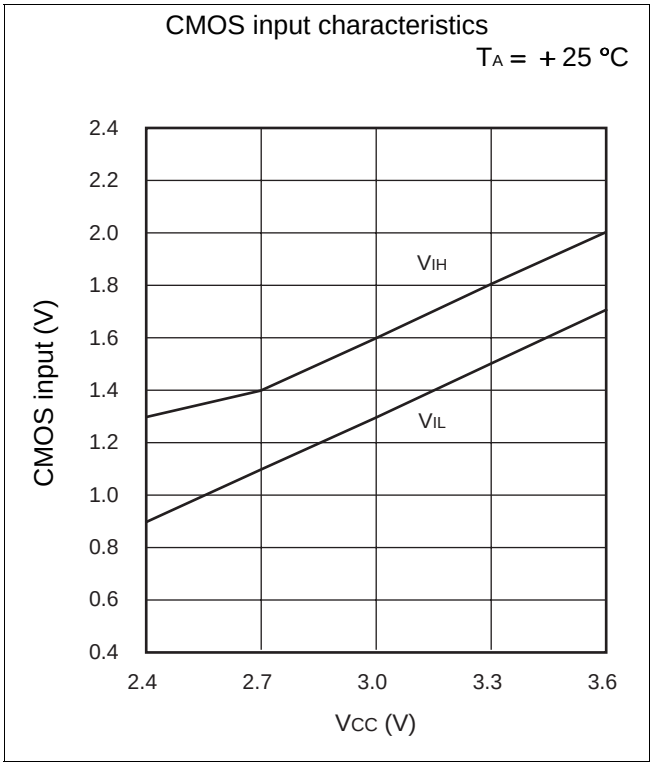
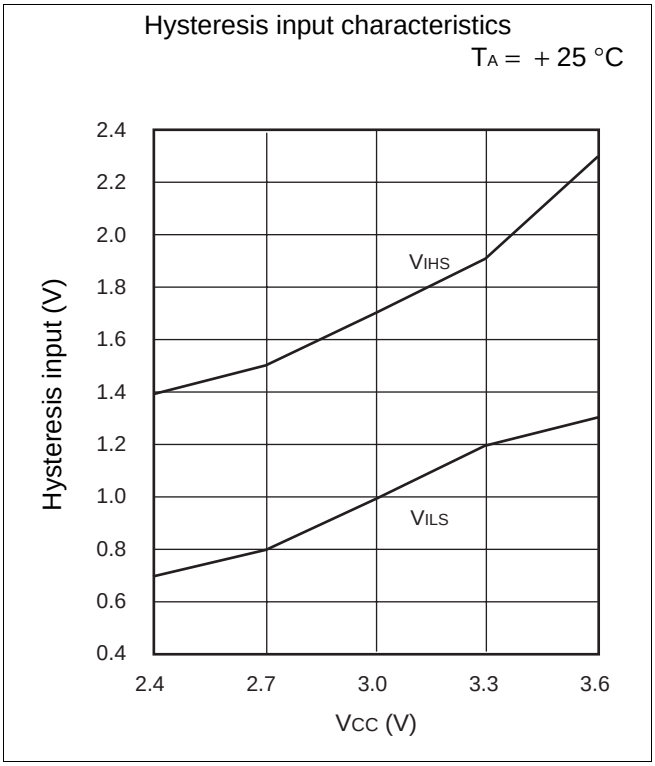
■ EXAMPLE CHARACTERISTICS









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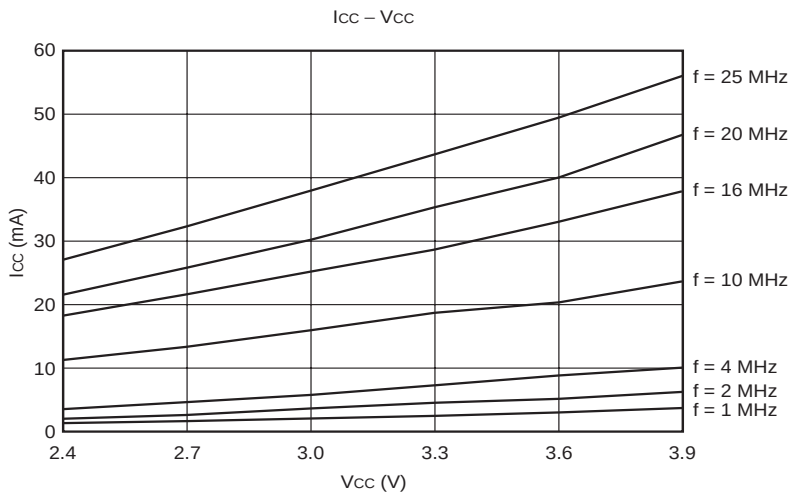

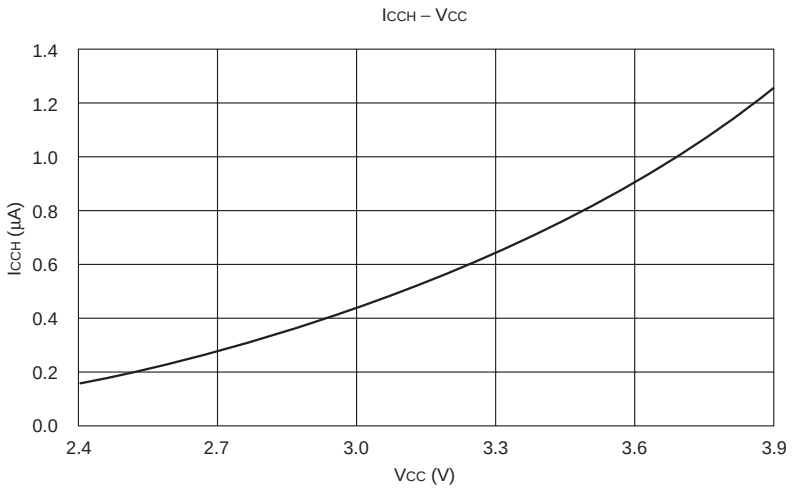

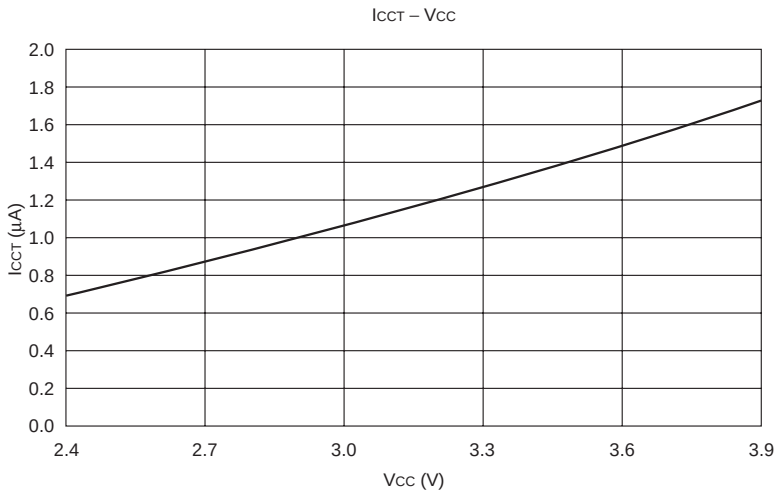

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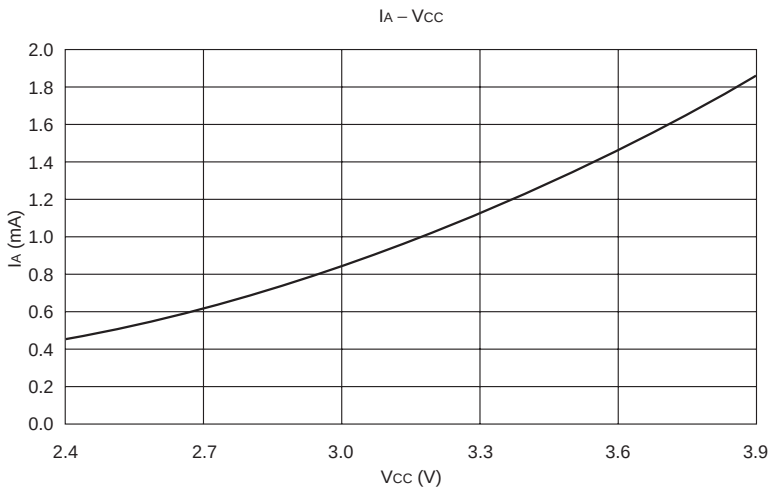

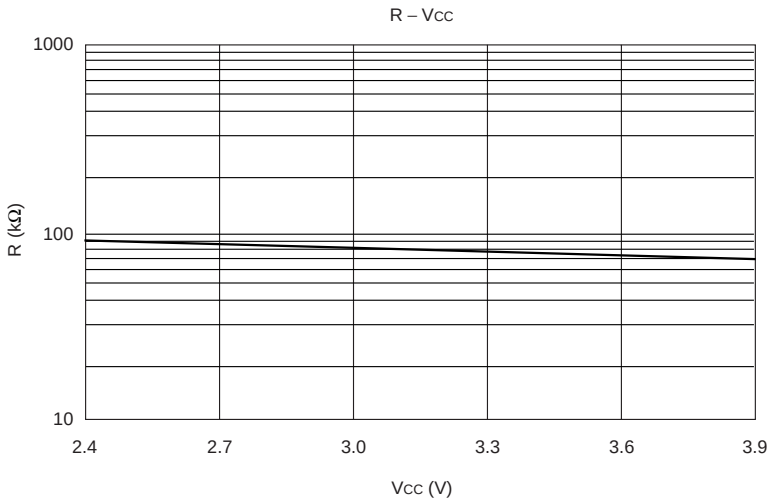

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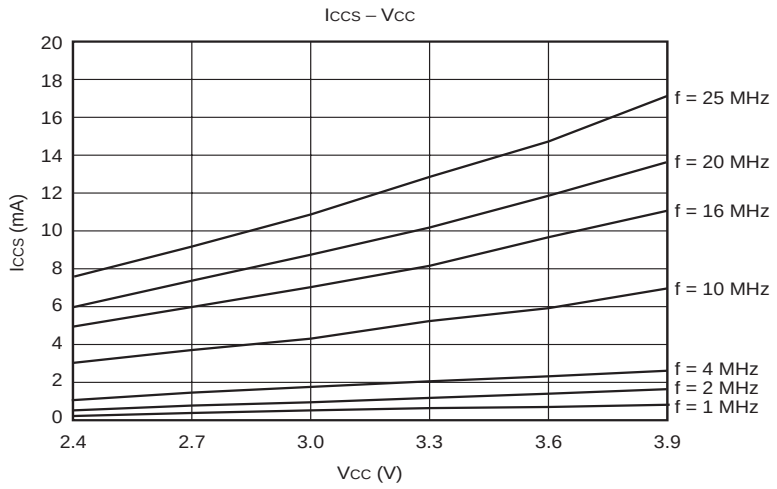

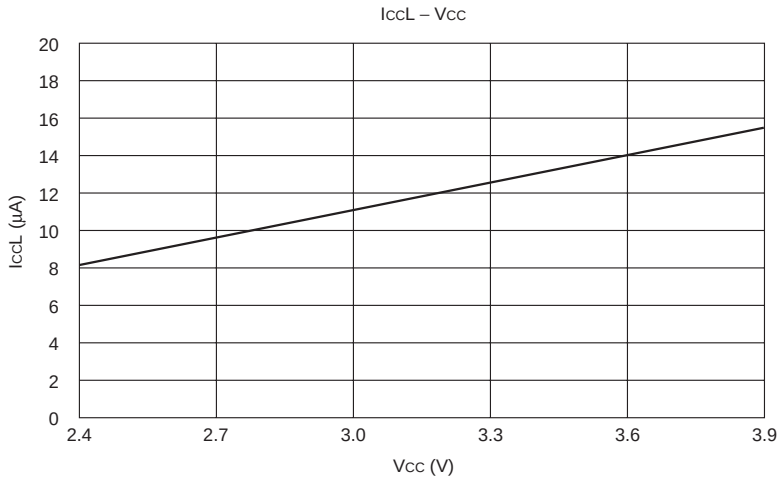

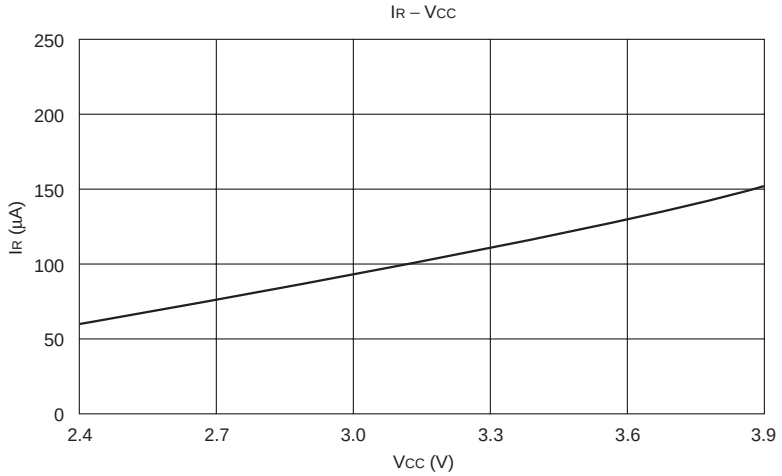

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■ ORDERING INFORMATION

Model	Package	Remarks
MB90F481PF MB90F482PF MB90487PF MB90F488PF	100-pin plastic QFP (FPT-100P-M06)	
MB90F481PFV MB90F482PFV MB90487PFV MB90F488PFV	100-pin plastic LQFP (FPT-100P-M05)	

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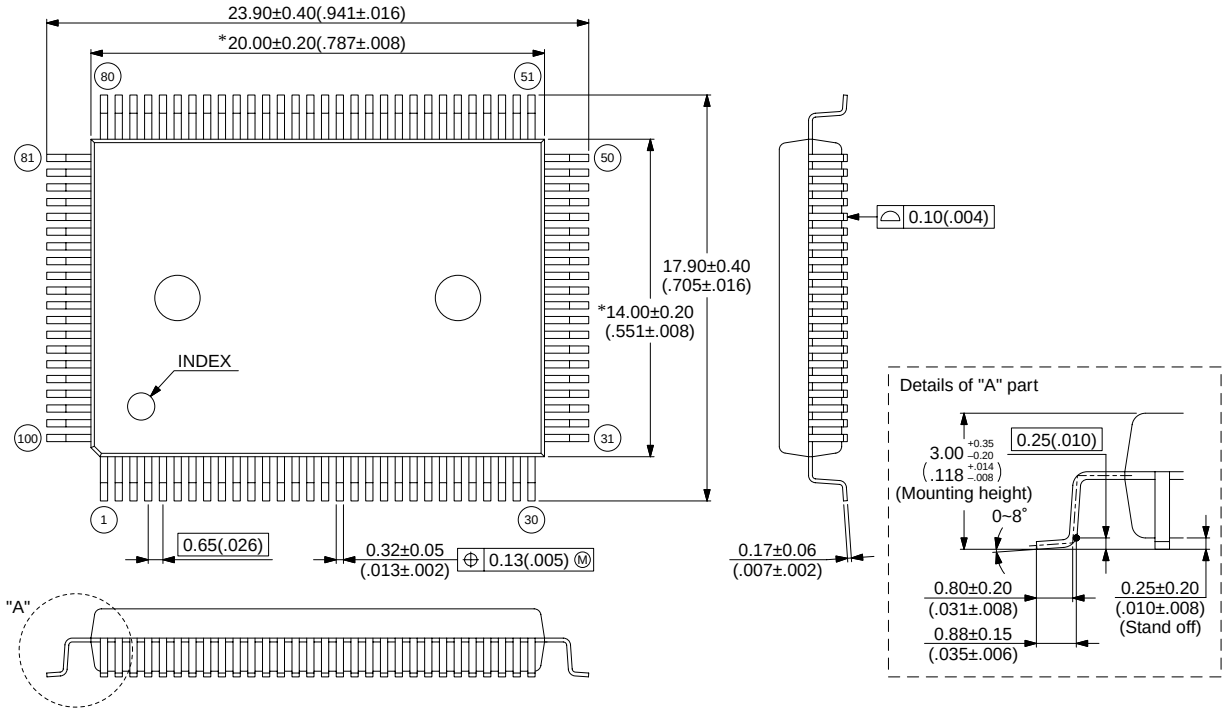
■ PACKAGE DIMENSIONS

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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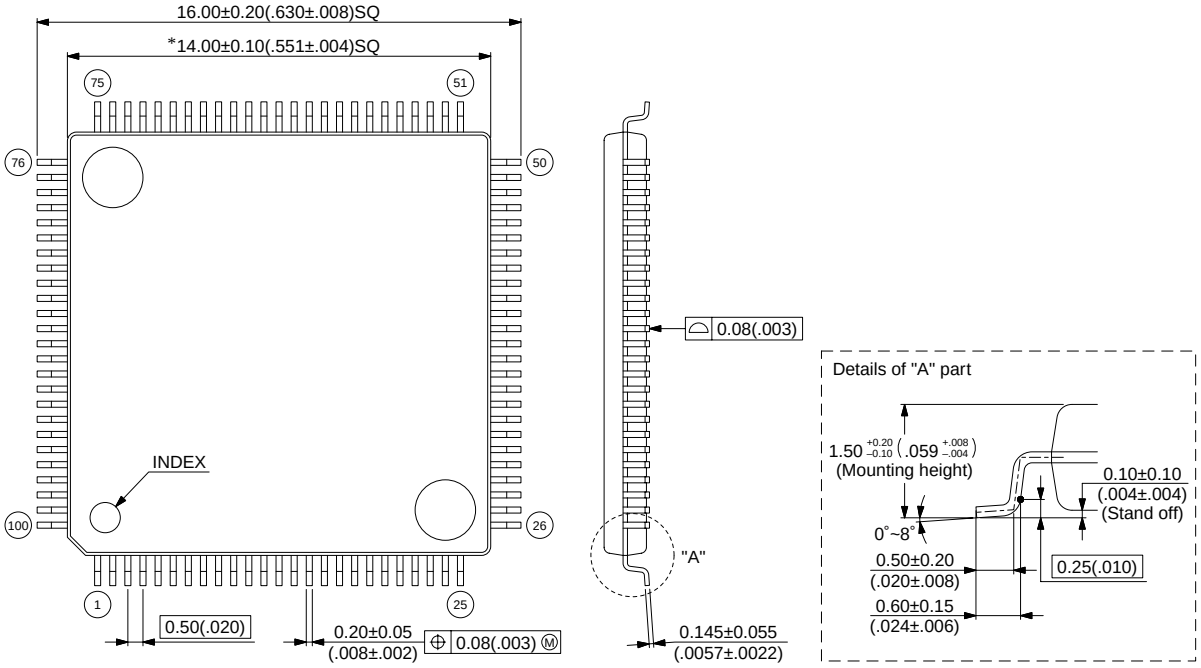
(Continued)

100-pin plastic LQFP
(FPT-100P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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