June 2007

ADC08500
High Performance, Low Power 8-Bit, 500 MSPS A/D Converter

General Description

The ADC08500 is a low power, high performance CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 500 MSPS. Consuming a typical 0.8 Watts at 500 MSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist, producing a high 7.5 ENOB with a 250 MHz input signal and a 500 MHz sample rate while providing a 10^{-18} B.E.R. Output formatting is offset binary and the LVDS digital outputs are compatible with IEEE 1596.3-1996, with the exception of an adjustable common mode voltage between 0.8V and 1.2V.

The converter has a 1:2 demultiplexer that feeds two LVDS buses and reduces the output data rate on each bus to half the sampling rate.

The converter typically consumes less than 3.5 mW in the Power Down Mode and is available in a 128-lead, thermally enhanced exposed pad LQFP and operates over the Industrial (-40°C ≤ T_A ≤ +85°C) temperature range.

Features

- Internal Sample-and-Hold
- Single +1.9V ±0.1V Operation
- Choice of SDR or DDR output clocking
- Multiple ADC Synchronization Capability
- Guaranteed No Missing Codes
- Serial Interface for Extended Control
- Fine Adjustment of Input Full-Scale Range and Offset
- Duty Cycle Corrected Sample Clock

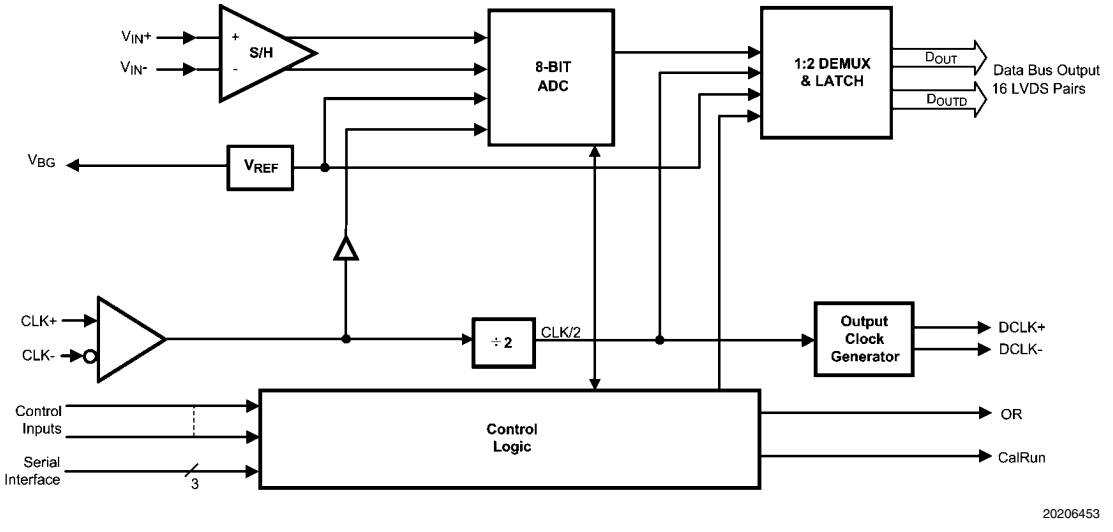
Key Specifications

■ Resolution	8 Bits
■ Max Conversion Rate	500 MSPS (min)
■ Bit Error Rate	10^{-18} (typ)
■ ENOB @ 250 MHz Input	7.5 Bits (typ)
■ DNL	±0.15 LSB (typ)
■ Power Consumption	
■ — Operating	0.8 W (typ)
— Power Down Mode	3.5 mW (typ)

Applications

- Direct RF Down Conversion
- Digital Oscilloscopes
- Satellite Set-top boxes
- Communications Systems
- Test Instrumentation

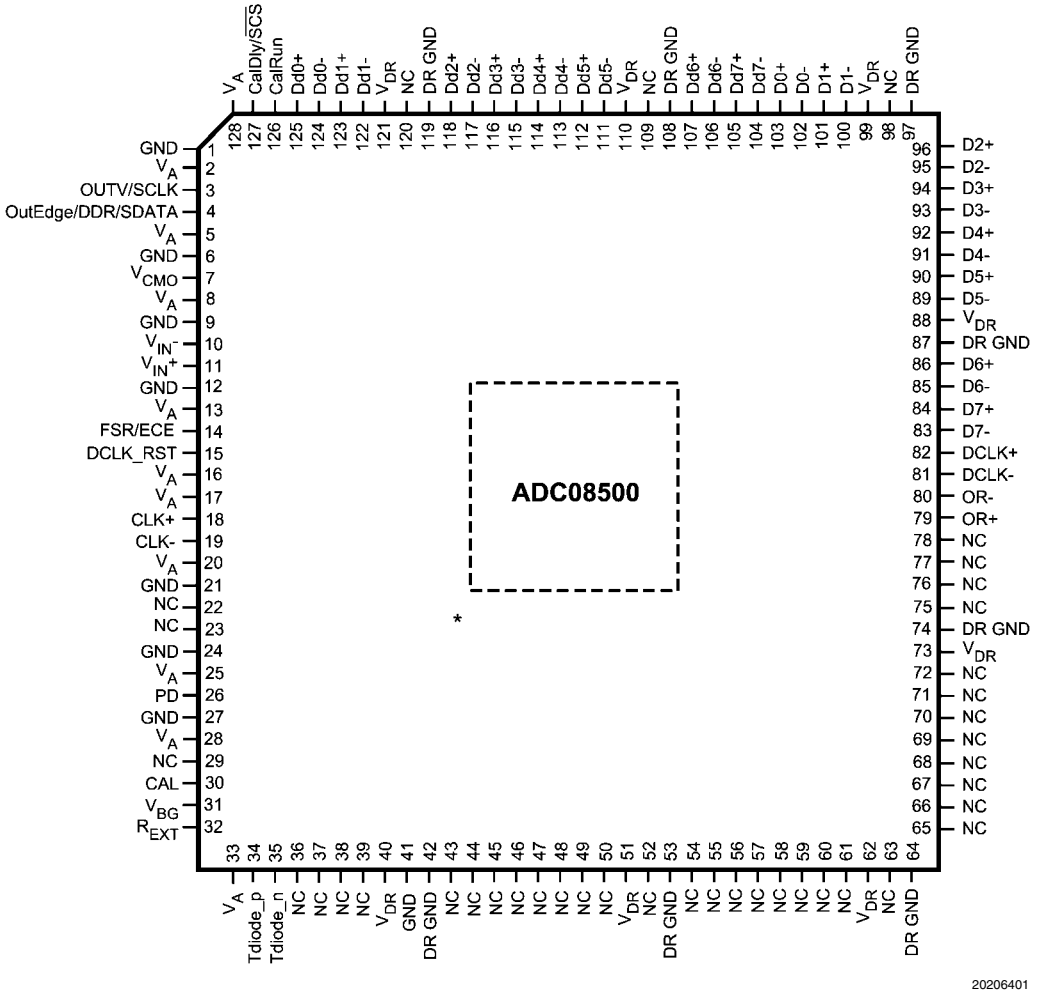
Block Diagram



Ordering Information

Industrial Temperature Range ($-40°C < T_A < +85°C$)	NS Package
ADC08500CIYB	128-Pin Exposed Pad LQFP
ADC08500DEV	Development Board

Pin Configuration



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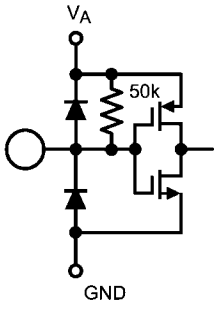
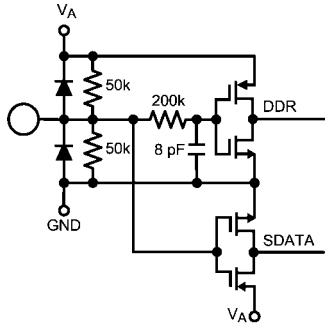
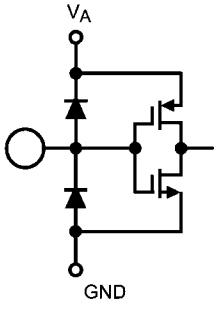
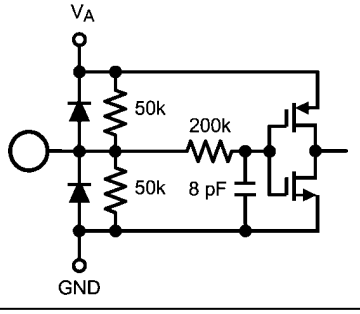
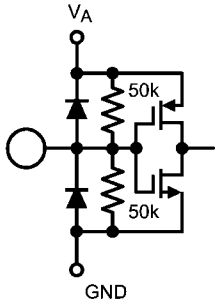
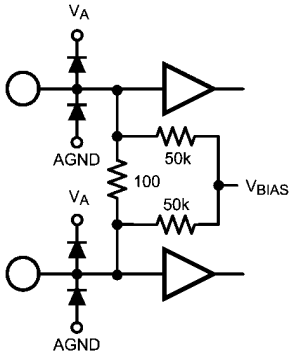
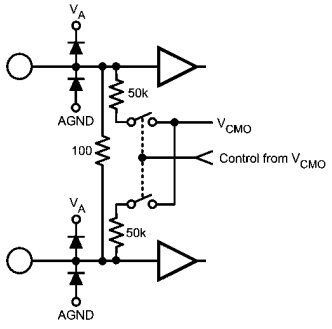
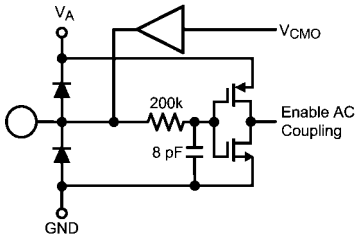
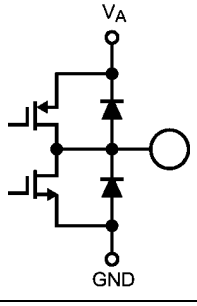
* Exposed pad on back of package must be soldered to ground plane to ensure rated performance.

Pin Descriptions and Equivalent Circuits

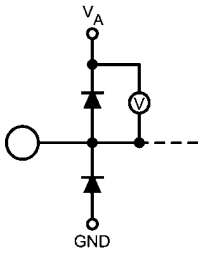
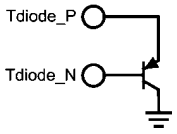
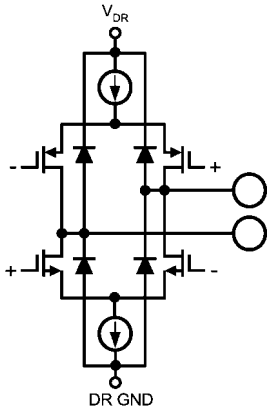
Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
3	OutV / SCLK		Output Voltage Amplitude and Serial Interface Clock. Tie this pin high for normal differential DCLK and data amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. See *1.1.6 The LVDS Outputs*. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data. See *1.2 NORMAL/EXTENDED CONTROL* for details on the extended control mode. See *1.3 THE SERIAL INTERFACE* for description of the serial interface.
4	OutEdge / DDR / SDATA		DCLK Edge Select, Double Data Rate Enable and Serial Data Input. This input sets the output edge of DCLK+ at which the output data transitions. When this pin is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. See *1.1.5.2 Double Data Rate*. When the extended control mode is enabled, this pin functions as the SDATA input. See *1.2 NORMAL/EXTENDED CONTROL* for details on the extended control mode. See *1.3 THE SERIAL INTERFACE* for description of the serial interface.
15	DCLK_RST		DCLK Reset. A positive pulse on this pin is used to reset and synchronize the DCLK outs of multiple converters. See *1.5 MULTIPLE ADC SYNCHRONIZATION* for detailed description.
26	PD		Power Down Pin. A logic high on the PD pin puts the entire device into the Power Down Mode.
30	CAL		Calibration Cycle Initiate. A minimum t_{CAL_L} input clock cycles logic low followed by a minimum of t_{CAL_H} input clock cycles high on this pin initiates the self calibration sequence. See *2.4.2 Self Calibration* for an overview of self-calibration and *2.4.2.2 On-Command Calibration* for a description of on-command calibration.
14	FSR/ECE		Full Scale Range Select and Extended Control Enable. In non-extended control mode, a logic low on this pin sets the full-scale differential input range to a reduced V_{IN} input level . A logic high on this pin sets the full-scale differential input range to a higher V_{IN} input level. See Converter Electrical Characteristics. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$. See *1.2 NORMAL/EXTENDED CONTROL* for information on the extended control mode.

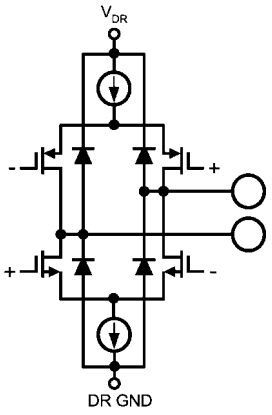
Pin Functions

Pin No	Symbol	Equivalent Circuit	Description
127	CalDly / $\overline{SCS}$		Calibration Delay and Serial Interface Chip Select. With a logic high or low on pin 14, this pin functions as Calibration Delay and sets the number of clock cycles after power up before calibration begins. See *1.1.1 Self-Calibration*. With pin 14 floating, this pin acts as the enable pin for the serial interface input and the CalDly value becomes "0" (short delay with no provision for a long power-up calibration delay).
18 19	CLK+ CLK-		LVDS Clock input pins for the ADC. The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on the falling edge of CLK+. See *1.1.2 Acquiring the Input* for a description of acquiring the input and *2.3 THE CLOCK INPUTS* for an overview of the clock inputs.
11 10	V_{IN}+ V_{IN}–		Analog signal inputs to the ADC. The differential full-scale input range of this input is programmable using the FSR pin 14 in normal mode and the Input Full-Scale Voltage Adjust register in the extended control mode. Refer to the V_{IN} specification in the Converter Electrical Characteristics for the full-scale input range in the normal mode. Refer to *1.4 REGISTER DESCRIPTION* for the full-scale input range in the extended control mode.
7	V_{CMO}		Common Mode Voltage. This pin is the common mode output in d.c. coupling mode and also serves as the a.c. coupling mode select pin. When d.c. coupling is used, the voltage output at this pin is required to be the common mode input voltage at V_{IN}+ and V_{IN}– when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog inputs. This pin is capable of sourcing or sinking 100 µA. See *2.2 THE ANALOG INPUT*.
31	V_{BG}		Bandgap output voltage capable of 100 µA source/sink.
126	CalRun		Calibration Running indication. This pin is at a logic high when calibration is running.

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
32	R_{EXT}		External bias resistor connection. Nominal value is 3.3 kOhms (±0.1%) to ground. See *1.1.1 Self-Calibration*.
34 35	Tdiode_P Tdiode_N		Temperature Diode Positive (Anode) and Negative (Cathode) for die temperature measurements. See *2.6.2 Thermal Management*.
83 84 85 86 89 90 91 92 93 94 95 96 100 101 102 103	D7- D7+ D6- D6+ D5- D5+ D4- D4+ D3- D3+ D2- D2+ D1- D1+ D0- D0+		Input channel LVDS Data Outputs that are not delayed in the output demultiplexer. Compared with the Dd outputs, these outputs represent the later time samples. These outputs should always be terminated with a 100Ω differential resistor.
104 105 106 107 111 112 113 114 115 116 117 118 122 123 124 125	Dd7- Dd7+ Dd6- Dd6+ Dd5- Dd5+ Dd4- Dd4+ Dd3- Dd3+ Dd2- Dd2+ Dd1- Dd1+ Dd0- Dd0+		Input channel LVDS Data Outputs that are delayed by one CLK cycle in the output demultiplexer. Compared with the D outputs, these outputs represent the earlier time sample. These outputs should always be terminated with a 100Ω differential resistor.

Pin Functions

Pin No	Symbol	Equivalent Circuit	Description
79 80	OR+ OR-		Out Of Range output. A differential high at these pins indicates that the differential input is out of range (outside the range $\pm V_{IN}/2$ as programmed by the FSR pin in non-extended control mode or the Input Full-Scale Voltage Adjust register setting in the extended control mode).
82 81	DCLK+ DCLK-		Differential Clock outputs used to latch the output data. Delayed and non-delayed data outputs are supplied synchronous to this signal. This signal is at 1/2 the input clock rate in SDR mode and at 1/4 the input clock rate in the DDR mode.The DCLK outputs are not active during a calibration cycle, therefore this is not recommended as a system clock.
2, 5, 8, 13, 16, 17, 20, 25, 28, 33, 128	V_A		Analog power supply pins. Bypass these pins to ground.
40, 51 ,62, 73, 88, 99, 110, 121	V_{DR}		Output Driver power supply pins. Bypass these pins to DR GND.
1, 6, 9, 12, 21, 24, 27, 41	GND		Ground return for V_A.
42, 53, 64, 74, 87, 97, 108, 119	DR GND		Ground return for V_{DR}.
22, 23, 29, 36–39, 43–50, 52, 54–61, 63, 65–72, 75–78, 98, 109, 120	NC		No Connection. Make no connection to these pins.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_{DR})	2.2V
Supply Difference V_{DR} - V_A	0V to 100 mV
Voltage on Any Input Pin	−0.15V to (V_A +0.15V)
Ground Difference |GND - DR GND|	0V to 100 mV
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at T_A = 85°C	2.0 W
ESD Susceptibility (Note 4)	
Human Body Model	2500V
Machine Model	250V
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1, 2)

Ambient Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Analog Input Common Mode Voltage	V_{CMO} ±50 mV
V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	200 mV to V_A
Ground Difference |GND - DR GND|	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	0.4V_{P-P} to 2.0V_{P-P}

Package Thermal Resistance

Package	θ_{JA}	θ_{JC} (Top of Package)	θ_{J-PAD} (Thermal Pad)
128-Lead Exposed Pad LQFP	25°C / W	10°C / W	2.8°C / W

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 5)

Converter Electrical Characteristics

The following specifications apply after calibration for V_A = V_{DR} = +1.9V_{DC}, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential 870 mV_{P-P}, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 500 MHz at 0.5V_{P-P} with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity	DC Coupled, 1MHz Sine Wave Overanged	±0.3	**±0.9**	LSB (max)
DNL	Differential Non-Linearity	DC Coupled, 1MHz Sine Wave Overanged	±0.15	**±0.6**	LSB (max)
	Resolution with No Missing Codes			**8**	Bits
V_{OFF}	Offset Error		-0.5	**−1.5** **0.5**	LSB (min) LSB (max)
V_{OFF}_ADJ	Input Offset Adjustment Range	Extended Control Mode	±45		mV
PFSE	Positive Full-Scale Error (Note 9)			**±25**	mV (max)
NFSE	Negative Full-Scale Error (Note 9)			**±25**	mV (max)
FS_ADJ	Full-Scale Adjustment Range	Extended Control Mode	±20	**±15**	%FS
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth		1.7		GHz
B.E.R.	Bit Error Rate		10^{-18}		Error/Sample
	Gain Flatness	d.c. to 500 MHz	±0.5		dBFS
ENOB	Effective Number of Bits	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	7.5		Bits
		f_{IN} = 124 MHz, V_{IN} = FSR − 0.5 dB	7.5	**7.1**	Bits (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	7.5	**7.1**	Bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	47		dB
		f_{IN} = 124 MHz, V_{IN} = FSR − 0.5 dB	47	**44.5**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	47	**44.5**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	48		dB
		f_{IN} = 124 MHz, V_{IN} = FSR − 0.5 dB	47.5	**45.3**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	47.5	**45.3**	dB (min)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
THD	Total Harmonic Distortion	f_{IN} = 50 MHz, V_{IN} = FSR – 0.5 dB	-55		dB
		f_{IN} = 124 MHz, V_{IN} = FSR – 0.5 dB	-56	**–47.5**	dB (max)
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	-56	**–47.5**	dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 50 MHz, V_{IN} = FSR – 0.5 dB	–60		dB
		f_{IN} = 124 MHz, V_{IN} = FSR – 0.5 dB	–60		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	–60		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 50 MHz, V_{IN} = FSR – 0.5 dB	–65		dB
		f_{IN} = 124 MHz, V_{IN} = FSR – 0.5 dB	–65		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	–65		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 50 MHz, V_{IN} = FSR – 0.5 dB	55		dB
		f_{IN} = 124 MHz, V_{IN} = FSR – 0.5 dB	56	**47.5**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	56	**47.5**	dB (min)
IMD	Intermodulation Distortion	f_{IN1} = 121 MHz, V_{IN} = FSR – 7 dB f_{IN2} = 126 MHz, V_{IN} = FSR – 7 dB	-50		dB
	Out of Range Output Code (In addition to OR Output high)	(V_{IN}+) – (V_{IN}–) > + Full Scale		**255**	
		(V_{IN}+) – (V_{IN}–) < – Full Scale		**0**	
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Full Scale Analog Differential Input Range	FSR pin 14 Low	650	**570**	mV_{P-P} (min)
				730	mV_{P-P} (max)
		FSR pin 14 High	870	**790**	mV_{P-P} (min)
				950	mV_{P-P} (max)
V_{CMI}	Analog Input Common Mode Voltage		V_{CMO}	**V_{CMO} – 50** **V_{CMO} + 50**	mV (min) mV (max)
C_{IN}	Analog Input Capacitance, Normal operation (Notes 10, 11)	Differential	0.02		pF
		Each input pin to ground	1.6		pF
R_{IN}	Differential Input Resistance		100	**94**	Ω (min)
				106	Ω (max)
ANALOG OUTPUT CHARACTERISTICS					
V_{CMO}	Common Mode Output Voltage	I_{CMO} = ±100 µA	1.26	**0.95** **1.45**	V (min) V (max)
V_{CMO_LVL}	V_{CMO} input threshold to set DC Coupling mode	V_A = 1.8V	0.60		V
		V_A = 2.0V	0.66		V
TC V_{CMO}	Common Mode Output Voltage Temperature Coefficient	T_A = –40°C to +85°C	118		ppm/°C
C_{LOAD} V_{CMO}	Maximum V_{CMO} load Capacitance			80	pF
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.26	**1.20** **1.33**	V (min) V (max)
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = –40°C to +85°C I_{BG} = ±100 µA	28		ppm/°C
C_{LOAD} V_{BG}	Maximum Bandgap Reference Load Capacitance			80	pF
TEMPERATURE DIODE CHARACTERISTICS					
ΔV_{BE}	Temperature Diode Voltage	192 µA vs. 12 µA, T_J = 25°C	71.23		mV
		192 µA vs. 12 µA, T_J = 85°C	85.54		mV
CHANNEL-TO-CHANNEL CHARACTERISTICS					
	Offset Error Match		1		LSB

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
	Positive Full-Scale Error Match	Zero offset selected in Control Register	1		LSB
	Negative Full-Scale Error Match	Zero offset selected in Control Register	1		LSB
	Phase Matching (I,Q)	F_{IN} = 1.0 GHz	< 1		Degree
CLOCK INPUT CHARACTERISTICS					
V_{ID}	Differential Clock Input Level	Sine Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
		Square Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
I_I	Input Current	V_{IN} = 0 or V_{IN} = V_A	±1		µA
C_{IN}	Input Capacitance (Notes 10, 11)	Differential	0.02		pF
		Each input to ground	1.5		pF
DIGITAL CONTROL PIN CHARACTERISTICS					
V_{IH}	Logic High Input Voltage	(Note 12)		**0.85 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage	(Note 12)		**0.15 x V_A**	V (max)
C_{IN}	Input Capacitance (Notes 11, 13)	Each input to ground	1.2		pF
DIGITAL OUTPUT CHARACTERISTICS					
V_{OD}	LVDS Differential Output Voltage	Measured differentially, OutV = V_A, V_{BG} = Floating, (Note 15)	710	**400**	mV_{P-P} (min)
				920	mV_{P-P} (max)
		Measured differentially, OutV = GND, V_{BG} = Floating, (Note 15)	510	**280**	mV_{P-P} (min)
				720	mV_{P-P} (max)
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels		±1		mV
V_{OS}	Output Offset Voltage, see *Figure 1*	V_{BG} = Floating	800		mV
V_{OS}	Output Offset Voltage, see *Figure 1*	V_{BG} = V_A (Note 15)	1200		mV
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±1		mV
I_{OS}	Output Short Circuit Current	Output+ & Output- connected to 0.8V	±4		mA
Z_O	Differential Output Impedance		100		Ohms
V_{OH}	Cal_Run H level output	I_{OH} = -400 uA (Note 12)	1.65	**1.5**	V
V_{OL}	Cal_Run L level output	I_{OH} = 400 uA (Note 12)	0.15	**0.3**	V
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = Low PD = High	340 1.8	**408**	mA (max) mA
I_{DR}	Output Driver Supply Current	PD = Low PD = High	112 0.012	**157**	mA (max) mA
P_D	Power Consumption	PD = Low PD = High	0.8 3.5	**1.0**	W (max) mW
PSRR1	D.C. Power Supply Rejection Ratio	Change in Full Scale Error with change in V_A from 1.8V to 2.0V	30		dB
PSRR2	A.C. Power Supply Rejection Ratio	248 MHz, 50mV_{P-P} riding on V_A	51		dB
AC ELECTRICAL CHARACTERISTICS					
f_{CLK1}	Maximum Input Clock Frequency			**500**	MHz (min)
f_{CLK2}	Minimum Input Clock Frequency		200		MHz
	Input Clock Duty Cycle	200 MHz ≤ Input clock frequency ≤ 800 MHz (Note 12)	50	20 80	% (min) % (max)
t_{CL}	Input Clock Low Time	(Note 12)	500	**400**	ps (min)
t_{CH}	Input Clock High Time	(Note 12)	500	**400**	ps (min)
	DCLK Duty Cycle	(Note 12)	50	**45** **55**	% (min) % (max)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
t_{RS}	Reset Setup Time	(Note 12)	150		ps
t_{RH}	Reset Hold Time	(Note 12)	250		ps
t_{SD}	Synchronizing Edge to DCLK Output Delay		$t_{OD} + t_{OSK}$		
t_{RPW}	Reset Pulse Width	(Note 11)		**4**	CLK± Cycles (min)
t_{LHT}	Differential Low to High Transition Time	10% to 90%, C_L = 2.5 pF	250		ps
t_{HLT}	Differential High to Low Transition Time	10% to 90%, C_L = 2.5 pF	250		ps
t_{OSK}	DCLK to Data Output Skew	50% of DCLK transition to 50% of Data transition, SDR Mode and DDR Mode, 0° DCLK (Note 12)	±50		ps (max)
t_{SU}	Data to DCLK Set-Up Time	DDR Mode, 90° DCLK (Note 12)	1.7		ns
t_H	DCLK to Data Hold Time	DDR Mode, 90° DCLK (Note 12)	1.9		ns
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data	1.3		ns
t_{AJ}	Aperture Jitter		0.4		ps rms
t_{OD}	Input Clock to Data Output Delay (in addition to Pipeline Delay)	50% of Input Clock transition to 50% of Data transition	3.1		ns
	Pipeline Delay (Latency) (Notes 11, 14)	D Outputs		**13**	CLK± Cycles
		Dd Outputs		**14**	
	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to get accurate conversion	1		CLK± Cycle
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)		500		ns
f_{SCLK}	Serial Clock Frequency	(Note 12)	100		MHz
t_{SSU}	Data to Serial Clock Setup Time	(Note 12)	2.5		ns (min)
t_{SH}	Data to Serial Clock Hold Time	(Note 12)	1		ns (min)
	Serial Clock Low Time			**4**	ns (min)
	Serial Clock High Time			**4**	ns (min)
t_{CAL}	Calibration Cycle Time		1.4×10^5		CLK± Cycles
t_{CAL_L}	CAL Pin Low Time	See *Figure 9* (Note 11)		80	CLK± Cycles (min)
t_{CAL_H}	CAL Pin High Time	See *Figure 9* (Note 11)		80	CLK± Cycles (min)
t_{CalDly}	Calibration delay determined by CalDly (pin 127)	CalDly = Low See *1.1.1 Self-Calibration*, *Figure 9*, (Note 15)		2^{25}	CLK± Cycles (min)
		CalDly = High See *1.1.1 Self-Calibration*, *Figure 9*, (Note 15)		2^{31}	CLK± Cycles (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

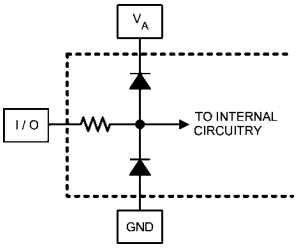
Note 2: All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power, ground and digital output pins.

Note 4: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Note 5: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 6: The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



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Note 7: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.

Note 8: Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See Transfer Characteristic *Figure 2*. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Note 10: The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 11: This parameter is guaranteed by design and is not tested in production.

Note 12: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 13: The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 14: The ADC08500 has two LVDS output buses, which each clock data out at one half the sample rate. The data at each bus is clocked out at one half the sample rate. The second bus (D0 through D7) has a pipeline latency that is one clock cycle less than the latency of the first bus (Dd0 through Dd7)

Note 15: Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 400 mv (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40mV (typical).

Specification Definitions

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the CLK input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

Bit Error Rate (B.E.R.) is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time. A B.E.R. of 10^{-18} corresponds to a statistical error in one word about every four (4) years.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at sample rate = 500 MSPS with a 1MHz input sinewave.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

Positive Gain Error = Offset Error – Positive Full-Scale Error

Negative Gain Error = –(Offset Error – Negative Full-Scale Error)

Gain Error = Negative Full-Scale Error – Positive Full-Scale Error = Positive Gain Error + Negative Gain Error

INTEGRAL NON-LINEARITY (INL) is a measure of worst case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value step. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^n$$

where V_{FS} is the differential full-scale amplitude V_{IN} as set by the FSR input and "n" is the ADC resolution in bits, which is 8 for the ADC08500.

LVDS DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) is the absolute value of the difference between the V_D+ & V_D- outputs; each measured with respect to Ground.

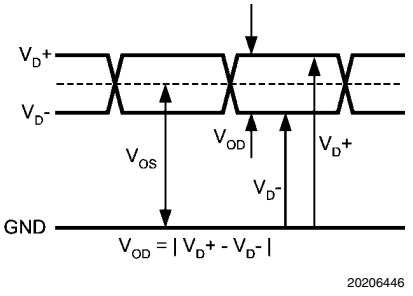


FIGURE 1.

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage referenced to ground. ie., $[(V_D+) + (V_D-)]/2$.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential $-V_{IN}/2$. For the ADC08500 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 127.5.

OUTPUT DELAY (t_{OD}) is the time delay after the falling edge of DCLK before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential $+V_{IN}/2$. For the ADC08500 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 50 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

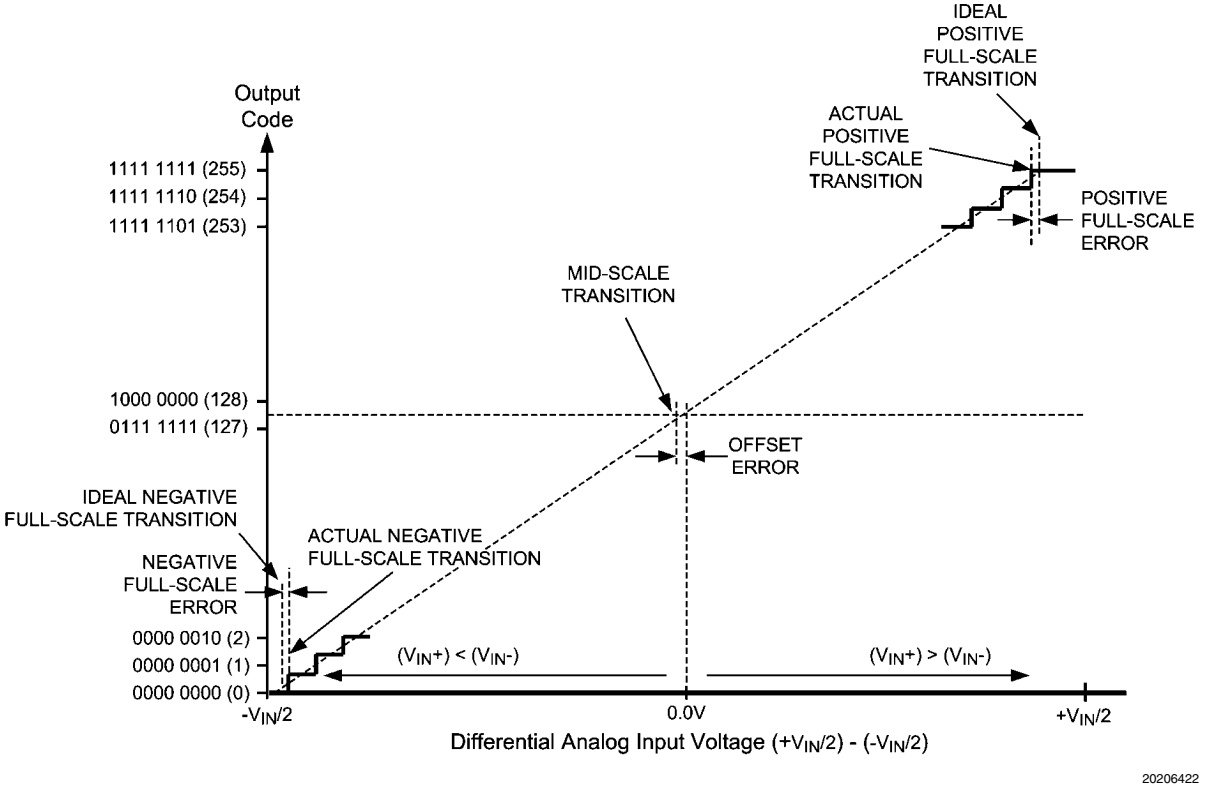


FIGURE 2. Input / Output Transfer Characteristic

Timing Diagrams

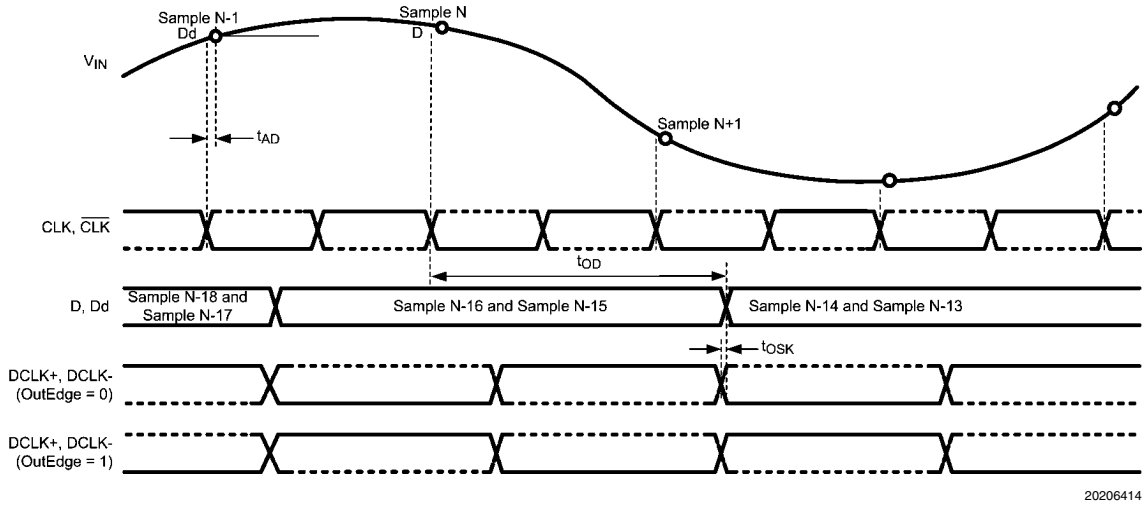


FIGURE 3. ADC08500 Timing — SDR Clocking

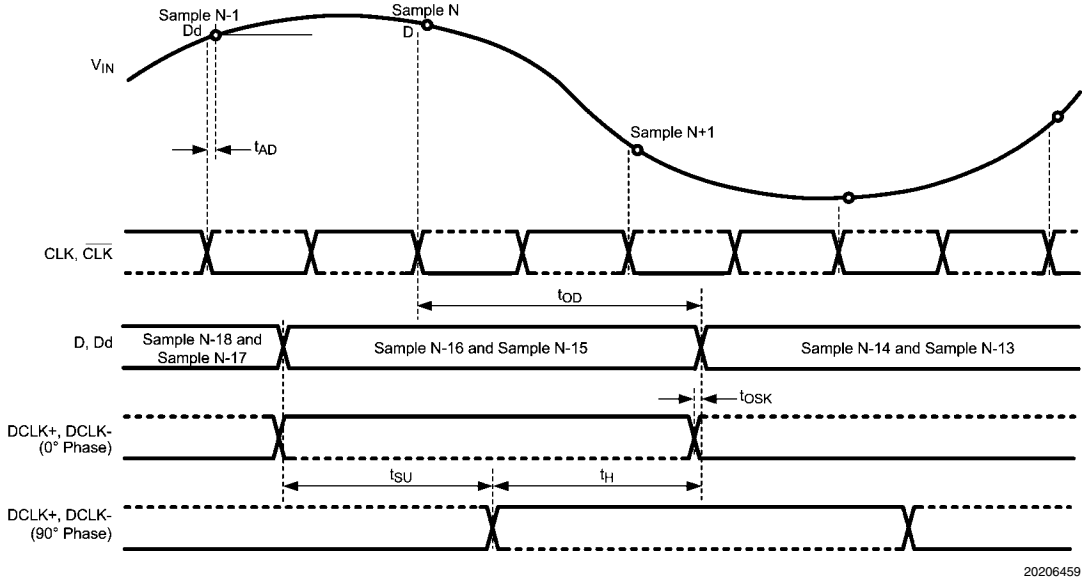


FIGURE 4. ADC08500 Timing — DDR Clocking

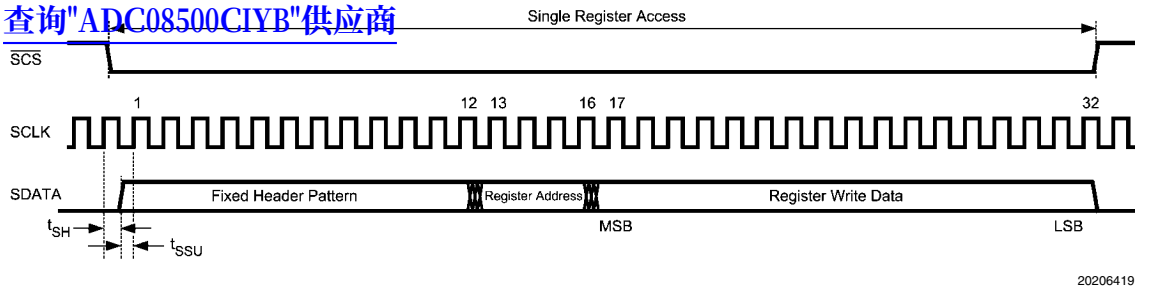


FIGURE 5. Serial Interface Timing

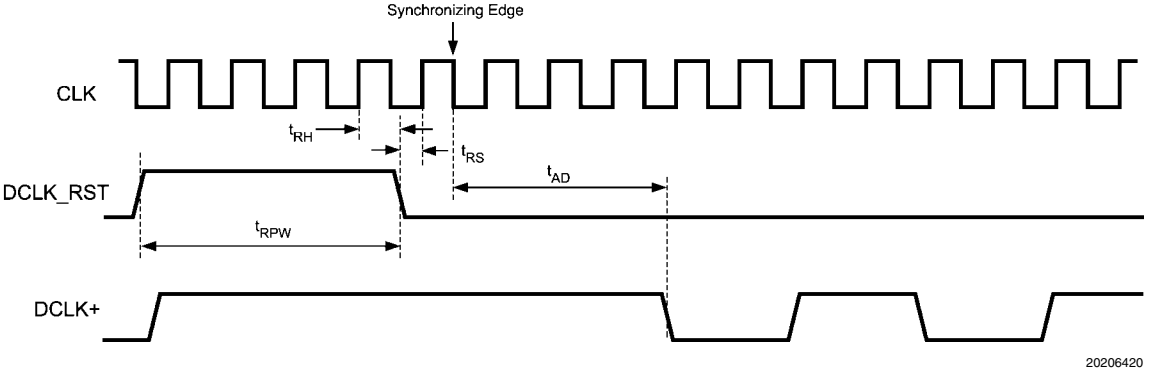


FIGURE 6. Clock Reset Timing in DDR Mode

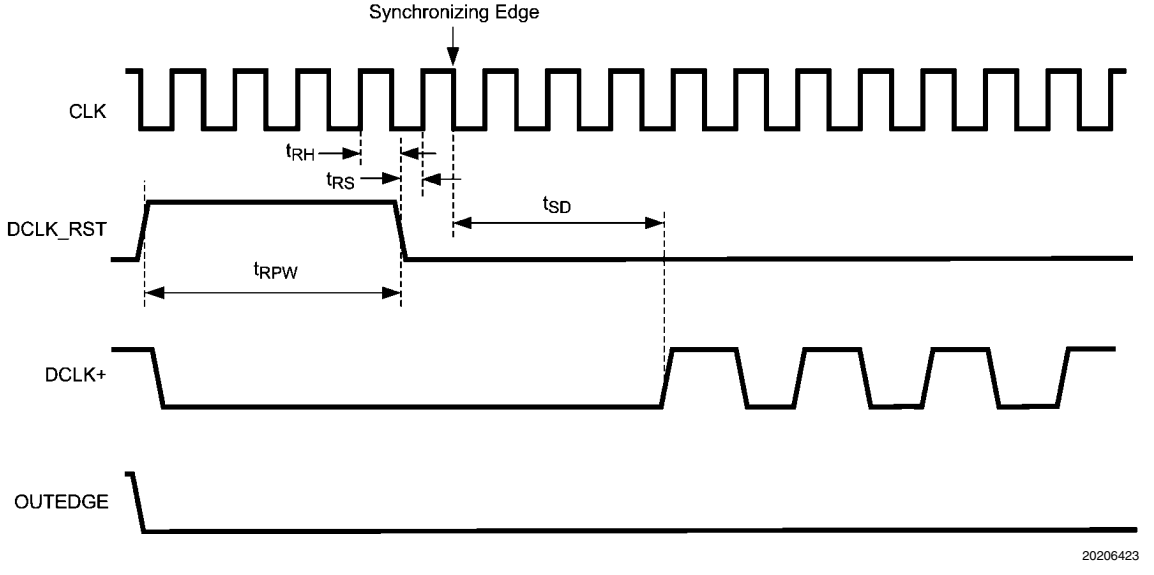


FIGURE 7. Clock Reset Timing in SDR Mode with OUTEDGE Low

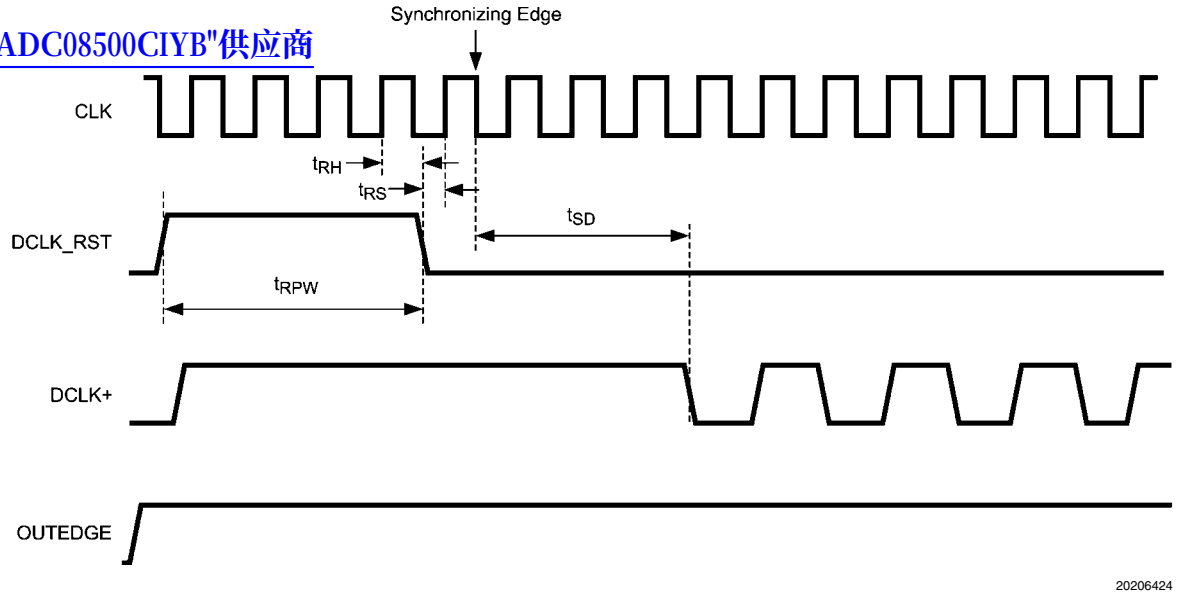


FIGURE 8. Clock Reset Timing in SDR Mode with OUTEDGE High

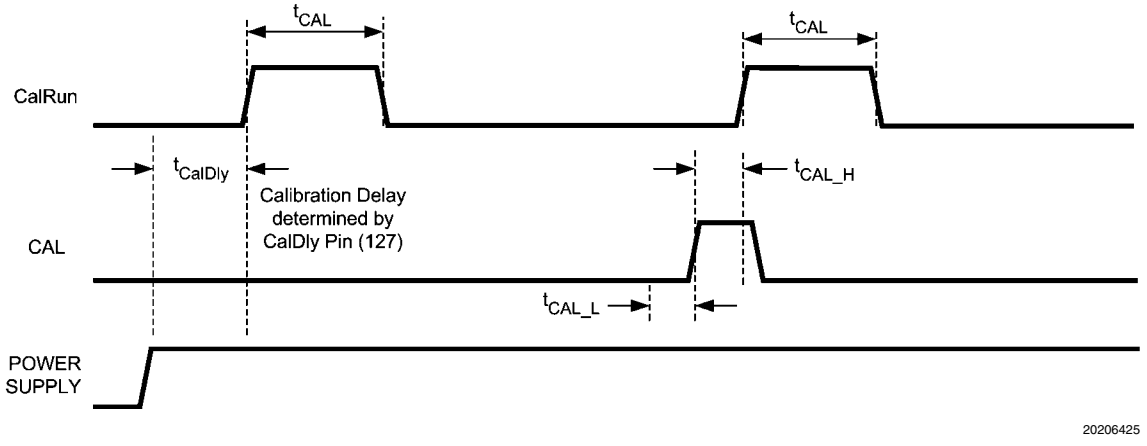
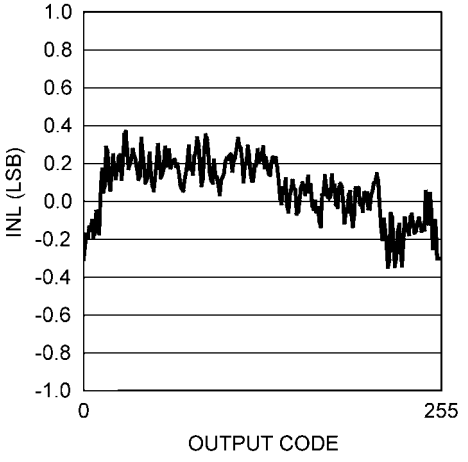


FIGURE 9. Self Calibration and On-Command Calibration Timing

Typical Performance Characteristics

$V_A = V_{DR} = 1.9V$, $f_{CLK} = 500$ MHz, $T_A = 25°C$ unless otherwise stated.

INL vs CODE



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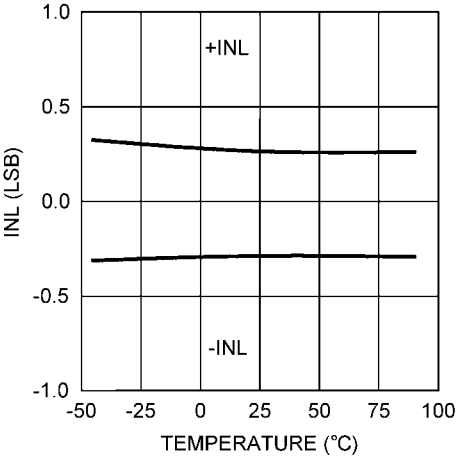
INL vs TEMPERATURE



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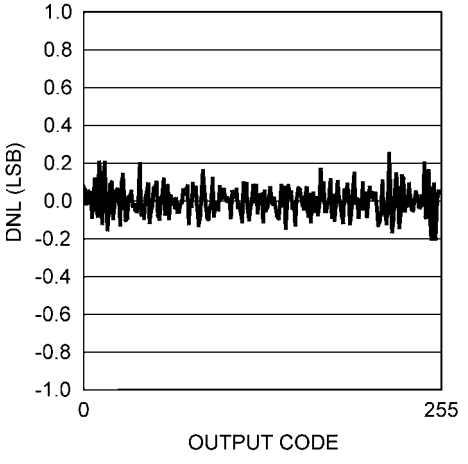
DNL vs. CODE



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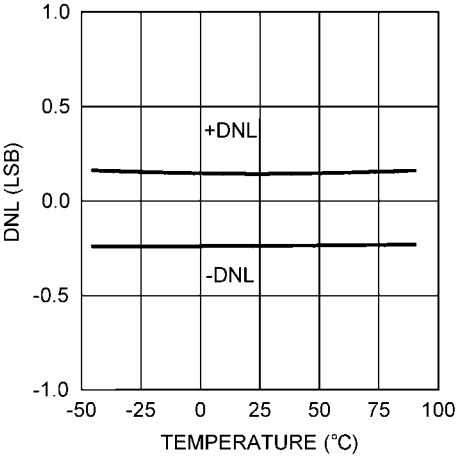
DNL vs. TEMPERATURE



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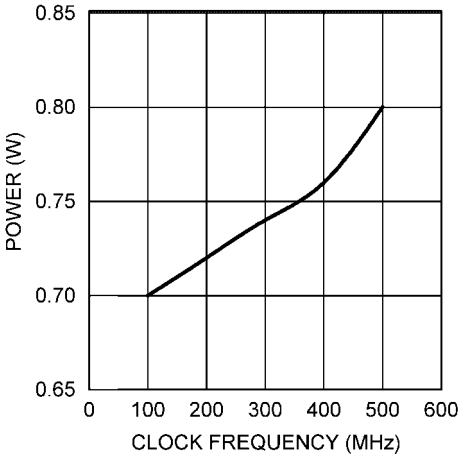
POWER CONSUMPTION vs. SAMPLE RATE



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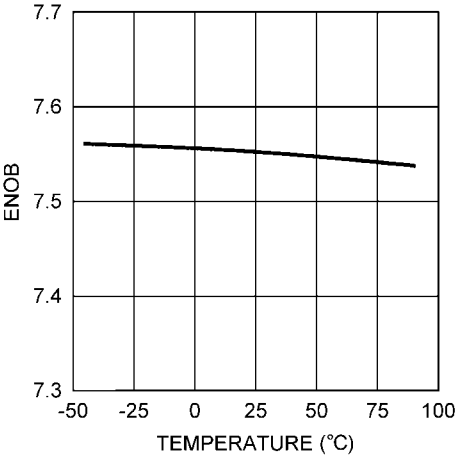
ENOB vs. TEMPERATURE



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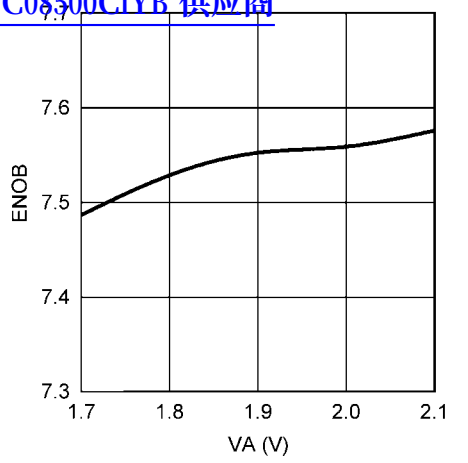
ENOB vs. SUPPLY VOLTAGE



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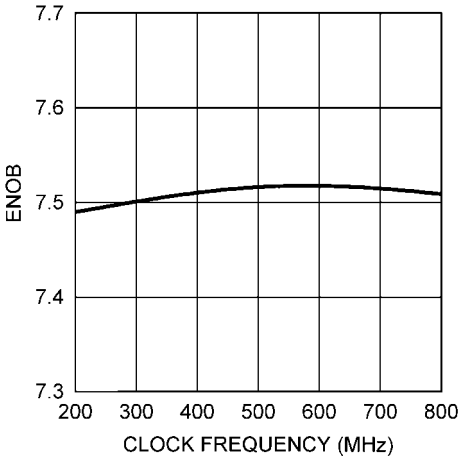
ENOB vs. SAMPLE RATE



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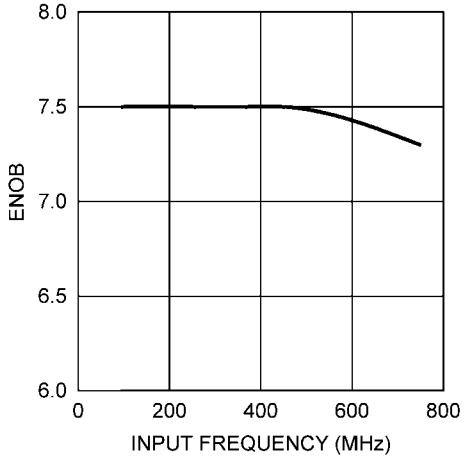
ENOB vs. INPUT FREQUENCY



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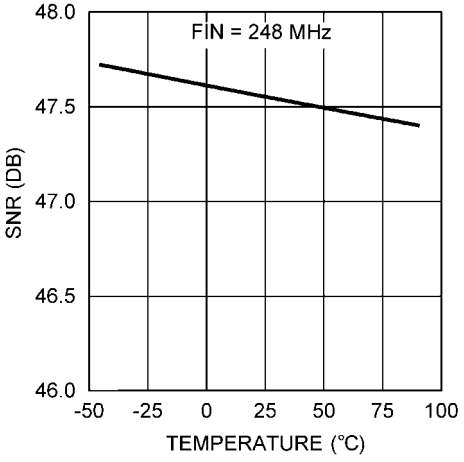
SNR vs. TEMPERATURE



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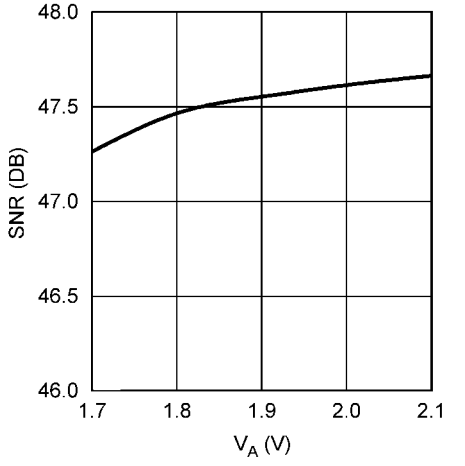
SNR vs. SUPPLY VOLTAGE



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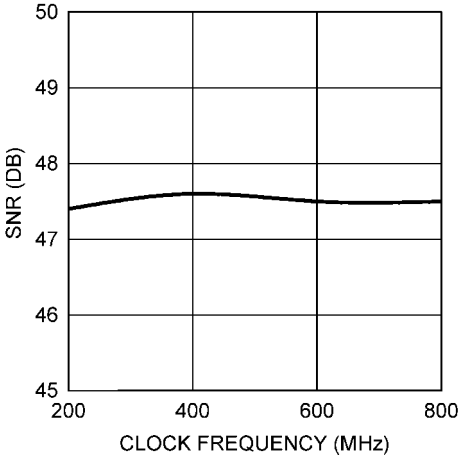
SNR vs. SAMPLE RATE



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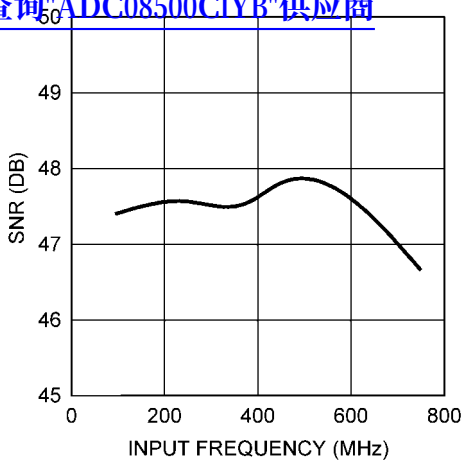
SNR vs. INPUT FREQUENCY



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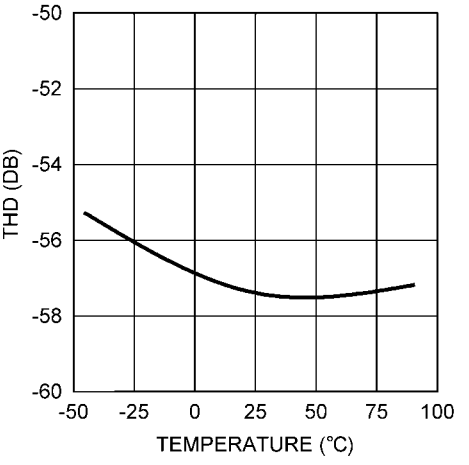
THD vs. TEMPERATURE



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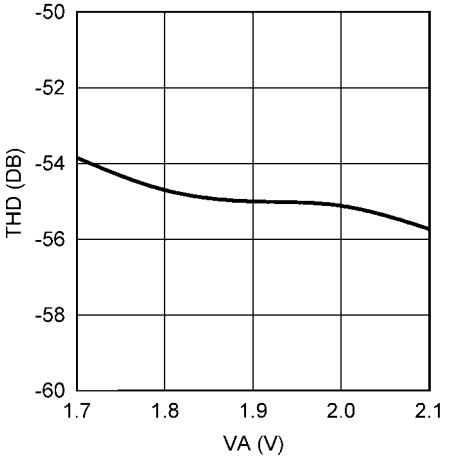
THD vs. SUPPLY VOLTAGE



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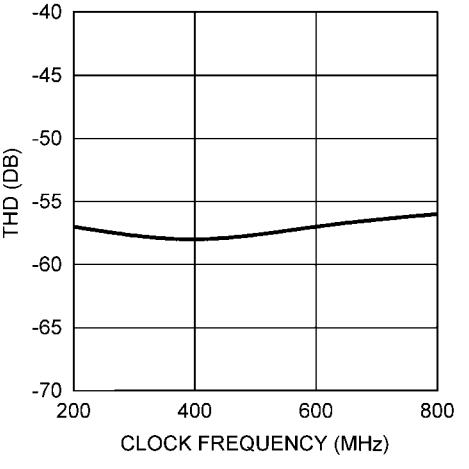
THD vs. SAMPLE RATE



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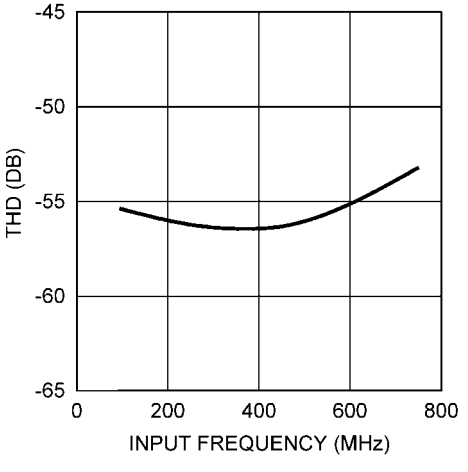
THD vs. INPUT FREQUENCY



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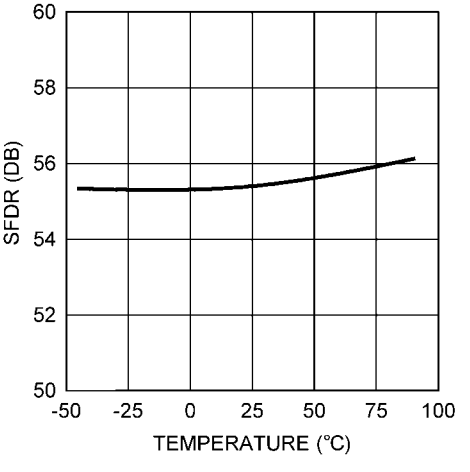
SFDR vs. TEMPERATURE



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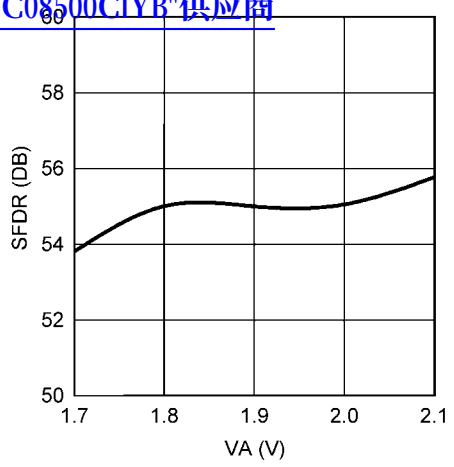
SFDR vs. SUPPLY VOLTAGE



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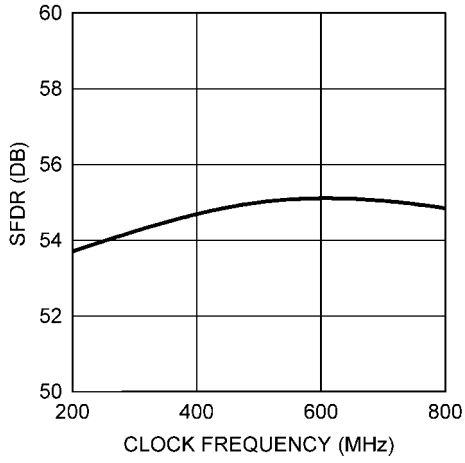
SFDR vs. SAMPLE RATE



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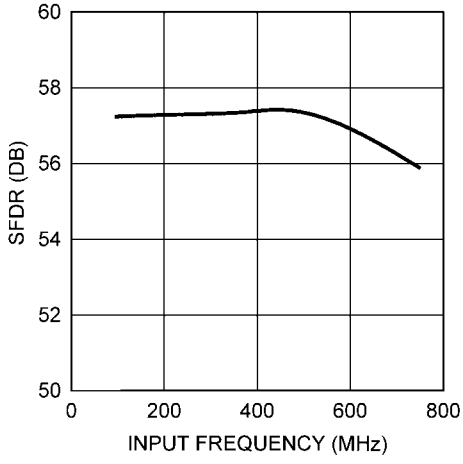
SFDR vs. INPUT FREQUENCY



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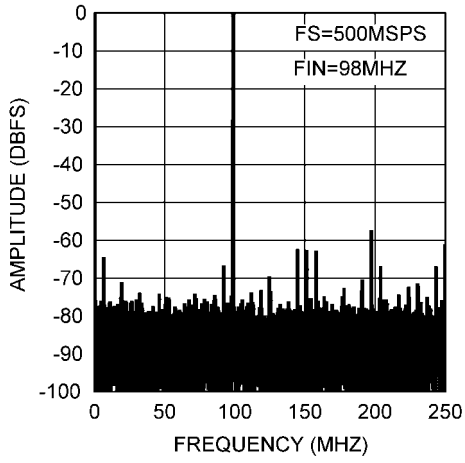
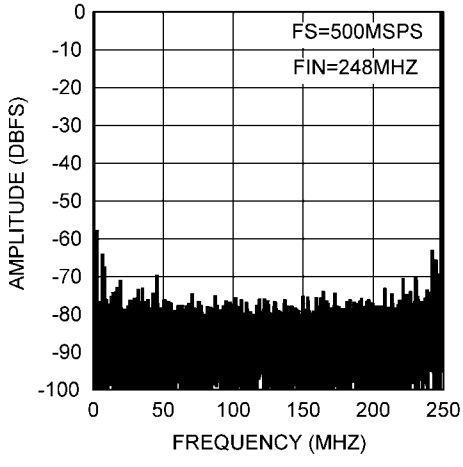
Spectral Response at f_{IN} = 98 MHz



20206487

Spectral Response at f_{IN} = 248 MHz



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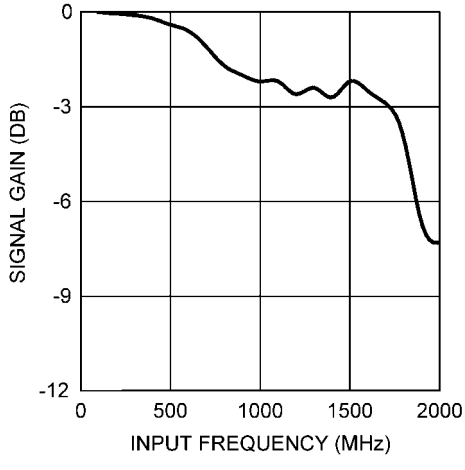
FULL POWER BANDWIDTH



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1.0 Functional Description

The ADC08500 is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

While it is generally poor practice to allow an active pin to float, pins 4 and 14 of the ADC08500 are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a pin to float, connecting that pin to a potential of one half the V_A supply voltage will have the same effect as allowing it to float.

1.1 OVERVIEW

The ADC08500 uses a calibrated folding and interpolating architecture that achieves 7.5 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 200 MSPS to 500 MSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from one or both of the channels is below negative full scale or above positive full scale.

The converter has a 1:2 demultiplexer that feeds two LVDS output buses. The data on these buses provide an output word rate on each bus at half the ADC sampling rate and must be interleaved by the user to provide output words at the full conversion rate.

The output levels may be selected to be normal or reduced. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

1.1.1 Self-Calibration

A self-calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the self calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, self calibration must be re-run whenever the sense of the FSR pin is changed. For best performance, we recommend that self calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, according to the particular system design requirements. See *2.4.2.2 On-Command Calibration* for more information. Calibration can not be initiated or run while the device is in the power-down mode. See *1.1.7 Power Down* for information on the interaction between Power Down and Calibration.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least t_{CAL_L} clock cycles, then hold it high for at least another t_{CAL_H} clock cycles as defined in the Converter Electrical Characteristics. The time taken by the calibration procedure is specified as t_{CAL} in Converter Electrical Characteristics. Holding the CAL pin high upon power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned t_{CAL_L} clock cycles followed by t_{CAL_H} clock cycles.

CalDly (pin 127) is used to select one of two delay times after the application of power before the start of calibration. This calibration delay time is depedent on the setting of the CalDly pin and is specified as t_{CalDly} in the Converter Electrical Characteristics. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Calibration Operation Notes:

- During the calibration cycle, the OR output may be active as a result of the calibration algorithm. All data on the output pins and the OR output are invalid during the calibration cycle.
- During the power-up calibration and during the on-command calibration, all clocks are halted on chip, including internal clocks and DCLK, while the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This is to reduce noise during the input resistor calibration portion of the calibration cycle.
  This external resistor is located between pin 32 and ground. R_{EXT} must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because R_{EXT} is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used.
- The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

1.1.2 Acquiring the Input

Data is acquired at the falling edge of CLK+ (pin 18) and the digital equivalent of that data is available at the digital outputs 13 clock cycles later for the D output bus and 14 clock cycles later for the Dd output bus. There is an additional internal delay called t_{OD} before the data is available at the outputs. See the Timing Diagram. The ADC08500 will convert as long as the clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with self calibration, enables a very flat SINAD/ENOB response beyond 500 MHz. The ADC08500 output data signaling is LVDS and the output format is offset binary.

1.1.3 Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the ADC08500 also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ

either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with register-based control and those pin-based controls are disabled. These pins are OutV (pin 3), OutEdge/DDR (pin 4), FSR (pin 14) and CalDly (pin 127). See *1.2 NORMAL/EXTENDED CONTROL* for details on the Extended Control mode.

1.1.4 The Analog Inputs

The ADC08500 must be driven with a differential input signal. Operation with a single-ended signal is not recommended. It is important that the inputs either be a.c. coupled to the inputs with the V_{CMO} pin grounded, or d.c. coupled with the V_{CMO} pin left floating. An input common mode voltage equal to the V_{CMO} output must be provided when d.c. coupling is used.

The input full-scale range is programmable in the normal mode by setting a level on pin 14 (FSR) as defined in by the specification V_{IN} in the Converter Electrical Characteristics. The full-scale range setting operates equally on both ADCs.

In the Extended Control mode, programming the Input Full-Scale Voltage Adjust register allows the input full-scale range to be adjusted as described in *1.4 REGISTER DESCRIPTION* and *2.2 THE ANALOG INPUT*.

1.1.5 Clocking

The ADC08500 must be driven with an a.c. coupled, differential clock signal. *2.3 THE CLOCK INPUTS* describes the use of the clock input pins. A differential LVDS output clock is available for use in latching the ADC output data into whatever receives that data.

The ADC08500 offers two options for output clocking. These options include a choice of which DCLK edge the output data transitions on and a choice of Single Data Rate (SDR) or Double Data Rate (DDR) outputs.

The ADC08500 also has the option to use a duty cycle corrected clock receiver as part of the input clock circuit. This feature is enabled by default and provides improved ADC clocking. This circuitry allows the ADC to be clocked with a signal source having a duty cycle ratio of 20 / 80 % (worst case).

1.1.5.1 OutEdge Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). This is chosen with the OutEdge input (pin 4). A high on the OutEdge input causes the output data to transition on the rising edge of DCLK, while grounding this input causes the output to transition on the falling edge of DCLK. See *2.4.3 Output Edge Synchronization*.

1.1.5.2 Double Data Rate

A choice of single data rate (SDR) or double data rate (DDR) output is offered. With single data rate the DCLK frequency is the same as the data rate of the two output buses. With double data rate the DCLK frequency is half the data rate and data is sent to the outputs on both DCLK edges. DDR clocking is enabled in non-Extended Control mode by allowing pin 4 to float.

1.1.6 The LVDS Outputs

The data outputs, the Out Of Range (OR) and DCLK, are LVDS. Output current sources provide 3 mA of output current to a differential 100 Ohm load when the OutV input (pin 14) is high or 2.2 mA when the OutV input is low. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC08500 is used is noisy, it may be necessary to tie the OutV pin high. The LVDS data output have a typical common mode voltage of 800 mV when the V_{BG} pin is unconnected and floating. This common mode voltage can be increased to 1.2V by tying the V_{BG} pin to V_A if a higher common mode is required.

IMPORTANT NOTE: Tying the V_{BG} pin to V_A will also increase the differential LVDS output voltage by up to 40 mV.

1.1.7 Power Down

The ADC08500 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, the output pins are put into a high impedance state and the device power consumption is reduced to a minimual level. Upon return to normal operation, the pipeline will contain meaningless information.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

1.2 NORMAL/EXTENDED CONTROL

The ADC08500 may be operated in one of two modes. In the simpler "normal" control mode, the user affects available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through a serial interface and a set of 3 registers. The two control modes are selected with pin 14 (FSR/ECE: Extended Control Enable). The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational.

Table 1 shows how several of the device features are affected by the control mode chosen.

TABLE 1. Features and Modes

Feature	Normal Control Mode	Extended Control Mode
SDR or DDR Clocking	DDR Clocking selected with pin 4 floating. SDR clocking selected when pin 4 not floating.	Selected with nDE in the Configuration Register (Addr-1h; bit-10). When the device is in DDR mode, address 1h, bit-8 must be set to 0b.
DDR Clock Phase	Not Selectable (0° Phase Only)	Selected with DCP in the Configuration Register (Addr- 1h; bit-11).
SDR Data transitions with rising or falling DCLK edge	SDR Data transitions with rising edge of DCLK+ when pin 4 is high and on falling edge when low.	Selected with OE in the Configuration Register (Addr- 1h; bit-8).
LVDS output level	Normal differential data and DCLK amplitude selected when pin 3 is high and reduced amplitude selected when low.	Selected with the OV in the Configuration Register (Addr- 1h; bit-9).
Power-On Calibration Delay	Short delay selected when pin 127 is low and longer delay selected when high.	Short delay only.
Full-Scale Range	Normal input full-scale range selected when pin 14 is high and reduced range when low. Selected range applies to both channels.	Up to 512 step adjustments over a nominal range specified in *1.4 REGISTER DESCRIPTION*. Selected using the Input Full-Scale Adjust register (Addr- 3h; bits-7 thru 15).
Input Offset Adjust	Not possible	512 steps of adjustment using the Input Offset register (Addr- 2h; bits-7 thru 15) as specified in *1.4 REGISTER DESCRIPTION*.

The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in *Table 2*.

TABLE 2. Extended Control Mode Operation (Pin 14 Floating)

Feature	Extended Control Mode Default State
SDR or DDR Clocking	DDR Clocking
DDR Clock Phase	Data changes with DCLK edge (0° phase)
LVDS Output Amplitude	Normal amplitude (710 mV_{P-P})
Calibration Delay	Short Delay
Full-Scale Range	700 mV nominal for both channels
Input Offset Adjust	No adjustment for either channel

1.3 THE SERIAL INTERFACE

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$). Three write only registers are accessible through this serial interface.

$\overline{SCS}$: This signal should be asserted low while accessing a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted at the rising edge of this signal.

SDATA: Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See *Figure 5*.

Each Register access consists of 32 bits, as shown in *Figure 5* of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. These 12 bits form the header. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in *Table 3*.

Refer to *1.4 REGISTER DESCRIPTION* for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

IMPORTANT NOTE: The Serial Interface should not be written to when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

TABLE 3. Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after H0, A0 loaded last					
A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Reserved
0	0	0	1	1h	Configuration
0	0	1	0	2h	Input Offset
0	0	1	1	3h	Input Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Reserved
1	0	1	0	Ah	Reserved
1	0	1	1	Bh	Reserved
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	Reserved
1	1	1	0	Eh	Reserved
1	1	1	1	Fh	Reserved

1.4 REGISTER DESCRIPTION

Three write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Configuration Register

Addr: 1h (0001b) **W only (0xB2FF)**

D15	D14	D13	D12	D11	D10	D9	D8
1	0	1	DCS	DCP	nDE	OV	OE

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 Must be set to 1b

Bit 14 Must be set to 0b

Bit 13 Must be set to 1b

Bit 12 DCS: Duty Cycle Stabilizer. When this bit is set to 1b, a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disbaled.

Bit 11 DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges ("0° Phase"). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells ("90° Phase"), using the one-half speed DCLK shown in *Figure 4* as the phase reference.

POR State: 0b

Bit 10 nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Dual Data Rate) mode whereby a data word is output with each rising and falling edge of DCLK. When this bit is set to a 1b, data bus clocking follows the SDR (single data rate) mode whereby each data word is output with either the rising or falling edge of DCLK , as determined by the OutEdge bit.

POR State: 0b

Bit 9 OV: Output Voltage. This bit determines the LVDS outputs' voltage amplitude and has the same function as the OutV pin that is used in the normal control mode. When this bit is set to 1b, the standard output amplitude of 710 mV_{P-P} is used. When this bit is set to 0b, the reduced output amplitude of 510 mV_{P-P} is used.

POR State: 1b

Bit 8 OE: Output Edge. This bit selects the DCLK edge with which the data words transition in the SDR mode and has the same effect as the OutEdge pin in the normal control mode. When this bit is 1b, the data outputs change with the rising edge of DCLK+. When this bit is 0b, the data output change with the falling edge of DCLK+.

POR State: 0b

Bits 7:0 Must be set to 1b.

Input Offset

Addr: 2h (0010b) **W only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)			Offset Value				(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8 Offset Value. The input offset of the I-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.

POR State: 0000 0000b

Bit 7 Sign bit. 0b gives positive offset, 1b gives negative offset resulting in total offset adjustment of ±45 mV.

POR State: 0b

Bit 6:0 Must be set to 1b

Input Full-Scale Voltage Adjust

Addr: 3h (0011b), W only (0x807F)

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7 Full Scale Voltage Adjust Value. The input full-scale voltage of the I-Channel ADC is adjusted linearly and monotonically from the nominal 700 mV_{P-P} differential by the value in this field.

0000 0000 0 560 mV_{P-P}

1000 0000 0 700 mV_{P-P}

1111 1111 1 840 mV_{P-P}

For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.

POR State: 1000 0000 0b (no adjustment)

Bits 6:0 Must be set to 1b

1.4.1 Note Regarding Extended Mode Offset Correction

When using the Input channel Offset Adjust register, the following information should be noted.

For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure below.

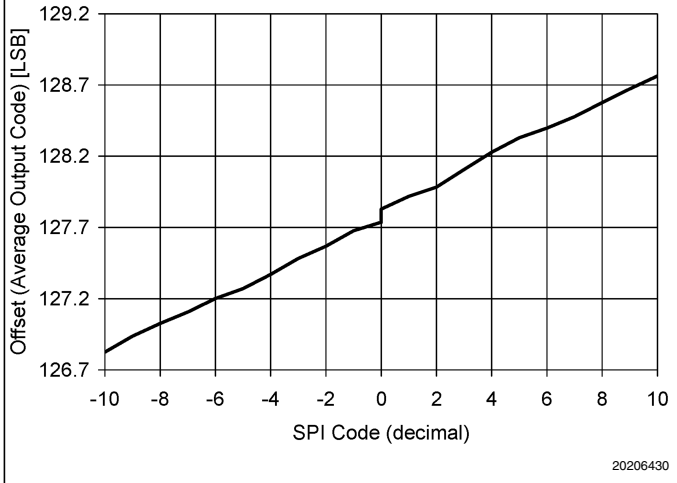


FIGURE 10. Extended Mode Offset Behavior

1.5 MULTIPLE ADC SYNCHRONIZATION

The ADC08500 has the capability to precisely reset its sampling clock input to DCLK output relationship as determined by the user-supplied DCLK_RST pulse. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that all the ADCs use for sampling.

The DCLK_RST signal must observe some timing requirements that are shown in *Figure 6*, *Figure 7*, and *Figure 8* of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{RH}, t_{RS}, and t_{RPW} in the Converter Electrical Characteristics.

The DCLK_RST signal can be asserted asynchronous to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state. The state in which DCLK is held during the reset period is determined by the mode of operation (SDR/DDR) and the setting of the Output Edge configuration pin or bit. (Refer to *Figure 6*, *Figure 7*, and *Figure 8* for the DCLK reset conditions). Therefore, depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted in synchronization with the CLK rising edge, the next CLK falling edge synchronizes the DCLK output with those of other ADC08500s in the system. The DCLK output is enabled again after a constant delay which is equal to the CLK input to DCLK output delay (t_{AD}). The device always exhibits this delay characteristic in normal operation.

The DCLK_RST pin should NOT be brought high while the calibration process is running (while CalRun is high). Doing so could cause a digital glitch in the digital circuitry, resulting in corruption and invalidation of the calibration.

2.0 Applications Information

2.1 THE REFERENCE VOLTAGE

The voltage reference for the ADC08500 is derived from a 1.254V bandgap reference which is made available at pin 31, V_{BG}, for user convenience. This output has an output current capability of ±100 µA and should be buffered if more current than this is required.

The internal bandgap-derived reference voltage has a nominal value of V_{IN}, as determined by the FSR pin and described in *1.1.4 The Analog Inputs*.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Configuration Register in the Extended Control mode, as explained in *1.2 NORMAL/EXTENDED CONTROL*.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See *2.2.2 Out Of Range (OR) Indication*.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is typically 800 mV when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage to a typical value of 1200 mV the V_{BG} pin can be connected directly to the supply rails.

2.2 THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. In the normal mode, the full-scale input range is selected using the FSR pin as specified in the Converter Electrical Characteristics. In the Extended Control mode, the full-scale input range is selected by programming the Full-Scale Voltage Adjust register through the Serial Interface. For best performance when adjusting the input full-scale range in the Extended Control, refer to *1.4 REGISTER DESCRIPTION* for guidelines on limiting the amount of adjustment.

Table 4 gives the input to output relationship with the FSR pin high when the normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in *Table 4* are reduced to 75% of the values indicated. In the Extended Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

TABLE 4. DIFFERENTIAL INPUT TO OUTPUT RELATIONSHIP (Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}−	Output Code
V_{CM} – 217.5 mV	V_{CM} + 217.5 mV	0000 0000
V_{CM} – 109 mV	V_{CM} + 109 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 109 mV	V_{CM} – 109 mV	1100 0000
V_{CM} + 217.5 mV	V_{CM} – 217.5 mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

Note that a precise d.c. common mode voltage must be present at the ADC inputs. This common mode voltage, V_{CMO}, is provided on-chip when a.c. input coupling is used and the input signal is a.c. coupled to the ADC.

When the inputs are a.c. coupled, the V_{CMO} output *must* be grounded, as shown in *Figure 11*. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50k-Ohm resistors.

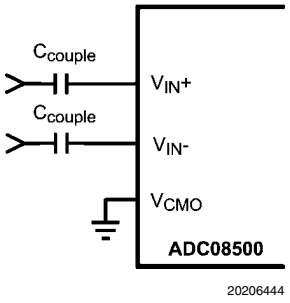


FIGURE 11. Differential Input Drive

When the d.c. coupled mode is used, a common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

2.2.1 Handling Single-Ended Input Signals

There is no provision for the ADC08500 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC.

2.2.1.1 a.c. Coupled Input

The easiest way to accomplish single-ended a.c. input to differential a.c. signal is by using an appropriate balun, as shown in *Figure 12*.

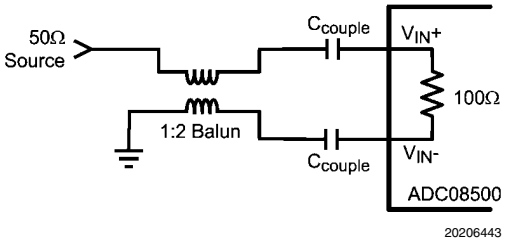


FIGURE 12. Single-Ended to Differential signal conversion using a balun

Figure 12 is a generic depiction of a single-ended to differential signal conversion using a balun. The circuitry specific to the balun will depend upon the type of balun selected and the overall board layout. It is recommended that the system designer contact the manufacturer of the balun they have se-

lected to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, it is important to understand the input architecture of the ADC. There are specific balun parameters of which the system designer should be mindful. A designer should match the impedance of their analog source to the ADC08500's on-chip 100Ω differential input termination resistor. The range of this input termination resistor is described in the electrical table as the specification R_{IN}.

Also, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance should be no more than ±2.5° and the amplitude imbalance should be limited to less than 1dB at the desired input frequency range. Finally, when selecting a balun, the VSWR (Voltage Standing Wave Ratio), bandwidth and insertion loss of the balun should also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss should be considered so that the signal at the balun output is within the specified input range of the ADC as described in the Converter Electrical Characteristics as the specification V_{IN}.

2.2.1.2 d.c. Coupled Input

When d.c. coupling to the ADC08500 analog inputs is required, single-ended to differential conversion may be easily accomplished with the LMH6555. An example of this type of circuit is shown in *Figure 13*. In such applications, the LMH6555 performs the task of single-ended to differential conversion while delivering low distortion and noise, as well as output balance, that supports the operation of the ADC08500. Connecting the ADC08500 V_{CMO} pin to the V_{CM_REF} pin of the LMH6555, through an appropriate buffer, will ensure that the common mode input voltage is as needed for optimum performance of the ADC08500. The LMV321 was chosen to buffer V_{CMO} for its low voltage operation and reasonable offset voltage.

Be sure that the current drawn from the V_{CMO} output does not exceed 100 µA.

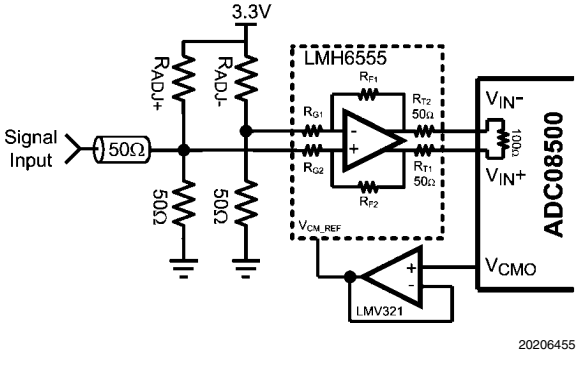


FIGURE 13. Example of Servicing the Analog Input with V_{CMO}

In *Figure 13*, R_{ADJ-} and R_{ADJ+} are used to adjust the differential offset that can be measured at the ADC inputs V_{IN+} / V_{IN-}. An unadjusted positive offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ-} position. Likewise, an unadjusted negative offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ+} position. *Table 5* gives suggested R_{ADJ-} and R_{ADJ+} values for various unadjusted differential offsets to bring the V_{IN+} / V_{IN-} offset back to within |15mV|.

TABLE 5. D.C. Coupled Offset Adjustment

Unadjusted Offset Reading	Resistor Value
0mV to 10mV	no resistor needed
11mV to 30mV	20.0kΩ
31mV to 50mV	10.0kΩ
51mV to 70mV	6.81kΩ
71mV to 90mV	4.75kΩ
91mV to 110mV	3.92kΩ

2.2.2 Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh.

2.2.3 Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC08500 is derived from an internal band-gap reference. The FSR pin controls the effective reference voltage of the ADC08500 such that the differential full-scale input range at the analog inputs is a normal amplitude with the FSR pin high, or a reduced amplitude with FSR pin low as defined by the specification V_{IN} in the Converter Electrical Characteristics. Best SNR is obtained with FSR high, but better distortion and SFDR are obtained with the FSR pin low.

2.3 THE CLOCK INPUTS

The ADC08500 has differential LVDS clock inputs, CLK+ and CLK-, which must be driven with an a.c. coupled, differential clock signal. Although the ADC08500 is tested and its performance is guaranteed with a differential 500 MHz clock, it typically will function well with clock frequencies indicated in the Converter Electrical Characteristics. The clock inputs are internally terminated and biased. The clock signal must be capacitively coupled to the clock pins as indicated in *Figure 14*.

Operation up to the sample rates indicated in the Converter Electrical Characteristics is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management . See *2.6.2 Thermal Management*.

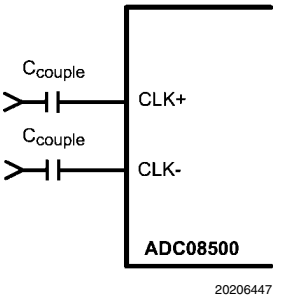


FIGURE 14. Differential (LVDS) Clock Connection

The differential Clock line pair should have a characteristic impedance of 100Ω and be terminated at the clock source in

that (100Ω) characteristic impedance. The clock line should be as short and as direct as possible. The ADC08500 clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient clock levels will result in poor dynamic performance. Excessively high clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the clock level within the range specified as V_{ID} in the Converter Electrical Characteristics.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The ADC08500 features a duty cycle clock correction circuit which can maintain performance over temperature. The ADC will meet its performance specification if the input clock high and low times are maintained within the duty cycle range as specified in the Converter Electrical Characteristics.

High speed, high performance ADCs such as the ADC08500 require a very stable clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)}/V_{INFSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

Note that the maximum jitter described above is the RSS sum of the jitter from all sources, including that in the ADC clock, that added by the system to the ADC clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Input clock amplitudes above those specified in the Converter Electrical Characteristics may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 127/128 when both input pins are at the same potential.

2.4 CONTROL PINS

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the ADC08500 and facilitate its use. These control pins provide Full-Scale Input Range setting, Self Calibration, Calibration Delay, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down feature.

2.4.1 Full-Scale Input Range Setting

The input full-scale range can be selected with the FSR control input (pin 14) in the normal mode of operation. The is specified as V_{IN} in the Converter Electrical Characteristics. In the extended control mode, the input full-scale range may be programmed using the Full-Scale Adjust Voltage register. See *2.2 THE ANALOG INPUT* for more information.

2.4.2 Self Calibration

The ADC08500 self-calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is a clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress.

2.4.2.1 Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, as described in the Calibration Delay Section, below.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The ADC08500 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See *2.4.2.2 On-Command Calibration*.

The internal power-on calibration circuitry comes up in an unknown logic state. If the clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 200 mW. The power consumption will be normal after the clock starts.

2.4.2.2 On-Command Calibration

To initiate an on-command calibration, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of t_{CAL_L} input clock cycles, then brought high for a minimum of another t_{CAL_H} input clock cycles. The calibration cycle will begin t_{CAL_H} input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum t_{CAL_H} and t_{CAL_L} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in *1.1.1 Self-Calibration* for best performance, a self calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly according to the particular system performance requirements. ENOB drops slightly as junction temperature increases and executing a new self calibration cycle will essentially eliminate the change.

During a Power-On calibration cycle, both the ADC and the input termination resistor are calibrated. As dyanamic performance changes slightly with junction temperature, an On-Command calibration can be executed to bring the performance of the ADC in line.

2.4.2.3 Calibration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration, as described in *1.1.1 Self-Calibration*. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

2.4.3 Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these clock signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that clock signal can be used to latch the output data into the receiving circuit.

When OutEdge (pin 4) is high, the output data is synchronized with (changes with) the rising edge of the DCLK+ (pin 82). When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the ADC08500 is capable, slight differences in the lengths of the clock and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK edge that best suits the application circuit and layout.

2.4.4 LVDS Output Level Control

The output level can be set to one of two levels with OutV (pin3). The strength of the output drivers is greater with OutV high. With OutV low there is less power consumption in the output drivers, but the lower output level means decreased noise immunity.

For short LVDS lines and low noise systems, satisfactory performance may be realized with the FSR input low. If the LVDS lines are long and/or the system in which the ADC08500 is used is noisy, it may be necessary to tie the FSR pin high.

2.4.5 Power Down Feature

The Power Down pin (PD) suspends device operation and puts the ADC08500 into a minimum power consumption state. See *1.1.7 Power Down* for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

2.5 THE DIGITAL OUTPUTS

The ADC08500 demultiplexes the output data of the ADC onto two LVDS output buses. The results of successive conversions started on the odd falling edges of the CLK+ pin are available on one of the two LVDS buses, while the results of conversions started on the even falling edges of the CLK+ pin are available on the other LVDS bus. This means that, the word rate at each LVDS bus is 1/2 the ADC08500 input clock rate and the two buses must be multiplexed to obtain the entire 0.5 GSPS conversion result.

Since the minimum recommended input clock rate for this device is 200 MSPS, the effective rate can be reduced to as low as 100 MSPS by using the results available on just one of the the two LVDS buses and a 200 MHz input clock, decimating the 200 MSPS data by two.

There is one LVDS output clock pair (DCLK+/-) available for use to latch the LVDS outputs on all buses. Whether the data is sent at the rising or falling edge of DCLK is determined by the sense of the OutEdge pin, as described in *2.4.3 Output Edge Synchronization*.

DDR (Double Data Rate) clocking can also be used. In this mode a word of data is presented with each edge of DCLK, reducing the DCLK frequency to 1/4 the input clock frequency. See the Timing Diagram section for details.

The OutV pin is used to set the LVDS differential output levels. See *2.4.4 LVDS Output Level Control*.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}– will produce an output code of all ones, a full-scale input level with V_{IN}– positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}– are equal, the output code will vary between codes 127 and 128.

2.6 POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC08500 should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a syatem where a lot of digital power is being consumed should not be used to supply power to the ADC08500. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

2.6.1 Supply Voltage

The ADC08500 is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08500 power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC08500. The circuit of *Figure 15* will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC08500, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output provides a minimum output current during power-up to ensure there is no turn-on spiking.

In the circuit of *Figure 15*, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended.

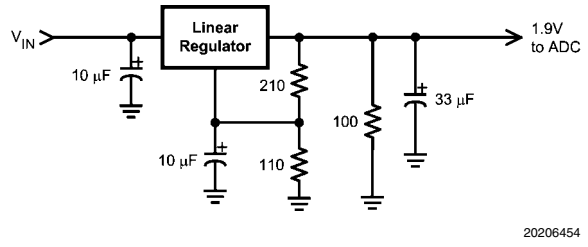


FIGURE 15. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage.

If the power is applied to the device without a clock signal present, the current drawn by the device might be below 200 mA. This is because the ADC08500 gets reset through clocked logic and its initial state is random. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the clock is established.

2.6.2 Thermal Management

The ADC08500 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 130°C. That is, T_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 130°C. This is not a problem if the ambient temperature is kept to a maximum of +85°C as specified in the Operating Ratings section.

Please note that the following are general recommendations for mounting exposed pad devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

The package of the ADC08500 has an exposed pad on its back that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional LQFP, but the exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The exposed pad of the device must be soldered down to ensure adequate heat conduction out of the package. The land pattern for this exposed pad should be at least as large as the 5 x 5 mm of the exposed pad of the package and be located such that the exposed pad of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground. A clearance of at least 0.5 mm should separate this land pattern from the mounting pads for the package pins.

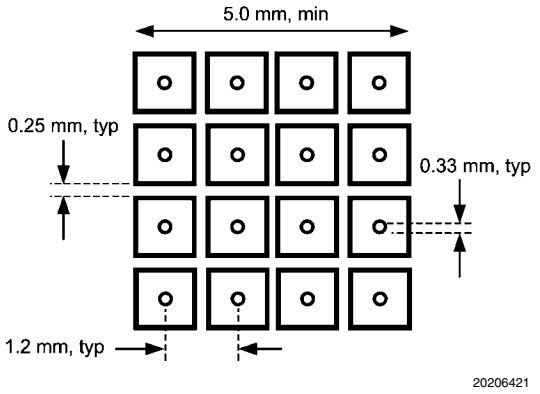


FIGURE 16. Recommended Package Land Pattern

Since a large aperture opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the land pattern of *Figure 16*.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2 square inches (6.5 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process as this wicking could cause voids in the solder between the package exposed pad and the thermal land on the PCB. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

If it is desired to monitor die temperature, a temperature sensor may be mounted on the heat sink area of the board near the thermal vias. .Allow for a thermal gradient between the temperature sensor and the ADC08500 die of $\theta_{J\text{-}PAD}$ times typical power consumption = 2.8 x 1.6 = 4.5°C. Allowing for a 5.5°C (including an extra 1°C) temperature drop from the die to the temperature sensor, then, would mean that maintaining a maximum pad temperature reading of 124.5°C will ensure that the die temperature does not exceed 130°C, assuming that the exposed pad of the ADC08500 is properly soldered down and the thermal vias are adequate. (The inaccuracy of the temperature sensor is addtional to the above calculation).

2.7 LAYOUT AND GROUNDING

Proper grounding and routing of all signals are essential to ensure accurate conversion. A single ground plane should be used instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to

isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input "ground" return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC08500. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

2.8 DYNAMIC PERFORMANCE

The ADC08500 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in Section 2.3.

It is good practice to keep the ADC clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than offered by the package pins.

2.9 USING THE SERIAL INTERFACE

The ADC08500 may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. *Table 6* and *Table 7* describe the functions of pins 3, 4, 14 and 127 in the non-extended control mode and the extended control mode, respectively.

2.9.1 Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. That is, the full-scale range, the power on calibration delay, the output voltage and the input coupling (a.c. or d.c.). The non-extended control mode is used by setting pin 14 high or low, as opposed to letting it float. *Table 6* indicates the pin functions of the ADC08500 in the non-extended control mode.

TABLE 6. Non-Extended Control Mode Operation (Pin 14 High or Low)

Pin	Low	High	Floating
3	Reduced V_{OD}	Normal V_{OD}	n/a
4	OutEdge = Neg	OutEdge = Pos	DDR
127	CalDly Short	CalDly Long	n/a
14	Reduced V_{IN}	Normal V_{IN}	Extended Control Mode

Pin 3 can be either high or low in the non-extended control mode. Pin 14 must not be left floating to select this mode. See *1.2 NORMAL/EXTENDED CONTROL* for more information.

Pin 4 can be high or low or can be left floating in the non-extended control mode. In the non-extended control mode, pin 4 high or low defines the edge at which the output data transitions. See *2.4.3 Output Edge Synchronization* for more information. If this pin is floating, the output clock (DCLK) is a DDR (Double Data Rate) clock (see *1.1.5.2 Double Data Rate*) and the output edge synchronization is irrelevant since data is clocked out on both DCLK edges.

Pin 127 in the non-extended control mode sets the calibration delay. Pin 127 is not designed to remain floating.

TABLE 7. Extended Control Mode Operation (Pin 14 Floating)

Pin	Function
3	SCLK (Serial Clock)
4	SDATA (Serial Data)
127	$\overline{SCS}$ (Serial Interface Chip Select)

2.10 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC08500. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in *1.1.4 The Analog Inputs* and *2.2 THE ANALOG INPUT*, the Input common mode voltage must remain within 50 mV of the V_{CMO} output , which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO} .

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC08500 as many high speed amplifiers will have higher distortion than will the ADC08500, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage. As mentioned in *2.1 THE REFERENCE VOLTAGE*, the reference voltage is intended to be fixed by FSR pin or Full-Scale Voltage Adjust register settings. Over driving this pin will not

change the full scale value, but can otherwise upset operation.

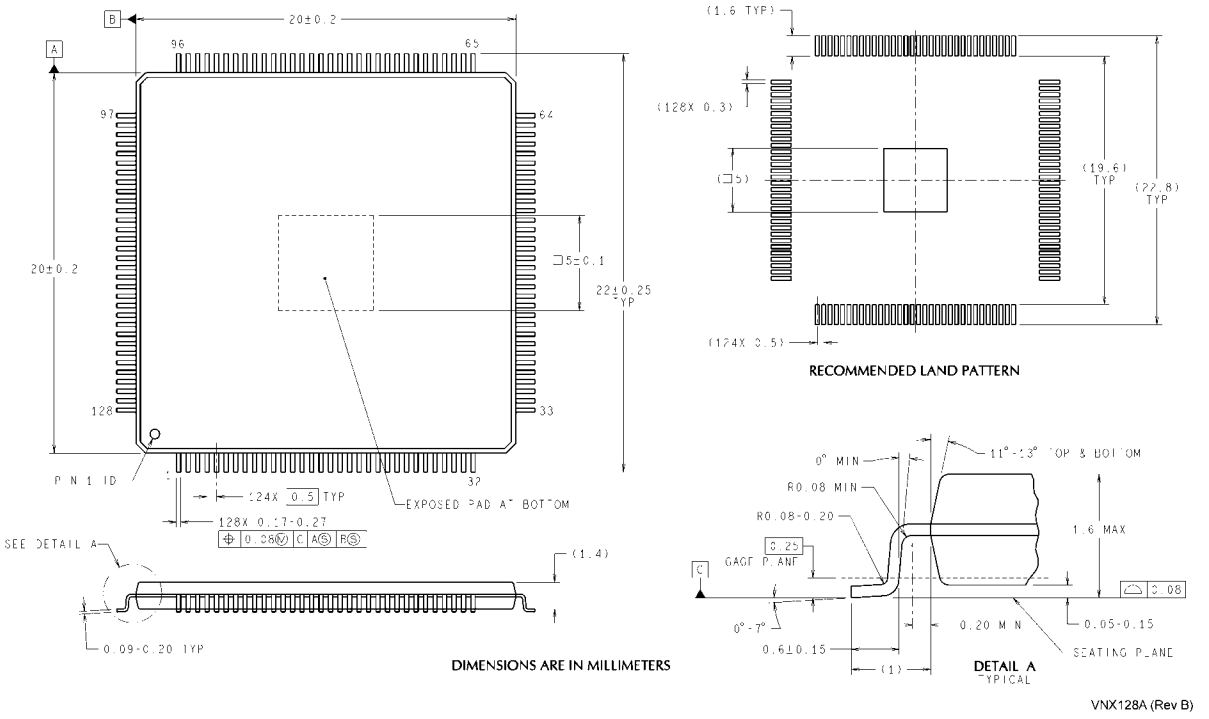
Driving the clock input with an excessively high level signal. The ADC clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate clock levels. As described in *2.3 THE CLOCK INPUTS*, insufficient clock levels can result in poor performance. Excessive clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in *2.6.2 Thermal Management*, it is important to provide adequate heat removal to ensure device reliability. This can be done either with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION MS-026, VARIATION BFB.

128-Lead Exposed Pad LQFP
Order Number ADC08500CIYB
NS Package Number VNX128A

Notes

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