

查询"5962-9756201Q2A"供应商

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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REV STATUS OF SHEETS	REV																		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13					

PMIC N/A	PREPARED BY Larry E. Shaw	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216		
STANDARD MICROCIRCUIT DRAWING	CHECKED BY Tuan D. Nguyen			
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	APPROVED BY Ray L. Monnin	MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, TTL, OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS W/3-STATE OUTPUTS, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 97-03-28			
	REVISION LEVEL			
		1 OF 13		

DSCC FORM 2233 APR 97 5962-E125-97
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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1.3 Absolute maximum ratings. 1/
[查询"5962-9756201Q2A"供应商](#)

Supply voltage range (V_{CC})	7.0 V dc
DC input voltage	7.0 V dc
Voltage applied to a disabled 3-state output	5.5 V dc
Storage temperature range	-65°C to +150°C
Operating free-air temperature range (T_A)	-55°C to 125°C
Maximum power dissipation (P_D)	704 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum low level input voltage (V_{IL})	+0.7 V
Maximum high level output current (I_{OH})	-12 mA
Maximum low level output current (I_{OL})	+32 mA
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, data before CLK \uparrow (t_s)	3 ns
Minimum hold time, data after CLK \uparrow (t_h)	3 ns
Minimum pulse duration, (t_w)	
CLK high	5.5 ns
CLK low	3 ns
Maximum clock frequency, (f_{clock})	100 MHz

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012).....XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 2/ Values will be added when they become available.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 3

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

- MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 4

查询"5962-9756201Q2A"供应商

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	VOH	V _{CC} = 4.5 V to 5.5 V 2/	I _{OH} = -2 mA	1, 2, 3	V _{CC} - 2		V
		V _{CC} = 4.5 V 2/	I _{OH} = -12 mA		2.4		
Low level output voltage	VOL	V _{CC} = 4.5 V 2/	I _{OL} = 32 mA	1, 2, 3		0.5	V
Input clamp voltage	V _{IK}	V _{CC} = 4.5 V	I _I = -18 mA	1, 2, 3		-1.2	V
High level input current	I _{IH}	V _{CC} = 5.5 V	V _I = 2.7 V	1, 2, 3		20	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V V _I = 0.4 V	Data	1, 2, 3		-3	mA
			All others 5/			-0.5	
Input current	I _I	V _{CC} = 5.5 V	V _I = 7 V	1, 2, 3		0.1	mA
Output current	I _O	V _{CC} = 5.5 V 3/	V _O = 2.25 V	1, 2, 3	-30	-112	mA
Supply current	I _{CCH}	V _{CC} = 5.5 V	Outputs high	1, 2, 3		120	mA
	I _{CCL}		Outputs low			128	
	I _{CCZ}		Outputs disabled			128	
Off-state output leakage current	I _{OZH}	V _{CC} = 5.5 V	V _O = 2.7 V	1, 2, 3		50	μA
	I _{OZL}	V _{CC} = 5.5 V	V _O = 0.4 V	1, 2, 3		-50	μA
Functional tests		See 4.4.1b, V _{CC} = 4.5 V, 5.5 V		7, 8			

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 5

DSCC FORM 2234
APR 97

9004708 0028964 994

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Clock frequency	f _{max}	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF,	9, 10, 11	100		MHz
Propagation delay time CLK to any Q	t _{PLH}	R ₁ = 500Ω R ₂ = 500Ω	9, 10, 11	3	11	ns
	t _{PHL}	^{4/}		4	11.5	
Output enable time, OE to any Q	t _{PZH}		9, 10, 11	2	7	ns
	t _{PZL}			3	11	
Output disable time, OE to any Q	t _{PHZ}		9, 10, 11	2	10	ns
	t _{PLZ}			2	7	

- ^{1/} Unused inputs that do not directly control the pin under test must be put at +2.5 V or -0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
- ^{2/} All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.
- ^{3/} The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and duration of the test condition shall not exceed one second.
- ^{4/} Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or -0.3 V.
- ^{5/} All others = OE, CLK.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-97562
		REVISION LEVEL	SHEET 6
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000			

Device type	01	
Case outlines	R and S	2
Terminal number	Terminal symbol	
1	\overline{OE}	\overline{OE}
2	1Q	1Q
3	1D	1D
4	2D	2D
5	2Q	2Q
6	3Q	3Q
7	3D	3D
8	4D	4D
9	4Q	4Q
10	GND	GND
11	CLK	CLK
12	5Q	5Q
13	5D	5D
14	6D	6D
15	6Q	6Q
16	7Q	7Q
17	7D	7D
18	8D	8D
19	8Q	8Q
20	VCC	VCC

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 7

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

FIGURE 2. Truth table.

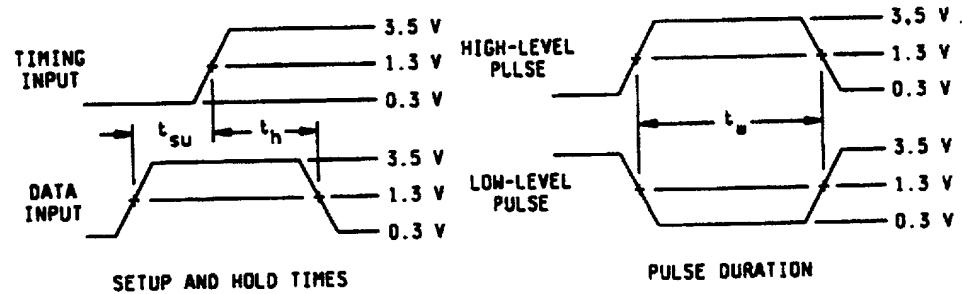
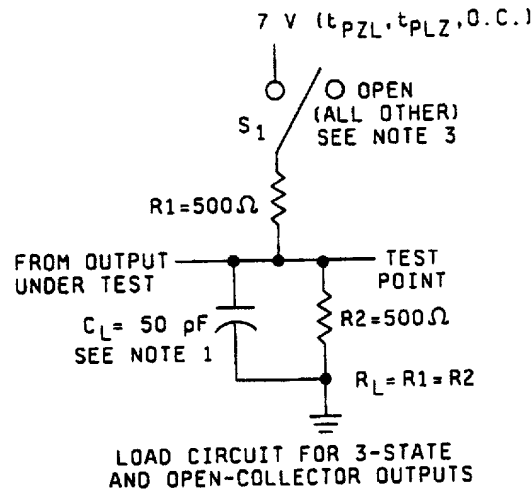
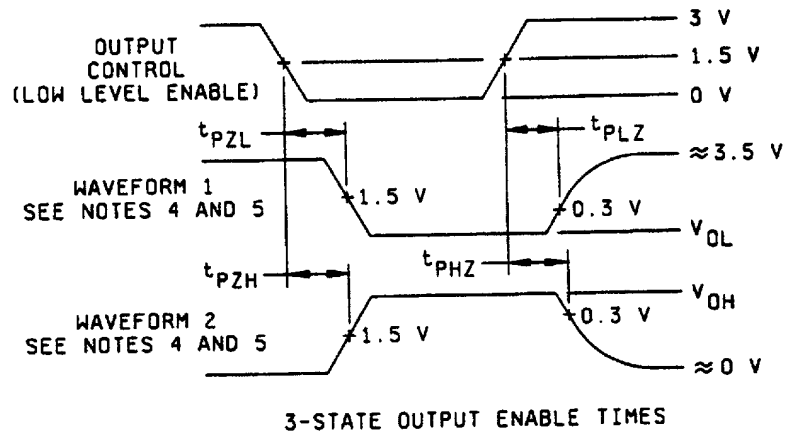
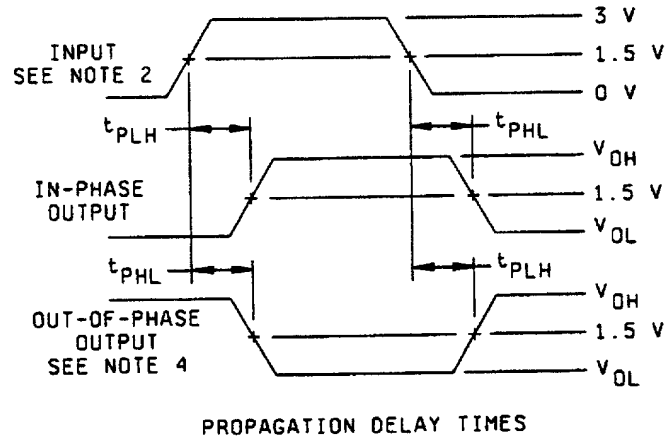


FIGURE 3. Test circuit and switching waveforms.

See notes at end of FIGURE 3.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-97562
	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	REVISION LEVEL	SHEET 8



- NOTES:
1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 1$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
 3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
 4. The outputs are measured one at a time with one transition per measurement.
 5. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 3. Test circuit and switching waveforms - Continued. 4/

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 9

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 10 (see MIL-PRF-38535, appendix A).

查询 5962-97562/QZA 供应商

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 10

4.4.1 Group A inspection.
[查询"5962-9756201Q2A"供应商](#)

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 11

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ C \pm 5^\circ C$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-97562
		REVISION LEVEL	SHEET 12

DSCC FORM 2234
APR 97

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6.6 Sources of supply.

[查询"5962-9756201Q2A"供应商](#)

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-97562
		REVISION LEVEL	SHEET 13
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000			

DSCC FORM 2234
APR 97

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Approved sources of supply for SMD 5962-97562 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9756201QSA	01295	SNJ54AS374W
5962-9756201QRA	01295	SNJ54AS374J
5962-9756201Q2A	01295	SNJ54AS374FK

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments Incorporated
 13500 N. Central Expressway
 P.O. Box 655303
 Dallas, TX 75265
 Point of contact: I-20 at FM 1788
 Midland, TX 79711-0448

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