19-0814; Rev 0; 5/07

EVALUATION KIT AVAILABLE

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

General Description

The MAX17009 is a 2-phase, step-down interleaved, fixed-frequency controller for AMD's® serial VID interface (SVI) CPU core supplies. Power-on detection of the CPU configures the MAX17009 as two independent single-phase regulators for a dual CPU core application, or one high-current, dual-phase, combined-output regulator for a unified core application. A reference buffer output (NBV_BUF) sets the voltage-regulation level for a North Bridge (NB) regulator, completing the total CPU cores and NB power requirements.

The MAX17009 is fully AMD SVI compliant. Output voltages are dynamically changed through a 2-wire serial interface, allowing the switching regulator and the reference buffer to be individually programmed to different voltages. A programmable slew-rate controller enables controlled transitions between VID codes, soft-start limits the inrush current, and soft-shutdown brings the output voltage back down to zero without any negative ring.

Transient phase repeat improves the response of the fixed-frequency architecture. Independently programmable AC and DC droop and selectable offset improve stability and reduce the total output-capacitance requirement. A thermistor-based temperature sensor allows for a programmable thermal-fault output ($\overline{VRHOT}$). The MAX17009 includes thermal-fault protection, undervoltage protection (UVP), and selectable output overvoltage protection (OVP). When any of these protection features detect a fault, the controller shuts down. True differential current sensing improves current limit, load-line accuracy, and current balance when operating in combined mode. The MAX17009 has an adjustable switching frequency, allowing 100kHz to 1.2MHz per-phase operation.

Applications

Mobile AMD SVI Core Supply

Multiphase CPU Core Supply

Voltage-Positioned, Step-Down Converters

Notebook/Desktop Computers

Pin Configuration appears at end of data sheet.

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Features

- **Dual-Output, Fixed-Frequency, Core Supply Controller**
- **Separate or Combinable Outputs Detected at Power-Up**
- **Reference Buffer Output for NB Controller**
- **±0.4% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **AMD SVI-Compliant Serial Interface**
- **7-Bit On-Board DAC: 0 to +1.550V Output Adjust Range**
- **Dynamic Phase Selection Optimizes Active/Sleep Efficiency**
- **Transient Phase Repeat Reduces Output Capacitance**
- **True Out-of-Phase Operation Reduces Input Capacitance**
- **Integrated Boost Switches**
- **Programmable AC and DC Droop**
- **Programmable 100kHz to 1.2MHz Switching Frequency**
- **Accurate Current Balance and Current Limit**
- **Adjustable Slew-Rate Control**
- **Power-Good (PWRGD) and Thermal-Fault ($\overline{VRHOT}$) Outputs**
- **System Power-OK (PGD_IN) Input**
- **Drives Large Synchronous-Rectifier MOSFETs**
- **4V to 26V Battery Input-Voltage Range**
- **Overvoltage, Undervoltage, and Thermal-Fault Protection**
- **Power Sequencing and Timing**
- **Soft-Startup and Soft-Shutdown**
- **< 1µA Typical Shutdown Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX17009GTL+	-40°C to +105°C	40 TQFN-EP*, 5mm x 5mm	T4055-1

+Denotes a lead-free package.

**EP = Exposed pad.*

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ABSOLUTE MAXIMUM RATINGS

V_{DD1}, V_{DD2}, V_{CC}, V_{DDIO} to GND_ ..... -0.3V to +6V
PWRGD to GND_ ..... -0.3V to +6V
FBDC_, FBAC_, $\overline{PRO}$ to GND_ ..... -0.3V to (V_{CC} + 0.3V)
GNDS2, THRM, $\overline{VRHOT}$ to GND_ ..... -0.3V to +6V
CSP_, CSN_, ILIM to GND_ ..... -0.3V to +6V
SVC, SVD, PGD_IN to GND_ ..... -0.3V to +6V
NBV_BUF, $\overline{NBSKP}$ to GND_ ..... -0.3V to (V_{CC} + 0.3V)
REF, OSC, TIME, OPTION to GND_ ..... -0.3V to (V_{CC} + 0.3V)
BST1, BST2 to GND_ ..... -0.3V to +36V
BST1 to V_{DD1} ..... -0.3V to +30V
BST2 to V_{DD2} ..... -0.3V to +30V
LX1 to BST1 ..... -6V to +0.3V
LX2 to BST2 ..... -6V to +0.3V
DH1 to LX1 ..... -0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 ..... -0.3V to (V_{BST2} + 0.3V)
DL1 to GND_ ..... -0.3V to (V_{DD1} + 0.3V)
DL2 to GND_ ..... -0.3V to (V_{DD2} + 0.3V)
GNDS1, GNDS_NB to GND_ ..... -0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
Multilayer PCB (derate 35.7mW/°C above +70°C) 2857mW
Single-Layer PCB (derate 22.2mW/°C above +70°C) .. 1778mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET	4		26	V
	V_{BIAS}	V_{CC}, V_{DD1}, V_{DD2}	4.5		5.5	
	V_{DDIO}		1.0		2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising 50mV typical hysteresis	4.10	4.25	4.45	V
V_{CC} Power-On Reset Threshold	V_{CC}	Falling edge, typical hysteresis = 1.1V, faults cleared and DL_ forced high when V_{CC} falls below this level		1.8		V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising 100mV typical hysteresis	0.7	0.8	0.9	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ forced above their regulation points		5	10	mA
Quiescent Supply Currents (V_{DD1}, V_{DD2})	I_{DD1}, I_{DD2}	Skip mode, FBDC_ forced above their regulation points		0.01	1	µA
Quiescent Supply Current (V_{DDIO})	I_{DDIO}			10	25	µA
Shutdown Supply Current (V_{CC})		$\overline{SHDN}$ = GND		0.01	1	µA
Shutdown Supply Currents (V_{DD1}, V_{DD2})		$\overline{SHDN}$ = GND		0.01	1	µA
Shutdown Supply Current (V_{DDIO})		$\overline{SHDN}$ = GND		0.01	1	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, no REF load	1.986	2.000	2.014	V
Reference Load Regulation		Sourcing: I_{REF} = 0 to 500µA	-2	-0.2		mV
		Sinking: I_{REF} = 0 to -100µA		0.21	6.2	
REF Fault Lockout Voltage		Typical hysteresis = 85mV		1.84		V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS CONTROLLERS						
DC Output-Voltage Accuracy (Note 1)	V_{OUT}	DAC codes from 0.8375V to 1.5500V	-0.4		+0.4	%
		DAC codes from 0.5000V to 0.8250V	-4		+4	mV
		DAC codes below 0.4875V	-10		+10	
DC Load Regulation		Either SMPS, PWM mode, droop disabled, zero to full load		-0.1		%
Line-Regulation Error		Either SMPS, 4V < V_{IN} < 26V		0.03		%/V
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode	-200		+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV; combined: $\Delta V_{OUT}/\Delta V_{GNDS1}$, -200mV ≤ V_{GNDS1} ≤ +200mV	0.95	1.00	1.05	V/V
GNDS_ Input Bias Current	$I_{GNDS\_}$		-2		+2	µA
Combined-Mode Detection Threshold		GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$	0.7	0.8	0.9	V
FBDC_ Input Bias Current	$I_{FBDC0\_}$	CSP_ = CSN_	-3		+3	µA
Switching-Frequency Accuracy	f_{OSC}	R_{OSC} = 143kΩ (f_{OSC} = 300kHz nominal)	-5		+5	%
		R_{OSC} = 35.7kΩ (f_{OSC} = 1.2MHz nominal) to 432kΩ (f_{OSC} = 99kHz nominal)	-7.5		+7.5	
Maximum Duty Factor	D_{MAX}		90	92		%
Minimum On-Time	t_{ONMIN}				175	ns
SMPS1-to-SMPS2 Phase Shift		SMPS2 starts after SMPS1		50		%
				180		Degrees
TIME Slew-Rate Accuracy		During transition: R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10		+10	%
		During transition: R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15		+15	
		Startup and shutdown		1		mV/µS
CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.05 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V	-3		+3	mV
Zero-Crossing Threshold	V_{ZX}	$V_{GND\_}$ - $V_{LX\_}$, SKIP mode		3		mV
Idle Mode™ Threshold Tolerance	V_{IDLE}	$V_{CSP\_}$ - $V_{CSN\_}$, SKIP mode, 0.15 x V_{LIMIT}	-1.5		+1.5	mV
CS_ Input-Leakage Current		CSP_ and CSN_	-0.2		+0.2	µA
CS_ Common-Mode Input Range		CSP_ and CSN_	0		2	V
Phase-Disable Threshold		CSP2	3	V_{CC} - 1	V_{CC} -0.4	V

Idle Mode is a trademark of Maxim Integrated Products, Inc.

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DROOP AND CURRENT BALANCE							
DC Droop Amplifier Transconductance	$G_{m(FBDC\_)}$	$\Delta I_{FBDC\_}/(\Delta V_{CS\_})$, $V_{FBDC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.00	1.03	mS
DC Droop and Current-Balance Amplifier Offset		$I_{FBDC\_}/G_{m(FBDC\_)}$		-1.5		+1.5	mV
AC Droop and Current-Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.00	1.03	mS
AC Droop and Current-Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$		-1.5		+1.5	mV
No-Load Positive Offset with Offset Enabled		Offset enabled, OPTION = REF or GND			12.5		mV
Transient Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 5mV hysteresis (typ), transient phase-repeat enabled, OPTION = OPEN or GND		-32		-18	mV
NB BUFFER							
NBV_BUF Output Voltage Accuracy	V_{NBV_BUF}	DAC codes from 0.8375V to 1.5500V		-0.4		+0.4	%
		DAC codes from 0.5000V to 0.8250V		-4		+4	mV
		DAC codes below 0.4875V to 0.0125V		-10		+10	
NBV_BUF Short-Circuit Current (Sets Slew Rate Together with External Capacitor C_{NBV_BUF})		DAC code set to 1.2V, V_{NBV_BUF} = 0.4V and 2V	R_{TIME} = 143kΩ, I_{NBV_BUF} = 7.0µA	-10		+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, I_{NBV_BUF} = 28µA to 2.8µA	-15		+15	
GNDS_NB Input Range	V_{GNDS_NB}			-200		+200	mV
GNDS_NB Gain	A_{GNDS_NB}	$\Delta V_{NBV\_BUF}/\Delta V_{GNDS\_NB}$, -200mV ≤ V_{GNDS_NB} ≤ +200mV		0.95	1.00	1.05	V/V
GNDS_NB Input Bias Current	I_{GNDS_NB}			-2		+2	µA
FAULT DETECTION							
Output Overvoltage Trip Threshold	$V_{OVP\_}$	Measured at FBDC_, rising edge	Normal operation	250	300	350	mV
			Output not in regulation after a downward VID transition	1.80	1.85	1.90	V
			Minimum OVP threshold		0.8		
Output Overvoltage Fault-Propagation Delay	t_{OVP}	FBDC_ forced 25mV above trip threshold			10		µs
Output Undervoltage-Protection Trip Threshold	V_{UVP}	Measured at FBDC_ with respect to unloaded output voltage		-450	-400	-350	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Undervoltage Fault-Propagation Delay	t_{UVP}	FBDC_ forced 25mV below trip threshold			10		µs
PWRGD Threshold		Measured at FBDC_ with respect to unloaded output voltage	Lower threshold, falling edge (undervoltage)	-350	-300	-250	V
		15mV hysteresis (typ)	Upper threshold, rising edge (overvoltage)	+150	+200	+250	
PWRGD Propagation Delay	$t_{PWRGD\_}$	FBDC_ forced 25mV outside the PWRGD trip thresholds			10		µs
PWRGD Output Low Voltage		I_{SINK} = 4mA				0.4	V
PWRGD Leakage Current	$I_{PWRGD\_}$	High state, PWRGD forced to 5.5V				1	µA
PWRGD Startup Delay and Transition Blanking Time	t_{BLANK}	Measured from the time when FBDC_ reaches the target voltage based on the slew rate set by R_{TIME}			20		µs
$\overline{VRHOT}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5	30	30.5	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold, falling edge			10		µs
$\overline{VRHOT}$ Output Low Voltage		I_{SINK} = 4mA				0.4	V
$\overline{VRHOT}$ Leakage Current		High state, $\overline{VRHOT}$ forced to 5V				1	µA
THRM Input Leakage				-100		+100	nA
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			160		°C
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.0	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state			0.7	2.0	Ω
		DL_, low state			0.25	0.6	
DH_ Gate-Driver Source/Sink Current	$I_{DH\_}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DL_ Gate-Driver Source Current	$I_{DL\_}$ (SOURCE)	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL\_}$ (SINK)	DL_ forced to 2.5V			8		A
Dead Time	t_{DH_DL}	DH_ low to DL_ high		15	25	40	ns
	t_{DL_DH}	DL_ low to DH_ high		9	20	35	
Internal Boost Diode Switch R_{ON}		BST1 to V_{DD1}, BST2 to V_{DD2}; measure with 10mA of current			10	20	Ω

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
2-WIRE SVI BUS LOGIC INTERFACE							
SVI Logic Input Current		SVC, SVD		-1		+1	µA
SVI Logic Input Threshold		SVC, SVD, rising edge, hysteresis = 0.15V_{DDIO}		0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}					3.4	MHz
START Condition Hold Time	$t_{HD,STA}$			160			ns
Repeated START Condition Setup Time	$t_{SU,STA}$			160			ns
STOP Condition Setup Time	$t_{SU,STO}$			160			ns
Data Hold	$t_{HD,DAT}$	A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of SCK signal) to bridge the undefined region of SCL's falling edge				70	ns
Data Setup Time	$t_{SU,DAT}$			10			ns
SVC Low Period	t_{LOW}			160			ns
SVC High Period	t_{HIGH}			60			ns
SVC/SVD Rise and Fall Time	t_R, t_F	Measured from 10% to 90% of V_{DDIO}				40	ns
Pulse Width of Spike Suppression		Input filters on SVD and SVC suppress noise spikes less than 50ns			20		ns
INPUTS AND OUTPUTS							
Logic Input Current		$\overline{SHDN}$, PGD_IN		-1		+1	µA
		$\overline{PRO}$, OPTION		-3		+3	
Logic Input Threshold		$\overline{SHDN}$, rising edge, hysteresis = 225mV		0.8		2.0	V
Four-Level Input-Logic Levels		OPTION	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.4	
Tri-Level Input-Logic Levels		$\overline{PRO}$	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			Low			0.4	
PGD_IN Logic Input Threshold		PGD_IN		0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
$\overline{NBSKP}$ Logic Output Voltage		Low state, I_{SINK} = 3mA				0.4	V
		High state, I_{SOURCE} = 3mA		V_{CC} - 0.4			

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
INPUT SUPPLIES					
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET	4	26	V
	V_{BIAS}	V_{CC}, V_{DD1}, V_{DD2}	4.5	5.5	
	V_{DDIO}		1.0	2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising 50mV typical hysteresis	4.10	4.45	V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising 100mV typical hysteresis	0.8	0.9	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ forced above their regulation points		10	mA
Quiescent Supply Currents (V_{DD1}, V_{DD2})	I_{DD1}, I_{DD2}	Skip mode, FBDC_ forced above their regulation points, T_A = -40°C to +85°C		1	µA
Quiescent Supply Current (V_{DDIO})	I_{DDIO}			25	µA
Shutdown Supply Current (V_{CC})		$\overline{SHDN}$ = GND, T_A = -40°C to +85°C		1	µA
Shutdown Supply Currents (V_{DD1}, V_{DD2})		$\overline{SHDN}$ = GND, T_A = -40°C to +85°C		1	µA
Shutdown Supply Current (V_{DDIO})		T_A = -40°C to +85°C		1	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, no REF load	1.98	2.02	V
Reference Load Regulation		Sourcing: I_{REF} = 0 to 500µA	-2		mV
		Sinking: I_{REF} = 0 to -100µA		6.2	
MAIN SMPS CONTROLLERS					
DC Output-Voltage Accuracy (Note 1)	V_{OUT}	DAC codes from 0.8375V to 1.5500V	-0.6	+0.6	%
		DAC codes from 0.5000V to 0.8250V	-6	+6	mV
		DAC codes from 0.4875V to 0.0125V	-15	+15	
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode	-200	+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV, Combined: $\Delta V_{OUT}/\Delta V_{GNDS1}$, -200mV ≤ V_{GNDS1} ≤ +200mV	0.95	1.05	V/V
Combined-Mode Detection Threshold		GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$	0.7	0.9	V
Switching-Frequency Accuracy	f_{OSC}	R_{OSC} = 143kΩ (f_{OSC} = 300kHz nominal)	-7.5	+7.5	%
		R_{OSC} = 35.7kΩ (f_{OSC} = 1.2MHz nominal) to 432kΩ (f_{OSC} = 99kHz nominal)	-10	+10	
Maximum Duty Factor	DMAX		90		%
Minimum On-Time	t_{ONMIN}			185	ns
TIME Slew-Rate Accuracy		During transition: R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10	+10	%
		During transition: R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15	+15	

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.05 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V		-3	+3	mV
Idle Mode Threshold Tolerance	V_{IDLE}	$V_{CSP\_}$ - $V_{CSN\_}$, SKIP mode, 0.15 x V_{LIMIT}		-1.5	+1.5	mV
CS_ Common-Mode Input Range		CSP_ and CSN_		0	2	V
Phase Disable Threshold		CSP2		3	V_{CC} - 0.4	V
DROOP AND CURRENT BALANCE						
DC Droop Amplifier Transconductance	$G_{m(FBDC\_)}$	$\Delta I_{FBDC\_}/(\Delta V_{CS\_})$, $V_{FBDC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.03	mS
DC Droop Amplifier Offset		$I_{FBDC\_}/G_{m(FBDC\_)}$		-1.5	+1.5	mV
AC Droop and Current-Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.03	mS
AC Droop and Current-Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$		-1.5	+1.5	mV
Transient-Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 5mV hysteresis (typ), transient phase repeat enabled, OPTION = OPEN or GND		-32	-18	mV
NB BUFFER						
NBV_BUF Output-Voltage Accuracy	V_{NBV_BUF}	DAC codes from 0.8375V to 1.5500V		-0.6	+0.6	%
		DAC codes from 0.5000V to 0.8250V		-6	+6	mV
		DAC codes from 0.4875V to 0.0125V		-15	+15	
NBV_BUF Short-Circuit Current (Sets Slew Rate Together with External Capacitor C_{NBV_BUF})		DAC code set to 1.2V, V_{NBV_BUF} = 0.4V and 2V	R_{TIME} = 143kΩ, I_{NBV_BUF} = 7.0µA	-10	+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, I_{NBV_BUF} = 28µA to 2.8µA	-15	+15	
GNDS_NB Input Range	V_{GNDS_NB}			-200	+200	mV
GNDS_NB Gain	A_{GNDS_NB}	$\Delta V_{NBV\_BUF}/\Delta V_{GNDS\_NB}$, -200mV ≤ V_{GNDS_NB} ≤ +200mV		0.95	1.05	V/V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
FAULT DETECTION						
Output Overvoltage Trip Threshold	$V_{OVP\_}$	Measured at FBDC_, rising edge	Normal operation	250	350	mV
Output Undervoltage-Protection Trip Threshold	V_{UVP}	Measured at FBDC_ with respect to unloaded output voltage		-450	-350	mV
PWRGD Threshold		Measured at FBDC_ with respect to unloaded output voltage	Lower threshold, falling edge (undervoltage)	-350	-250	V
		15mV hysteresis (typ)	Upper threshold, rising edge (overvoltage)	+150	+250	
PWRGD Output Low Voltage		I_{SINK} = 4mA			0.4	V
$\overline{VRHOT}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5	30.5	%
$\overline{VRHOT}$ Output Low Voltage		I_{SINK} = 4mA			0.4	V
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)		2.0	Ω
			Low state (pulldown)		2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state			2.0	Ω
		DL_, low state			0.6	
Dead Time	t_{DH_DL}	DH_ low to DL_ high		15	40	ns
	t_{DL_DH}	DL_ low to DH_ high		9	40	
Internal Boost Diode Switch R_{ON}		BST1 to V_{DD1}, BST2 to V_{DD2}, measured with 10mA of current			20	Ω
2-WIRE SVI BUS LOGIC INTERFACE						
SVI Logic Input Threshold		SVC, SVD, rising edge, hysteresis = 0.15 x V_{DDIO}		0.3 x V_{DDIO}	0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}				3.4	MHz
START Condition Hold Time	$t_{HD,STA}$			160		ns
Repeated START Condition Setup Time	$t_{SU,STA}$			160		ns
STOP Condition Setup Time	$t_{SU,STO}$			160		ns
Data Hold	$t_{HD,DAT}$	A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of SCK signal) to bridge the undefined region of SCL's falling edge			70	ns
Data Setup Time	$t_{SU,DAT}$			10		ns
SVC Low Period	t_{LOW}			160		ns
SVC High Period	t_{HIGH}			60		ns
SVC/SVD Rise and Fall Time	t_R, t_F	Measured from 10% to 90% of V_{DDIO}			40	ns

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUTS AND OUTPUTS						
Logic Input Threshold		$\overline{SHDN}$, rising edge, hysteresis = 225mV		0.8	2.0	V
Four-Level Input Logic Levels		OPTION	High	V_{CC} - 0.4		V
			Open	3.15	3.85	V
			REF	1.65	2.35	
			Low		0.4	
Tri-Level Input Logic Levels		$\overline{PRO}$	High	V_{CC} - 0.4		V
			Open	3.15	3.85	
			Low		0.4	
PGD_IN Logic Input Threshold		PGD_IN		0.3 x V_{DDIO}	0.7 x V_{DDIO}	V

Note 1: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage will have a DC regulation level higher than the error comparator threshold by 50% of the ripple.

Note 2: Specifications to T_A = -40°C to +105°C are guaranteed by design, not production tested.

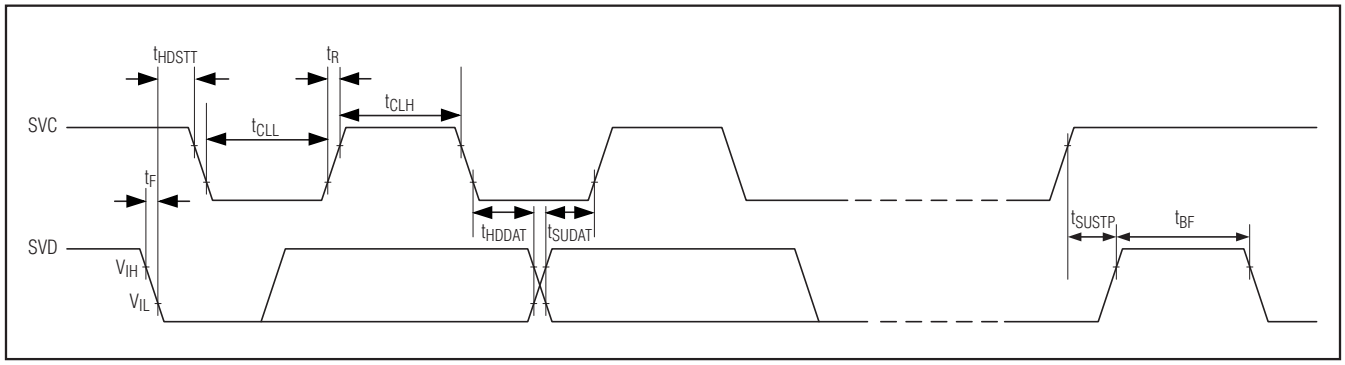
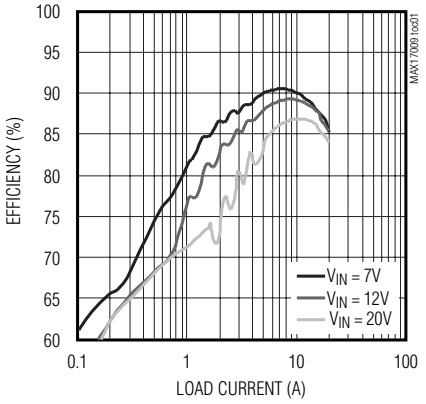


Figure 1. Timing Definitions Used in the Electrical Characteristics

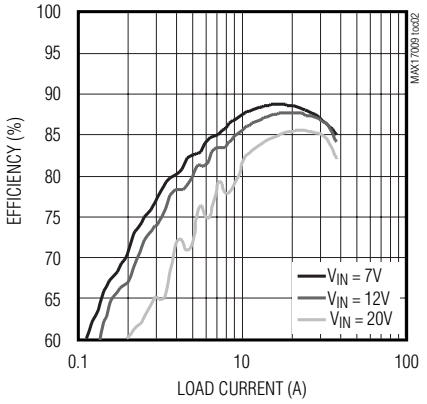
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

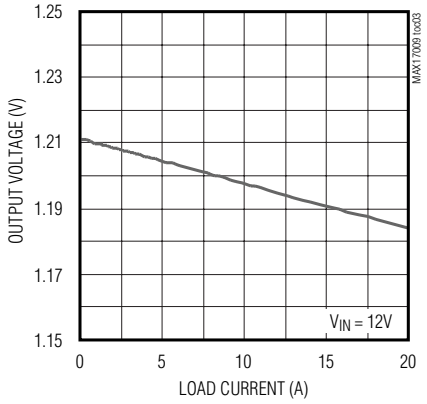
1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2125V)



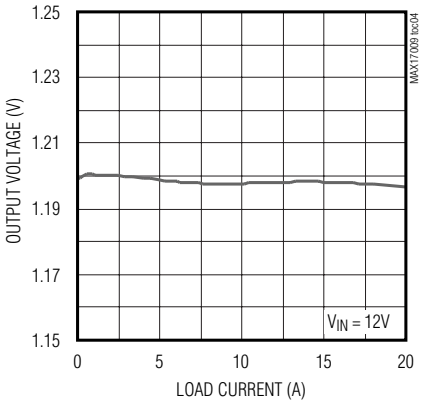
2-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2125V)



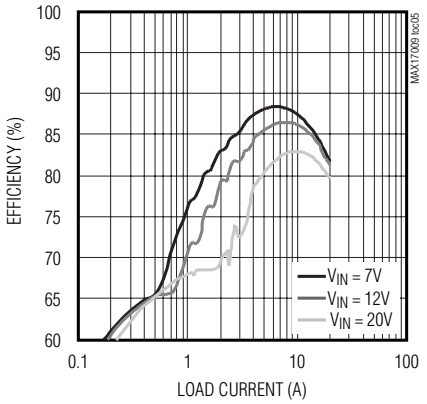
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.2125V, -1.2mV/A DROOP)



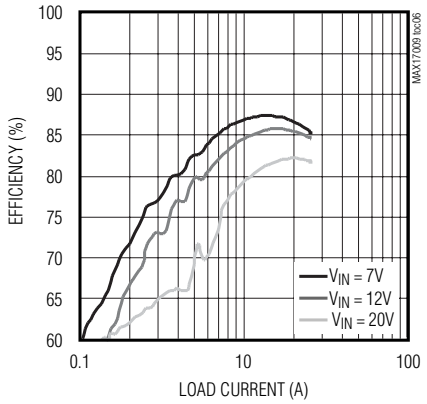
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.2000V, NO DROOP)



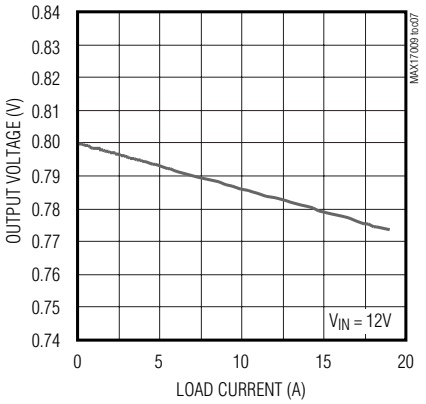
1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.8000V)



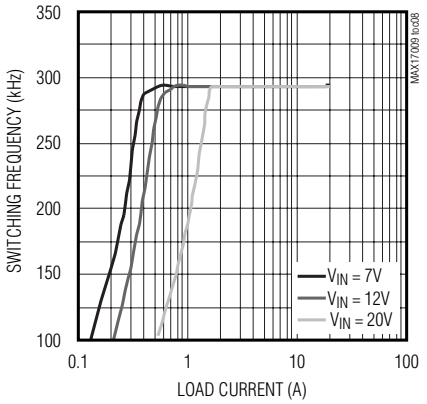
2-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.8000V)



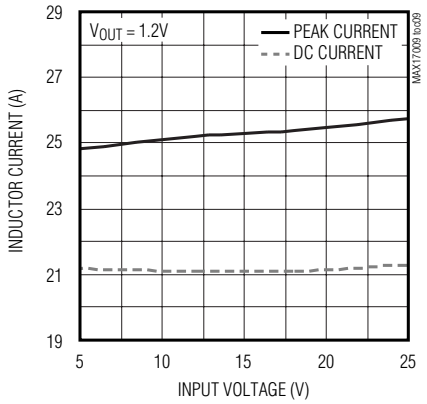
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.8000V, -1.2mV/A DROOP)



1-PHASE SWITCHING FREQUENCY vs. LOAD CURRENT



MAXIMUM INDUCTOR CURRENT vs. INPUT VOLTAGE

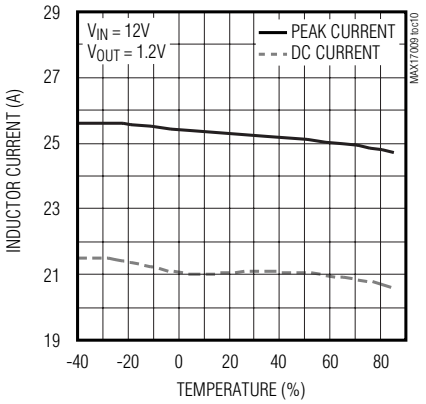


AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

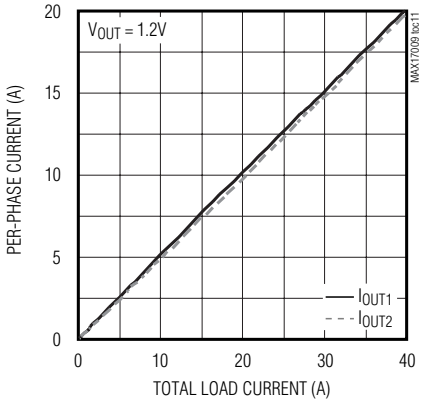
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

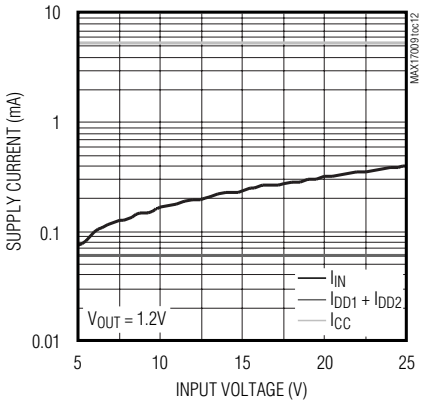
MAXIMUM INDUCTOR CURRENT vs. TEMPERATURE



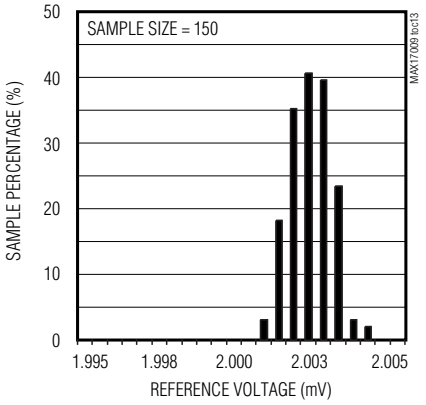
CURRENT BALANCE vs. LOAD CURRENT



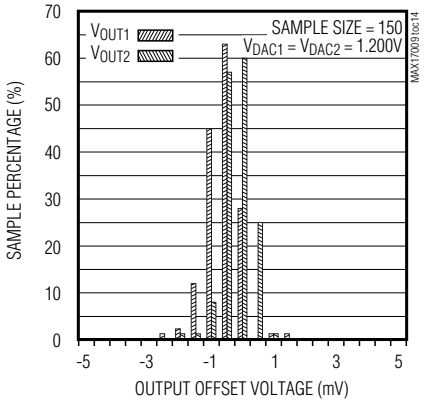
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



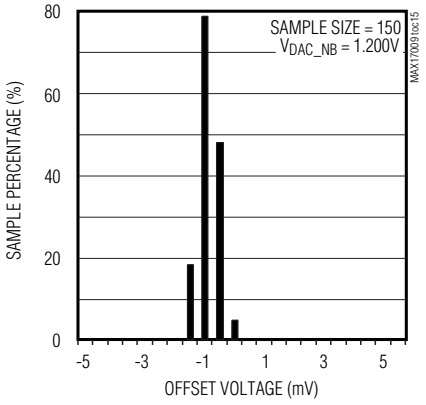
REFERENCE VOLTAGE DISTRIBUTION



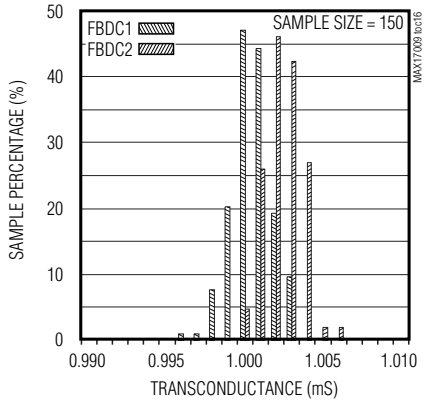
SMPS OUTPUT OFFSET VOLTAGE DISTRIBUTION



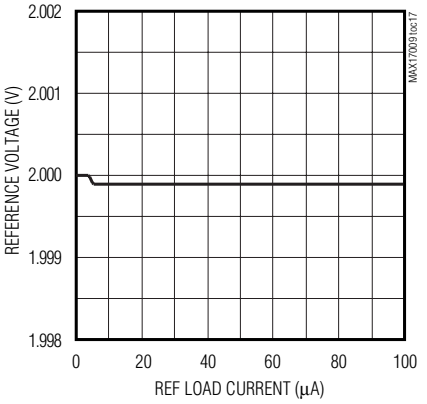
NBV_BUF OFFSET VOLTAGE DISTRIBUTION



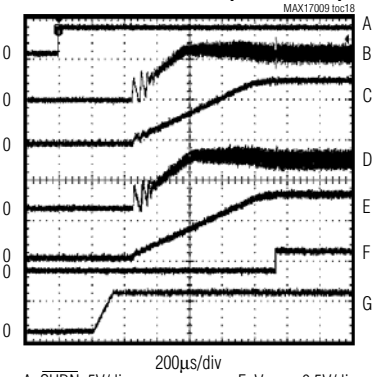
FBDC TRANSCONDUCTANCE DISTRIBUTION



REFERENCE VOLTAGE vs. LOAD CURRENT



STARTUP WAVEFORMS (HEAVY LOAD)



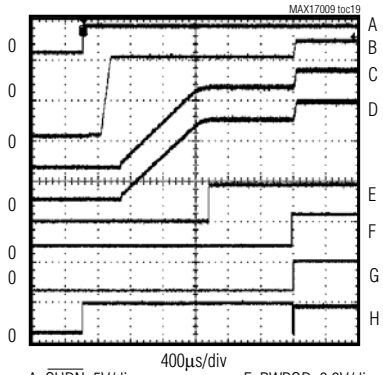
A. $\overline{SHDN}$, 5V/div
B. I_{LX1}, 10A/div
C. V_{OUT1}, 0.5V/div
D. I_{LX2}, 10A/div
E. V_{OUT2}, 0.5V/div
F. PWRGD, 5V/div
G. V_{NBV_BUF}, 0.5V/div

V_{IN} = 12V, V_{BOOT} = 0.8V, I_{LOAD1} = I_{LOAD2} = 12A

Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

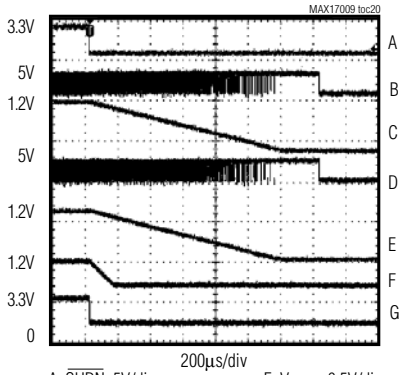
STARTUP SEQUENCE WAVEFORMS



A. $\overline{SHDN}$, 5V/div
B. V_{NBV_BUF}, 0.5V/div
C. V_{OUT1}, 0.5V/div
D. V_{OUT2}, 0.5V/div
E. PWRGD, 3.3V/div
F. PGD_IN, 3.3V/div
G. SVC, 2V/div
H. SVD, 2V/div

V_{IN} = 12V, V_{BOOT} = 1.0V, I_{LOAD1} = I_{LOAD2} = 3A

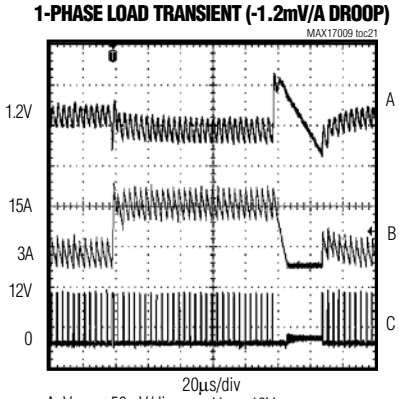
SHUTDOWN WAVEFORMS



A. $\overline{SHDN}$, 5V/div
B. DL1, 10V/div
C. V_{OUT1}, 0.5V/div
D. DL2, 10V/div
E. V_{OUT2}, 0.5V/div
F. V_{NBV_BUF}, 2V/div
G. PWRGD, 5V/div

V_{IN} = 12V, I_{LOAD1} = I_{LOAD2} = 3A

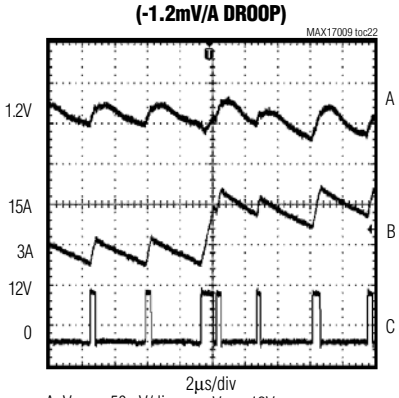
1-PHASE LOAD TRANSIENT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

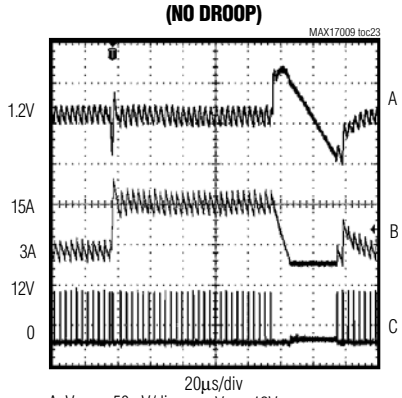
1-PHASE TRANSIENT PHASE REPEAT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

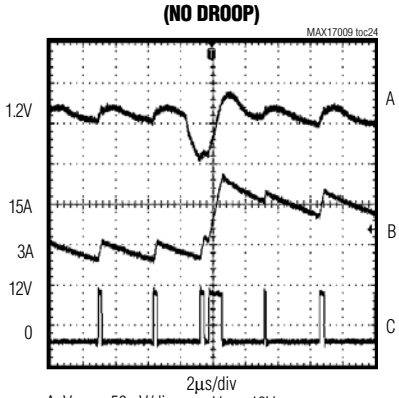
1-PHASE LOAD TRANSIENT (NO DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

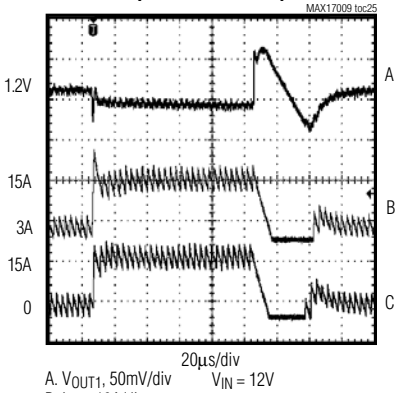
1-PHASE TRANSIENT PHASE REPEAT (NO DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

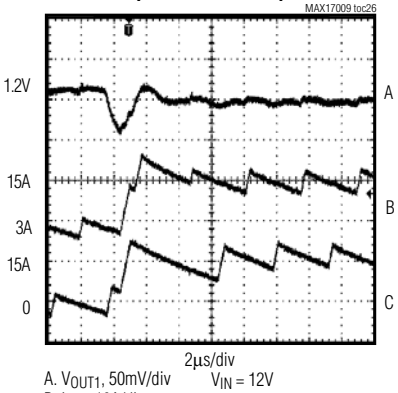
2-PHASE LOAD TRANSIENT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. I_{LX2}, 10A/div

V_{IN} = 12V
I_{LOAD} = 6A TO 30A TO 6A

2-PHASE TRANSIENT PHASE REPEAT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. I_{LX2}, 10A/div

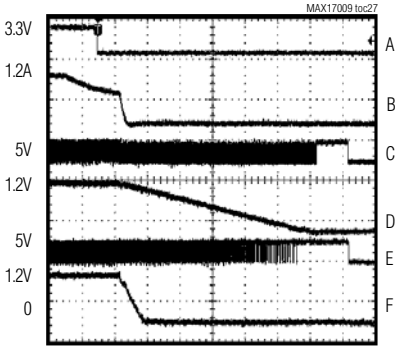
V_{IN} = 12V
I_{LOAD} = 6A TO 30A TO 6A

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

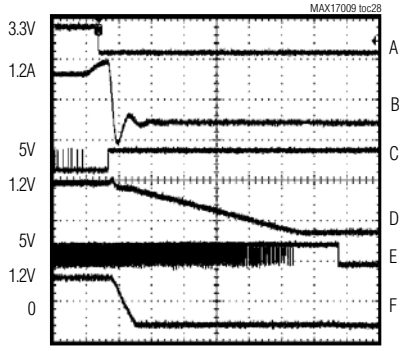
1-PHASE OUTPUT OVERLOAD



A. PWRGD, 5V/div
B. V_{OUT1}, 1V/div
C. DL1, 10V/div
D. V_{OUT2}, 1V/div
E. DL2, 10V/div
F. V_{NBV_BUF}, 1V/div

V_{IN} = 12V, I_{LOAD1} = 3A TO 30A, I_{LOAD2} = 3A

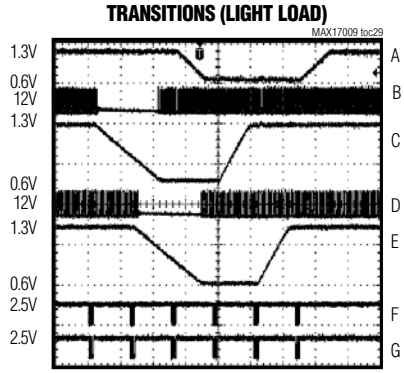
1-PHASE OUTPUT OVERVOLTAGE



A. PWRGD, 5V/div
B. V_{OUT1}, 1V/div
C. DL1, 10V/div
D. V_{OUT2}, 1V/div
E. DL2, 10V/div
F. V_{NBV_BUF}, 1V/div

V_{IN} = 12V, I_{LOAD1} = 50mA, I_{LOAD2} = 3A

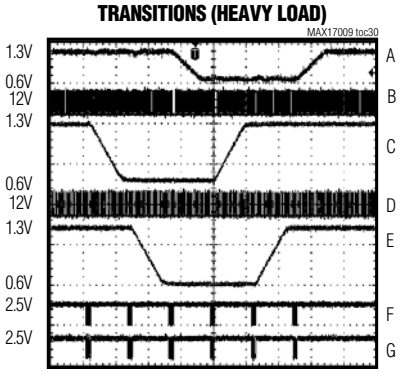
DYNAMIC OUTPUT-VOLTAGE TRANSITIONS (LIGHT LOAD)



A. V_{NBV_BUF}, 1V/div
B. LX1, 20V/div
C. V_{OUT1}, 0.5V/div
D. LX2, 20V/div
E. V_{OUT2}, 0.5V/div
F. SVC, 5V/div
G. SVD, 5V/div

V_{IN} = 12V, V_{DACS} = 1.3V TO 0.6V TO 1.3V,
I_{LOAD1} = I_{LOAD2} = 3A

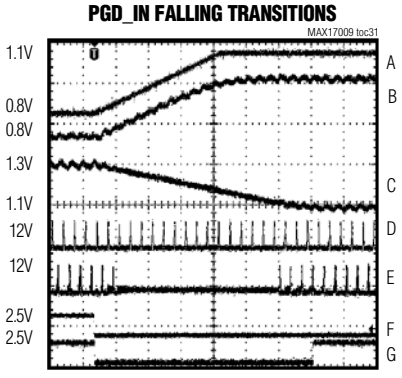
DYNAMIC OUTPUT-VOLTAGE TRANSITIONS (HEAVY LOAD)



A. V_{NBV_BUF}, 1V/div
B. LX1, 20V/div
C. V_{OUT1}, 0.5V/div
D. LX2, 20V/div
E. V_{OUT2}, 0.5V/div
F. SVC, 5V/div
G. SVD, 5V/div

V_{IN} = 12V, V_{DACS} = 1.3V TO 0.6V TO 1.3V,
I_{LOAD1} = I_{LOAD2} = 10A

PGD_IN FALLING TRANSITIONS



A. V_{NBV_BUF}, 200mV/div
B. V_{OUT1}, 200mV/div
C. V_{OUT2}, 200V/div
D. LX1, 20V/div
E. LX2, 20V/div
F. PGD_IN, 5V/div
G. PWRGD, 5V/div

V_{IN} = 12V, V_{BOOT} = 1.1V, V_{DAC1} = 0.8V, V_{DAC2} = 1.3V,
V_{NBV_BUF} = 0.8V, I_{LOAD1} = I_{LOAD2} = 3A

Pin Description

PIN	NAME	FUNCTION
1	PWRGD	Open-Drain, Power-Good Output. PWRGD indicates when both SMPSs are in regulation. PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). After output-voltage transitions, except during power-up and power-down, if FBDC_ is in regulation, then PWRGD is high impedance. During startup, PWRGD is held low an additional 20µs after the MAX17009 reaches the startup boot voltage set by the SVC, SVD pins. The MAX17009 stores the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{SHDN}$. PWRGD is forced low in shutdown. When in pulse-skipping mode, the upper PWRGD threshold comparator is blanked during a lower VID transition. The upper PWRGD threshold comparator is reenabled once the output is in regulation (Figure 4).
2	NBV_BUF	North Bridge Buffered Reference Voltage. This output is connected to the REFIN input of the NB controller (switcher or LDO) to set the NB regulator voltage. The NBV_BUF output current is set by the TIME resistor. The NBV_BUF current and the total output capacitance set the NBV_BUF slew rate: $I_{NBV\_BUF} = (7\mu A) \times (143k\Omega / R_{TIME})$ NBV_BUF Slew rate = $I_{NBV\_BUF} / C_{NBV\_BUF}$ I_{NBV_BUF} is the same during startup, shutdown, and any VID transition. Bypass to GND with a 100pF minimum low-ESR (ceramic) capacitor at the NBV_BUF pin.
3	$\overline{SHDN}$	Shutdown Control Input. Connect high (2V to V_{CC}) for normal operation. Connect to ground to put the IC into its 1µA max shutdown state. During startup, the SMPS output voltages and the NBV_BUF voltage are ramped up to the voltage set by the SVC, SVD inputs. The SMPSs start up and shut down at a fixed slew rate of 1mV/µs. The MAX17009 stores the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{SHDN}$.
4	REF	2.0V Reference Output. Bypass to GND with a 1µF maximum low-ESR (ceramic) capacitor. REF sources up to 500µA for external loads. Loading REF degrades output accuracy, according to the REF load-regulation error.
5	ILIM	Current-Limit Adjust Input. The positive current-limit threshold voltage is precisely 1/20 of the voltage between REF and ILIM over a 0.2V to 1.0V range of V(REF, ILIM). The I_{MIN} minimum current-limit threshold voltage in skip mode is precisely 15% of the corresponding positive current-limit threshold voltage.
6	OSC	Oscillator Adjustment Input. Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase): $f_{OSC} = 300kHz \times 143k\Omega / R_{OSC}$ A 35.7kΩ to 432kΩ corresponds to switching frequencies of 1.2MHz to 100kHz, respectively. Switching-frequency selection is limited by the minimum on-time. See the Switching frequency bullet in the *SMPS Design Procedure* section.

SVC	SVD	BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = V_{CC} OR GND)	BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = OPEN)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

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Pin Description (continued)

PIN	NAME	FUNCTION
7	TIME	Slew-Rate Adjustment Pin. Connect a resistor R_{TIME} from TIME to GND to set the internal slew rate: PWM Slew rate = (6.25mV/µs) x (143kΩ / R_{TIME}) NBV_BUF Slew rate = (7µA) x (143kΩ / R_{TIME}) / C_{NBV_BUF} where R_{TIME} is between 35.7kΩ and 357kΩ for corresponding slew rates between 25mV/µs to 2.5mV/µs, respectively, for the SMPSs, and NBV_BUF currents between 28µA and 2.8µA, respectively, for the NBV_BUF. This slew rate applies to both upward and downward VID transitions, and to the transition from boot mode to VID mode. Downward VID transition slew rate can appear slower because the output transition is not forced by the SMPS. The SMPS slew rate for startup and shutdown is fixed at 1mV/µs. The NBV_BUF slew rate is the same during startup, shutdown, and normal VID transitions.
8	SVC	Serial VID Clock. During the power-up sequence and in debug mode, SVC is the MSB of the 2-bit VID DAC.
9	SVD	Serial VID Data. During the power-up sequence and in debug mode, SVD is the LSB of the 2-bit VID DAC.
10	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components so the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
11	GNDS2	SMPS2 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS2 internally connects to a transconductance amplifier that fine tunes the output voltage compensating for voltage drops from the regulator ground to the load ground. Connect GNDS2 above 0.9V combined-mode operation (unified core). When operating in combined mode, GNDS1 is used as the remote ground-sense input.
12	FBDC2	Output of the DC Voltage-Positioning Transconductance Amplifier for SMPS2. Connect a resistor R_{FBDC2} between FBDC2 and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement: $R_{FBDC2} = R_{DROOPDC} / (R_{SENSE2} \times G_{m(FBDC2)})$ where $R_{DROOPDC}$ is the desired voltage positioning slope and $G_{m(FBDC2)}$ = 1mS typ. R_{SENSE2} is the value of the current-sense resistor that is used to provide the (CSP2, CSN2) current-sense voltage. To disable the load-line, short FBDC2 to the positive remote-sense point. FBDC2 is high impedance in shutdown.
13	FBAC2	Output of the AC Voltage-Positioning Transconductance Amplifier for SMPS2. The resistance between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop: $R_{FBAC2} = R_{DROOPAC} / (R_{SENSE2} \times G_{m(FBAC2)})$ where $R_{DROOPAC}$ is the transient (AC) voltage-positioning slope that provides an acceptable tradeoff between stability and load transient response, $G_{m(FBAC2)}$ and R_{SENSE2} is the value of the current-sense resistor that is used to provide the (CSP2, CSN2) current-sense voltage. The maximum difference between transient (AC) droop and DC droop should not exceed ±80mV at the maximum allowed load current (DC droop is set at the FBDC2 pin). Internally, V(FBDC2 - GNDS2) goes to the internal voltage integrator (slow DC loop), whereas V(FBAC2 - GNDS2) goes to the error comparator (fast transient loop). FBAC2 is high impedance in shutdown. **Note:** The AC and DC droop cannot be different by more than ±3mV/A.
14	V_{DDIO}	CPU I/O Voltage (1.8V or 1.5V). Logic thresholds for SVD and SVC are relative to the voltage at V_{DDIO}.
15	GNDS_NB	North Bridge Feedback Remote-Sense Input, Negative Side. Normally connected to GND directly at the load. GNDS_NB internally connects to a transconductance amplifier that fine tunes the NBV_BUF output voltage compensating for voltage drops from the regulator ground to the load ground.

Pin Description (continued)

PIN	NAME	FUNCTION
16	CSN2	Negative Current-Sense Input for SMPS2. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
17	CSP2	Positive Current-Sense Input for SMPS2. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. Connect CSP2 to V_{CC} to disable SMPS2. This allows the MAX17009 to operate as a 1-phase regulator.
18	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum. A V_{CC} UVLO event that occurs while the IC is functioning is latched, and can only be cleared by cycling V_{CC} power or by toggling $\overline{SHDN}$.
19	$\overline{NBSKP}$	North Bridge Skip Push-Pull Control Output. When $\overline{NBSKP}$ is high, the NB switching regulator is set to forced-PWM mode. When $\overline{NBSKP}$ is low, the NB switching regulator is set to pulse-skipping mode. The $\overline{NBSKP}$ level is set through the serial interface during normal operation. $\overline{NBSKP}$ is high in shutdown and during soft-shutdown. $\overline{NBSKP}$ is high in startup until commanded otherwise.
20	DH2	SMPS2 High-Side, Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
21	LX2	SMPS2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to phase 2's zero-crossing comparator.
22	BST2	Boost Flying-Capacitor Connection for the DH2 High-Side Gate Driver. An internal switch between V_{DD2} and BST2 charges the flying capacitor during the time the low-side FET is on.
23	V_{DD2}	Supply Voltage Input for the DL2 Driver. V_{DD2} is also the supply voltage used to internally recharge the BST2 flying capacitor during the off-time of phase 2. Connect V_{DD2} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD2} to GND with a 1µF or greater ceramic capacitor.
24	DL2	SMPS2 Low-Side Gate-Driver Output. DL2 swings from GND2 to V_{DD2}. DL2 is forced low in shutdown. DL2 is also forced high when an output overvoltage fault is detected. DL2 is forced low in skip mode after an inductor current zero crossing (GND2 - LX2) is detected.
25	GND2	Power Ground for SMPS2. Ground connection for the DL2 driver. Also used as an input to SMPS2's zero-crossing comparator. GND1 and GND2 are internally connected.
26	GND1	Power Ground for SMPS1. Ground connection for the DL1 driver. Also used as an input to SMPS1's zero-crossing comparator. GND1 and GND2 are internally connected.
27	DL1	SMPS1 Low-Side, Gate-Driver Output. DL1 swings from GND1 to V_{DD1}. DL1 is forced low in shutdown. DL1 is also forced high when an output overvoltage fault is detected. DL1 is forced low in skip mode after an inductor current zero crossing (GND1 - LX1) is detected.
28	V_{DD1}	Supply Voltage Input for the DL1 Driver. V_{DD1} is also the supply voltage used to internally recharge the BST1 flying capacitor during the off-time of phase 1. Connect V_{DD1} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD1} to GND with a 1µF or greater ceramic capacitor.
29	BST1	Boost Flying-Capacitor Connection for the DH1 High-Side Gate Driver. An internal switch between V_{DD1} and BST1 charges the flying capacitor during the time the low-side FET is on.
30	LX1	SMPS1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to phase 1's zero-crossing comparator.
31	DH1	SMPS1 High-Side, Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
32	$\overline{VRHOT}$	Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{VRHOT}$ is high impedance in shutdown.

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Pin Description (continued)

PIN	NAME	FUNCTION
33	$\overline{PRO}$	Protection Disable. $\overline{PRO}$ also sets the MAX17009 in debug mode. Connect $\overline{PRO}$ high to disable OVP protection. Connect $\overline{PRO}$ to GND to enable OVP protection. When $\overline{PRO}$ is floated, the MAX17009 disables the OVP protection and also enters debug mode (see the $\overline{SHDN}$ pin description). When PGD_IN is low in debug mode, the MAX17009 DAC voltages are set by the 2-bit boot VID. When PGD_IN is high, the MAX17009 changes to serial VID mode.
34	CSP1	Positive Current-Sense Input for SMPS1. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
35	CSN1	Negative Current-Sense Input for SMPS1. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
36	PGD_IN	System Power-Good Input. Indicates to the MAX17009 that the system is ready to enter serial VID mode. PGD_IN is low when $\overline{SHDN}$ first goes high, the MAX17009 decodes the boot VID to determine the boot voltage. The boot VID can be changed dynamically while PGD_IN remains low and PWRGD. The boot VID is stored after PWRGD goes high. PGD_IN goes high after the MAX17009 reaches the boot voltage. This indicates that the SVI block is active, and the MAX17009 starts to respond to the serial-interface commands. After PGD_IN has gone high, if at anytime PGD_IN should go low, the MAX17009 regulates to the previously stored boot VID.
37	OPTION	Four-Level Input to Enable Offset and Transient-Phase Repeat **OPTION** / **OFFSET ENABLED** / **TRANSIENT-PHASE REPEAT ENABLED** V_{CC} / 0 / 0 OPEN / 0 / 1 REF / 1 / 0 GND / 1 / 1 When OFFSET is enabled, the MAX17009 enables a fixed +12.5mV offset on each of the SMPS VID codes after PGD_IN goes high. This configuration is intended for applications that implement a load-line. An external resistor at FBDC_ sets the load-line. The offset can be disabled by setting the PSI_L bit to zero through the serial interface. When OFFSET is disabled, the intended application has no load-line, and the FBDC_ pins are directly connected to the remote-sense points. Transient phase repeat allows the MAX17009 to reenable the current phase in response to a load transient, even after that phase has finished its on-pulse.
38	FBAC1	Output of the AC Voltage-Positioning Transconductance Amplifier for SMPS1. The resistance between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop: $R_{FBAC1} = R_{DROOPAC} / (R_{SENSE1} \times G_{m(FBAC1)})$ where $R_{DROOPAC}$ is the transient (AC) voltage-positioning slope that $\overline{PRO}$vides an acceptable tradeoff between stability and load-transient response, $G_{m(FBAC1)}$ and R_{SENSE1} is the value of the current-sense resistor that is used to $\overline{PRO}$vide the (CSP1, CSN1) current-sense voltage. The maximum difference between transient (AC) droop and DC droop should not exceed ±80mV at the maximum allowed load current (DC droop is set at the FBDC2 pin). Internally, V(FBDC1 - GNDS1) goes to the internal voltage integrator (slow DC loop), whereas V(FBAC1 - GNDS1) goes to the error comparator (fast-transient loop). FBAC1 is high impedance in shutdown. **Note:** The AC and DC droop cannot be different by more than ±3mV/A.

Pin Description (continued)

PIN	NAME	FUNCTION
39	FBDC1	Output of the DC Voltage-Positioning Transconductance Amplifier for SMPS1. Connect a resistor R_{FBDC1} between FBDC1 and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement: $R_{FBDC1} = R_{DROOPDC} / (R_{SENSE1} \times G_{m(FBDC1)})$ where $R_{DROOPDC}$ is the desired voltage-positioning slope and $G_{m(FBDC1)}$ = 1mS typ. R_{SENSE1} is the value of the current-sense resistor that is used to $\overline{PRO}$vide the (CSP1, CSN1) current-sense voltage. To disable the load-line, short FBDC2 to the positive remote-sense point. FBDC1 is high impedance in shutdown.
40	GNDS1	SMPS1 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS1 internally connects to a transconductance amplifier that fine tunes the output voltage compensating for voltage drops from the regulator ground to the load ground. GNDS1 is the remote ground-sense input in combined-mode operation.
EP	EP	Exposed Pad. Connect the exposed backside pad to GND1 and GND2.

Table 1 shows the component selection for standard applications and Table 2 lists component suppliers.

Table 1. Component Selection for Standard Applications

COMPONENT	V_{IN} = 7V TO 20V V_{OUT} = 1.0V - 1.3V / 18A PER PHASE	V_{IN} = 4.5V TO 14V $V_{OUT\_}$ = 1.0V - 1.3V / 18A PER PHASE
MODE	Separate, 2-phase mobile (GNDS2 not high)	Separate, 2-phase mobile (GNDS2 not high)
Switching Frequency	280kHz (R_{OSC} = 154kΩ)	600kHz (R_{OSC} = 71.5kΩ)
$C_{IN\_}$, Input Capacitor (per Phase)	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(2) 10µF, 16V Taiyo Yuden TMK432BJ106KM
$C_{OUT\_}$, Output Capacitor (per Phase)	(2) 470µF, 2V, 6mΩ, low-ESR capacitor NEC/Tokin PSGD0E477M6 or Panasonic EEFUD0D471L6	(2) 330µF, 2.5V, 6mΩ, low-ESR capacitor Panasonic EEFSD0D331XR
$N_{H\_}$ High-Side MOSFET	(1) Fairchildsemi FDMS8690	(1) International Rectifier IRF7811W
$N_{L\_}$ Low-Side MOSFET	(2) Vishay Si7336ADP	(2) Fairchildsemi FDMS8660S
$D_{L\_}$ Schottky Rectifier	3A, 40V Schottky diode Central Semiconductor CMSH3-40	None
L_ Inductor	0.45µH, 30A, 1.1mΩ power inductor TOKO FDUE1040D-R45M or NEC/Tokin MPC1040LR45	0.22µH, 25A, 1mΩ power inductor NEC/Tokin MPC0730LR20

Note: Mobile applications should be designed for separate mode operation. Component selection dependent on AMD CPU AC and DC specifications.

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET	www.kemet.com
NEC Tokin	www.nec-tokin.com
Panasonic	www.panasonic.com

MANUFACTURER	WEBSITE
Pulse	www.pulseeng.com
Renesas	www.renesas.com
SANYO	www.secc.co.jp
Siliconix (Vishay)	www.vishay.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com

Standard Application Circuits

The MAX17009 standard application circuit (Figure 2) generates two independent 18A outputs for AMD mobile CPU applications. See Table 1 for component selections. Table 2 lists the component manufacturers.

Detailed Description

The MAX17009 consists of a dual-fixed-frequency PWM controller that generates the supply voltage for two independent CPU cores. A reference buffer output (NBV_BUF) sets the regulation voltage for a separate NB regulator. The CPU cores can be configured as independent outputs, or as a combined output based on the GNDS2 pin strap (GNDS2 pulled to 1.5V - 1.8V, which are the respective voltages for DDR3 and DDR2).

Both SMPS outputs and the NB buffer can be programmed to any voltage in the VID table (see Table 4) using the SVI. The CPU is the SVI bus master, while the MAX17009 is the SVI slave. Voltage transitions are commanded by the CPU as a single-step command from one VID code to another. The MAX17009 slews the SMPS outputs at the slew rate programmed by the external R_{TIME} resistor. For the NB buffer, the slew rate is set by the combination of R_{TIME} and the total capacitance on the output of the buffer.

By default, the MAX17009 SMPSs are always in pulse-skip mode. In separate mode, the PSI_L bit does not change the mode of operation, but removes the +12.5mV offset, if enabled by the OPTION pin. In combined mode, the PSI_L bit removes the +12.5mV offset and switches from 2-phase to 1-phase operation. The $\overline{NB\_SKP}$ output always follows the state of PSI_L for the NB regulator.

+5V Bias Supply (V_{CC}, V_{DD})

The MAX17009 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's main 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers.

The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}Q_G = 10mA \text{ to } 60mA \text{ (typ)}$$

where I_{CC} is provided in the *Electrical Characteristics* table, and $f_{SW}Q_G$ (per phase) is the driver's supply current, as defined in the MOSFET's data sheet. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (OSC)

Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase):

$$f_{SW} = 300kHz \times 143k\Omega / R_{OSC}$$

A 35.7kΩ to 432kΩ corresponds to switching frequencies of 1.2MHz to 100kHz, respectively. High-frequency (1.2MHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (100kHz) operation offers the best overall efficiency at the expense of component size and board space. Minimum on-time ($t_{ON(MIN)}$) must also be taken into consideration. See the Switching frequency bullet in the *SMPS Design Procedure* section.

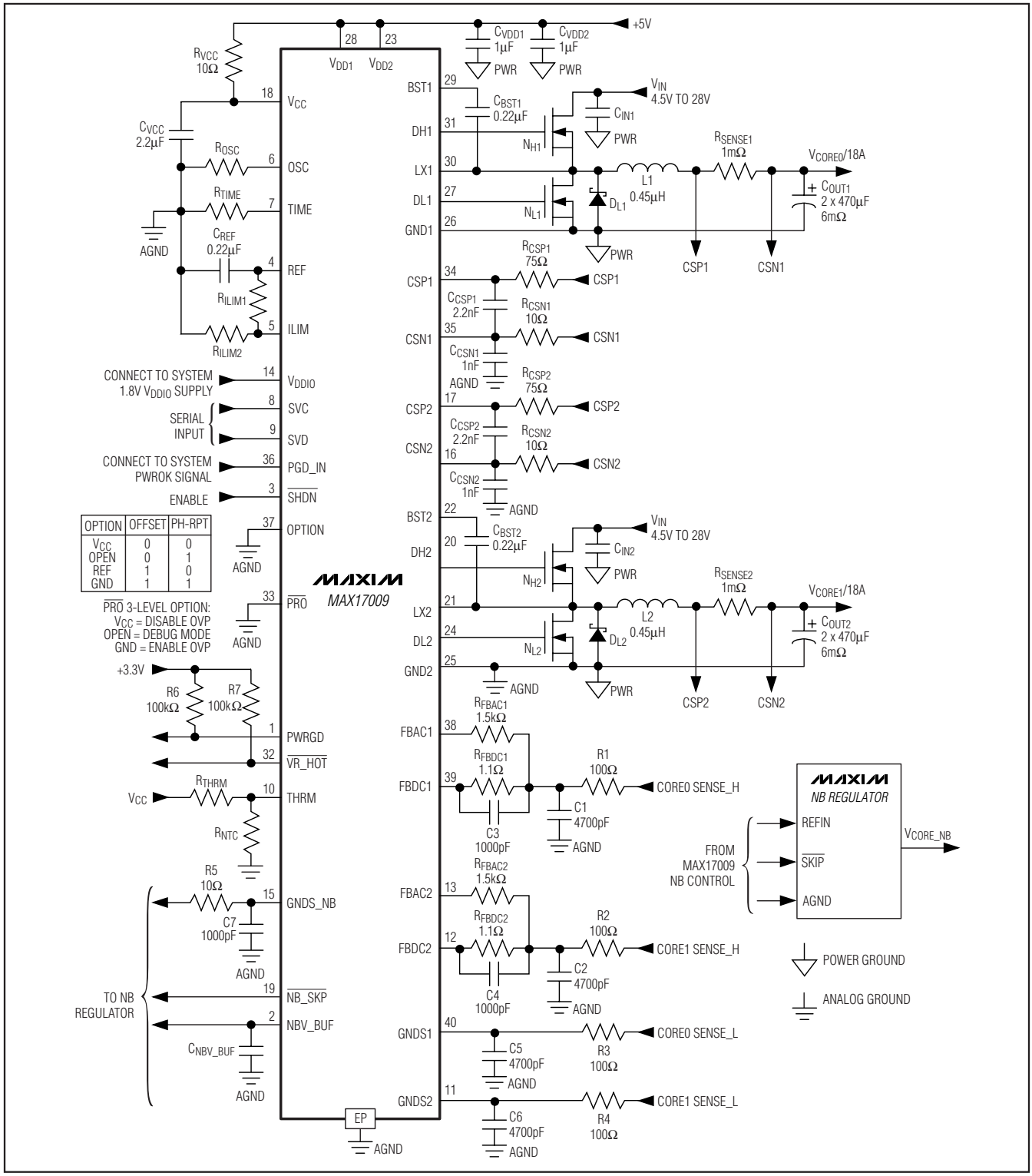

Figure 2. Standard Application Circuit

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Interleaved Multiphase Operation

The MAX17009 interleaves both phases—resulting in 180° out-of-phase operation that minimizes the input and output filtering requirements, reduces electromagnetic interference (EMI), and improves efficiency. The high-side MOSFETs do not turn on simultaneously during normal operation. The instantaneous input current is effectively reduced by the number of active phases, resulting in reduced input-voltage ripple, ESR power loss, and RMS ripple current (see the *Input-Capacitor Selection* section). Therefore, the controller achieves high performance while minimizing the component count, which reduces cost, saves board space, and lowers component power requirements, making the MAX17009 ideal for high-power, cost-sensitive applications.

Transient-Phase Repeat

When a transient occurs, the output-voltage deviation depends on the controller's ability to quickly detect the transient and slew the inductor current. A fixed-frequency controller typically responds only when a clock edge occurs, resulting in a delayed transient response. To minimize this delay time, the MAX17009 includes enhanced transient detection and transient- phase-repeat capabilities. If the controller detects that the output voltage has dropped by 25mV, the transient-detection comparator immediately retriggers the phase that completed its on-time last. The controller triggers the subsequent phases as normal on the appropriate oscillator edges. This effectively triggers a phase a full cycle early, increasing the total inductor-current slew rate and providing an immediate transient response.

The OPTION pin setting enables or disables the transient phase-repeat feature. Keep OPTION OPEN or connected to GND to enable transient-phase repeat. Connect OPTION to V_{CC} or REF to disable transient-phase repeat. See the *Offset and Transient-Phase Repeat (OPTION)* section.

Feedback Adjustment Amplifiers

Steady-State Voltage-Positioning Amplifier (DC Droop)

Each of the MAX17009 SMPS controllers includes two transconductance amplifiers—one for steady-state DC droop, and another for AC droop. The amplifiers' inputs are generated by summing their respective current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR.

The DC droop amplifier's output (FBDC) connects to the remote-sense point of the output through a resistor that sets each phase's DC voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FBDC} I_{FBDC}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the FBDC amplifier's output current (I_{FBDC}) is determined by each phase's current-sense voltage:

$$I_{FBDC} = G_{m(FBDC)} V_{CS}$$

where $V_{CS} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{M(FBDC)}$ is typically 1mS as defined in the *Electrical Characteristics* table.

DC droop is typically used together with the +12.5mV offset feature to keep within the DC tolerance window of the application. See the *Offset and Transient-Phase Repeat* (*OPTION)* section. The ripple voltage on FBDC must be less than the 18mV (min) transient phase repeat threshold:

$$\Delta I_L R_{SENSE} G_{m(FBDC)} R_{FBDC} + \Delta I_L R_{ESR} \le 18mV$$

$$R_{FBDC} \le \left(\frac{18mV}{\Delta I_L} - R_{ESR} \right) - R_{SENSE} G_{m(FBDC)}$$

where ΔI_L is the inductor ripple current, R_{ESR} is the effective output ESR at the remote sense point, R_{SENSE} is the current-sense element, and $G_{m(FBDC)}$ is 1.03mS (max) as defined in the *Electrical Characteristics* table. The worst-case inductor ripple occurs at the maximum input voltage and the minimum output-voltage conditions:

$$\Delta I_{L(MAX)} = \frac{V_{OUT(MIN)} \left(V_{IN(MAX)} - V_{OUT(MIN)} \right)}{V_{IN(MAX)} f_{OSC} L}$$

To disable voltage positioning, set R_{FBDC} to zero.

Transient Voltage-Positioning Amplifier (AC Droop)

The AC droop amplifier's output (FBAC) connects to the remote-sense point of the output through a resistor that sets each phase's AC voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FBAC} I_{FBAC}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the FBAC amplifier's output current (I_{FBAC}) is determined by each phase's current-sense voltage:

$$I_{FBAC} = G_{m(FBAC)} V_{CS}$$

where $V_{CS} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{M(FBAC)}$ is 1.03mS (max), as defined in the *Electrical Characteristics* table.

AC droop is required for stable operation of the MAX17009. A minimum of 1mV/A is recommended. AC droop must not be disabled.

The maximum allowable AC droop is limited by the recommended integrator correction range of ±100mV and on the DC droop:

$$\left|R_{FBAC} - R_{FBDC}\right| \le \frac{100mV}{1.03mS I_{LOAD(MAX)} R_{SENSE}}$$

Differential Remote Sense

The MAX17009 controller includes independent differential, remote-sense inputs for each CPU core to eliminate the effects of voltage drops along the PC board (PCB) traces and through the processor's power pins. The feedback-sense (FBDC_) input connects to the voltage-positioning resistor ($R_{FBDC\_}$). The ground-sense (GNDS_) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the feedback-sense (FBDC_) voltage-positioning resistor ($R_{FBDC\_}$), and ground-sense (GNDS_) input directly to the respective CPU core's remote-sense outputs as shown in Figure 2.

GNDS2 has a dual function. At power-on, the voltage level on GNDS2 configures the MAX17009 as two independent switching regulators, or one higher current two-phase regulator. Keep GNDS2 low during power-up to configure the MAX17009 in separate mode. Connect GNDS2 to a voltage above 0.8V (typ) for combined-mode operation. In the AMD mobile system, this is automatically done by the CPU that is plugged into the socket that pulls GNDS2 to the V_{DDIO} voltage level.

The MAX17009 checks the GNDS2 level at the time when the internal REFOK signal goes high, and latches the operating mode information (separate or combined mode). This latch is cleared by cycling the $\overline{SHDN}$ pin.

Integrator Amplifier

An internal integrator amplifier forces the DC average of the FBDC_ voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 3), allowing accurate DC output-voltage regulation regardless of the output-ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±100mV (min).

The MAX17009 disables the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode. The integrator remains disabled until 20µs after the transition is completed (the internal target settles), and the output is in regulation (edge detected on the error comparator).

When voltage positioning is disabled ($R_{FBDC\_}$ = 0Ω), the AC droop setting must be less than the ±100mV minimum adjustment range of the integrator amplifier to guarantee proper DC output-voltage accuracy. See the *Steady State Voltage-Positioning Amplifiers (DC Droop)* and the *Transient Voltage-Positioning Amplifiers (AC Droop)* sections.

2-Wire Serial Interface (SVC, SVD)

The MAX17009 supports the 2-wire, write only, serial-interface bus as defined by the AMD Serial VID Interface Specification. The serial interface is similar to the high-speed 3.4MHz I^2C bus, but without the master mode sequence. The bus consists of a clock line (SVC) and a data line (SVD). The CPU is the bus master, and the MAX17009 is the slave. The MAX17009 serial interface works from 100kHz to 3.4MHz. In the AMD mobile application, the bus runs at 3.4MHz.

The serial interface is active only after PGD_IN goes high in the startup sequence. The CPU sets the VID voltage of the three internal DACs and the PSI_L bit through the serial interface.

During the startup sequence, the SVC and SVD inputs serve an alternate function to set the 2-bit boot VID for all three DACs while PWRGD is low. In debug mode, the SVC and SVD inputs function in the 2-bit VID mode when PGD_IN is low, and in the serial-interface mode when PGD_IN is high.

Nominal Output-Voltage Selection

SMPS Output Voltage

The nominal no-load output voltage ($V_{TARGET\_}$) for each SMPS is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) and the offset voltage (V_{OFFSET}) as defined in the following equation:

$$V_{TARGET} = V_{FBDC} = V_{DAC} + V_{GNDS} + V_{OFFSET}$$

where V_{DAC} is the selected VID voltage of the SMPS DAC, V_{GNDS} is the ground-sense correction voltage, and V_{OFFSET} is the +12.5mV offset enabled by the OPTION pin, when the PSI_L is set high.

NBV_BUF Output Voltage

The nominal output voltage (V_{TARGET}) for the NBV_BUF is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}), as defined in the following equation:

$$V_{TARGET} = V_{NBV\_BUF} = V_{DAC} + V_{GNDS\_NB}$$

where $V_{DAC\_}$ is the selected VID voltage of the NBV_BUF DAC, and $V_{GNDS\_NB\_}$ is the ground-sense correction voltage. The offset voltage (V_{OFFSET}) is not applied to NBV_BUF.

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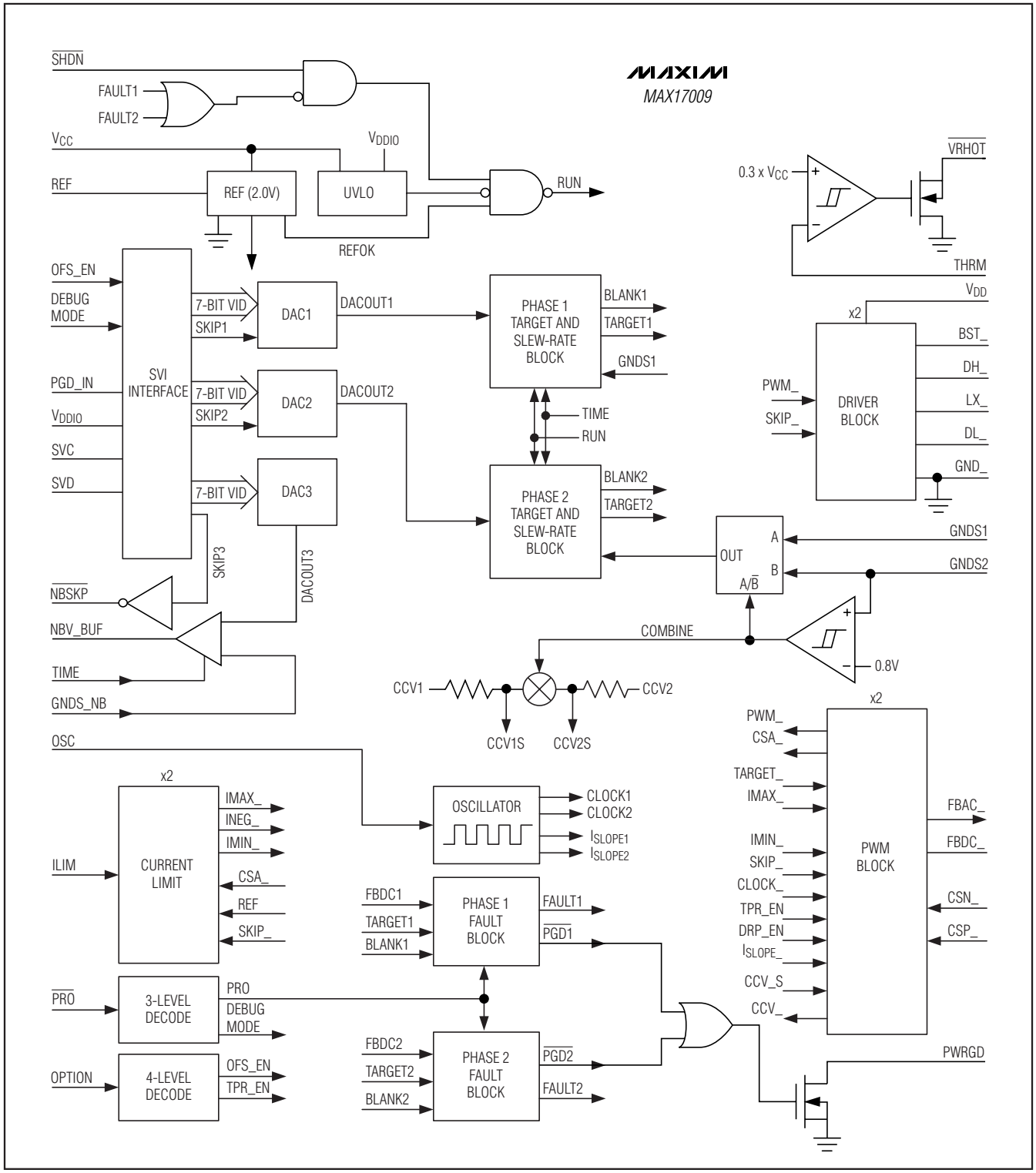

Figure 3. Functional Diagram

7-Bit DAC

Inside the MAX17009 are three 7-bit digital-to-analog converters (DACs). Each DAC can be individually programmed to different voltage levels through the serial-interface bus. The DAC sets the target for the output voltage for the SMPSs and the NB buffer output (NBV_BUF). The available DAC codes and resulting output voltages are compatible with the AMD SVI (Table 4) specifications

Boot Voltage

On startup, the MAX17009 slews the target for all three DACs from ground to the boot voltage set by the SVC and SVD pin voltage levels. While the output is still below regulation, the SVC and SVD levels can be changed, and the MAX17009 sets the DACs to the new boot voltage. Once the programmed boot voltage is reached and PWRGD goes high, the MAX17009 stores the boot VID. Changes in the SVC and SVD settings do not change the output voltage once the boot VID is stored. When PGD_IN goes high, the MAX17009 exits boot mode, and the three DACs can be independently set to any voltage in the VID table through the serial interface.

If PGD_IN goes from high to low anytime after the boot VID is stored, the MAX17009 sets all three DACs back to the voltage of the stored boot VID.

When in debug mode ($\overline{PRO}$ = OPEN), the MAX17009 uses a different boot-voltage code set. Keeping PGD_IN low allows the SVC and SVD inputs to set the three DACs to different voltages in the boot-voltage code table. When PGD_IN is subsequently set high, the three DACs can be independently set to any voltage in the VID table serial interface. Table 3 shows the boot-voltage code table.

Table 3. Boot-Voltage Code Table

SVC	SVD	BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = V_{CC} OR GND)	BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = OPEN)
0	0	1.1	1.4
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Offset

A +12.5mV offset can be added to both SMPS DAC voltages for applications that include DC droop. The offset is applied only after the MAX17009 exits boot mode (PGD_IN going from low to high), and the MAX17009 enters the serial-interface mode. The offset is disabled when the PSI_L bit is set, saving more power when the load is light.

The OPTION pin setting enables or disables the +12.5mV offset. Connect OPTION to REF or GND to enable the offset. Keep OPTION open or connected to V_{CC} to disable the offset. See the *Offset and Transient-Phase Repeat (OPTION)* section.

Output-Voltage Transition Timing

SMPS Output-Voltage Transition

The MAX17009 performs positive voltage transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance. The slew rate (set by resistor R_{TIME}) must be set fast enough to ensure that 35.7kΩ and 357kΩ for corresponding slew rates between 25mV/µs to 2.5mV/µs, respectively, for the SMPSs.

At the beginning of an output-voltage transition, the MAX17009 blanks both PWRGD comparator thresholds, preventing the PWRGD open-drain output from changing states during the transition. At the end of an upward VID transition, the controller enables both PWRGD thresholds approximately 20µs after the slew-rate controller reaches the target output voltage. At the end of a downward VID transition, the upper PWRGD threshold is enabled only after the output reaches the lower VID code setting.

The MAX17009 automatically controls the current to the minimum level required to complete the transition in the calculated time. The slew-rate controller uses an internal capacitor and current source programmed by R_{TIME} to transition the output voltage. The total transition time depends on R_{TIME}, the voltage difference, and the accuracy of the slew-rate controller (C_{SLEW} accuracy). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit set by ILIM. For all dynamic positive VID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt = 6.25mV/µs x 143kΩ / R_{TIME} is the slew rate, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See the TIME Slew-Rate Accuracy row in the *Electrical Characteristics* table for slew-rate limits.

The output voltage tracks the slewed target voltage, making the transitions relatively smooth. The average inductor current per phase required to make an output-voltage transition is:

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$$I_L \cong C_{OUT} \times (dV_{TARGET}/dt)$$

where dV_{TARGET}/dt is the required slew rate, C_{OUT} is the total output capacitance.

The MAX17009 SMPSs remain in a pulse-skipping mode even during upward and downward VID transitions. As such, downward VID transitions are not forced, and the output voltage may take a longer time to settle to the lower VID code. The discharge rate of the output voltage during downward transitions is dependent on the load current and total output capacitance for loads less than a minimum current, and dependent on the R_{TIME} programmed slew rate for heavier loads. The critical load current ($I_{LOAD(CRIT)}$) where the transition time is dependent on the load is:

$$I_{LOAD(CRIT)} \cong C_{OUT} \times (dV_{TARGET}/dt)$$

For load currents less than $I_{LOAD(CRIT)}$, the transition time is:

$$t_{TRANS} \cong \frac{C_{OUT} \times dV_{TARGET}}{I_{LOAD}}$$

For soft-start and shutdown, the controller uses a fixed slew rate of 1mV/µs. Figure 4 is the VID transition timing diagram. Table 4 shows the output-voltage VID DAC codes.

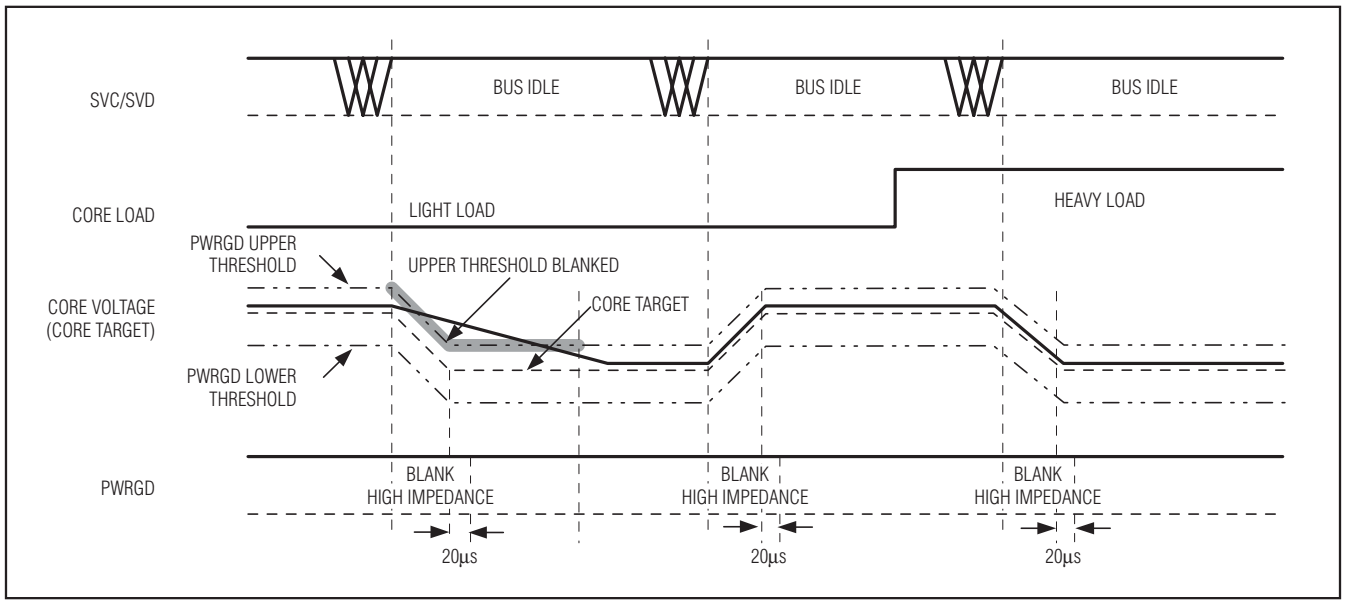

Figure 4. VID Transition Timing Figure

Table 4. Output Voltage VID DAC Codes

SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)
000_0000	1.5500	010_0000	1.1500	100_0000	0.7500	110_0000	0.3500
000_0001	1.5375	010_0001	1.1375	100_0001	0.7375	110_0001	0.3375
000_0010	1.5250	010_0010	1.1250	100_0010	0.7250	110_0010	0.3250
000_0011	1.5125	010_0011	1.1125	100_0011	0.7125	110_0011	0.3125
000_0100	1.5000	010_0100	1.1000	100_0100	0.7000	110_0100	0.3000
000_0101	1.4875	010_0101	1.0875	100_0101	0.6875	110_0101	0.2875
000_0110	1.4750	010_0110	1.0750	100_0110	0.6750	110_0110	0.2750
000_0111	1.4625	010_0111	1.0625	100_0111	0.6625	110_0111	0.2625
000_1000	1.4500	010_1000	1.0500	100_1000	0.6500	110_1000	0.2500
000_1001	1.4375	010_1001	1.0375	100_1001	0.6375	110_1001	0.2375

Table 4. Output Voltage VID DAC Codes (continued)

SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)	SVID[6:0]	OUTPUT VOLTAGE (V)
000_1010	1.4250	010_1010	1.0250	100_1010	0.6250	110_1010	0.2250
000_1011	1.4125	010_1011	1.0125	100_1011	0.6125	110_1011	0.2125
000_1100	1.4000	010_1100	1.0000	100_1100	0.6000	110_1100	0.2000
000_1101	1.3875	010_1101	0.9875	100_1101	0.5875	110_1101	0.1875
000_1110	1.3750	010_1110	0.9750	100_1110	0.5750	110_1110	0.1750
000_1111	1.3625	010_1111	0.9625	100_1111	0.5625	110_1111	0.1625
001_0000	1.3500	011_0000	0.9500	101_0000	0.5500	111_0000	0.1500
001_0001	1.3375	011_0001	0.9375	101_0001	0.5375	111_0001	0.1375
001_0010	1.3250	011_0010	0.9250	101_0010	0.5250	111_0010	0.1250
001_0011	1.3125	011_0011	0.9125	101_0011	0.5125	111_0011	0.1125
001_0100	1.3000	011_0100	0.9000	101_0100	0.5000	111_0100	0.1000
001_0101	1.2875	011_0101	0.8875	101_0101	0.4875	111_0101	0.0875
001_0110	1.2750	011_0110	0.8750	101_0110	0.4750	111_0110	0.0750
001_0111	1.2625	011_0111	0.8625	101_0111	0.4625	111_0111	0.0625
001_1000	1.2500	011_1000	0.8500	101_1000	0.4500	111_1000	0.0500
001_1001	1.2375	011_1001	0.8375	101_1001	0.4375	111_1001	0.0375
001_1010	1.2250	011_1010	0.8250	101_1010	0.4250	111_1010	0.0250
001_1011	1.2125	011_1011	0.8125	101_1011	0.4125	111_1011	0.0125
001_1100	1.2000	011_1100	0.8000	101_1100	0.4000	111_1100	0
001_1101	1.1875	011_1101	0.7875	101_1101	0.3875	111_1101	0
001_1110	1.1750	011_1110	0.7750	101_1110	0.3750	111_1110	0
001_1111	1.1625	011_1111	0.7625	101_1111	0.3625	111_1111	0

NBV_BUF Output-Voltage Transition

The MAX17009 includes a buffered output voltage that sets the target for the NB regulator. When a voltage transition on the NB DAC occurs, the NBV_BUF sources or sinks a programmed current on its output. The programmed current (I_{NBV_BUF}) is set by R_{TIME}. R_{TIME} is between 35.7kΩ and 357kΩ for corresponding I_{NBV_BUF} between 28µA and 2.8µA, respectively:

$$I_{NBV\_BUF} = (7\mu A) \times (143k\Omega / R_{TIME})$$

I_{NBV_BUF} and the external capacitor (C_{NBV_BUF}) set the voltage slew rate of the NBV_BUF:

$$dV_{NBV\_BUF}/dt = I_{NBV\_BUF} / C_{NBV\_BUF}$$

Program the NB regulator with a slew rate faster than that set by NBV_BUF to allow the NBV_BUF to control the NB regulator's output slew rate.

Alternatively, the NB regulator can be programmed with the desired slew rate, and the NBV_BUF voltage can approach a step function by keeping C_{NBV_BUF} small. A minimum of 100pF capacitor is required.

Pulse-Skipping Operation

The SMPS of the MAX17009 always operates in pulse-skipping mode. Pulse-skipping mode enables the driver's zero-crossing comparator, so the driver pulls its DL low when "zero" inductor current is detected (V_{GND} - V_{LX} = 0). This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output.

In the pulse-skipping operation, the controller terminates the on-time when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the Idle Mode current-sense threshold (V_{IDLE} = 0.15 x V_{LIMIT}). Under heavy-load conditions, the continuous inductor current remains above the Idle Mode current-sense threshold, so the on-time depends only on the feedback-voltage threshold. Under light-load conditions, the controller remains above the feedback voltage threshold, so the on-time duration depends solely on the Idle Mode current-sense threshold, which is approximately 15% of the full-load peak current-limit threshold set by ILIM.

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During downward VID transitions, the controller temporarily sets the OVP threshold to 1.85V (typ), preventing false OVP faults. Once the error amplifier detects that the output voltage is in regulation, the OVP threshold tracks the selected VID DAC code. The MAX17009 automatically uses forced-PWM operation during soft-shutdown.

When configured for separate-mode operation, both SMPSs remain in pulse-skipping mode, regardless of the PSI_L bit state.

When configured for combined-mode operation, the PSI_L bit sets the MAX17009 in 1-phase pulse-skipping mode or 2-phase pulse-skipping mode.

Idle Mode Current-Sense Threshold

The Idle Mode current-sense threshold forces a lightly loaded regulator to source a minimum amount of power with each on-time since the controller cannot terminate the on-time until the current-sense voltage exceeds the Idle Mode current-sense threshold (V_{IDLE} = 0.15 x V_{LIMIT}). Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses to avoid overcharging the output. When the clock edge occurs, if the output voltage still exceeds the feedback threshold, the controller does not initiate another on-time. This forces the controller to actually regulate the valley of the output voltage ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, the MAX17009 zero-crossing comparators are active. Therefore, an inherent automatic switchover to PFM takes place at light loads, resulting in a highly efficient operating mode. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The driver's zero-crossing comparator senses the inductor current across the low-side MOSFET. Once V_{GND} - V_{LX} drops below the zero-crossing threshold, the driver forces DL low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical-conduction" point). The load-current level at which the PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is given by:

$$I_{LOAD(SKIP)} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{2V_{IN}f_{SW}L}$$

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output-voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Current Sense

The output current of each phase is sensed differentially. A low offset voltage and high gain (10V/V) differential current amplifier at each phase allows low-resistance current-sense resistors to be used to minimize power dissipation. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 5). The time constant of the RC network should match the inductor's time constant (L/R_{DCR}):

$$\frac{L}{R_{DCR}} = R_{EQ}C_{SENSE}$$

where C_{SENSE} and R_{EQ} are the time-constant matching components. To minimize the current-sense error due to the current-sense inputs' bias current (I_{CSP} and I_{CSN}), choose R_{EQ} less than 2kΩ and use the above equation to determine the sense capacitance (C_{SENSE}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage-Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 5). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method above, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

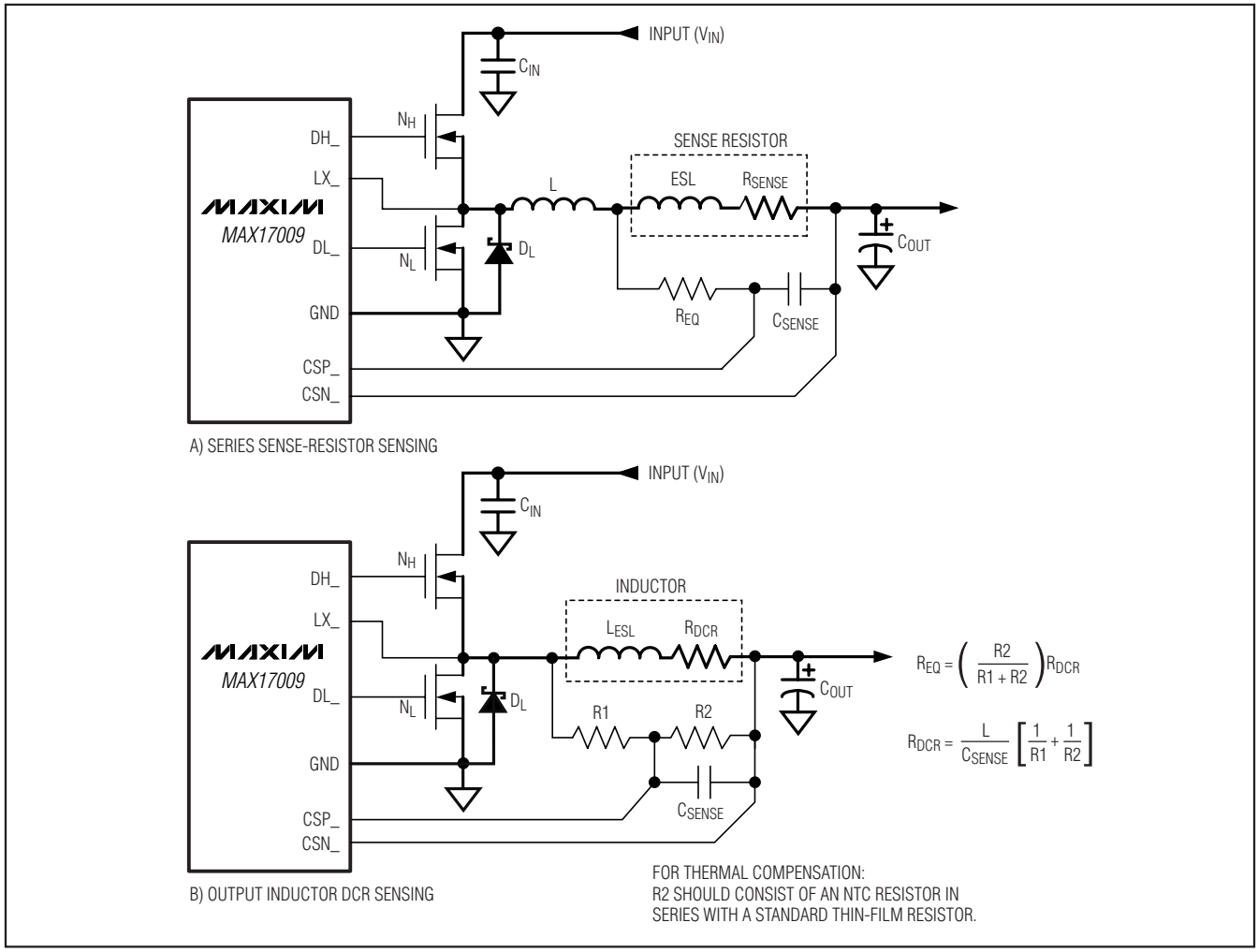

Figure 5. Current-Sense Configurations

$$\frac{L_{ESL}}{R_{SENSE}} = R_{EQ}C_{SENSE}$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, and C_{SENSE} and R_{EQ} are the time-constant matching components.

Combined-Mode Current Balance

When configured in combined mode, the MAX17009 current-mode architecture automatically forces the individual phases to remain current balanced. SMPS1 is the main voltage-control loop, and SMPS2 maintains the current balance between the phases. This control scheme regulates the peak inductor current of each phase, forcing them to remain properly balanced. Therefore, the average inductor current variation depends mainly on the variation in the current-sense element and inductance value.

Peak Current Limit

The MAX17009 current-limit circuit employs a fast peak inductor current-sensing algorithm. Once the current-sense signal (CSP to CSN) of the active phase exceeds the peak current-limit threshold, the PWM controller terminates the on-time. See the *Peak-Inductor Current Limit* section in the *SMPS Design Procedure* section.

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Power-Up Sequence (POR, UVLO, PGD_IN)

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller—V_{CC} above 4.25V and $\overline{SHDN}$ driven high. With the reference in regulation, the controller ramps the SMPS and NBV_BUF voltages to the boot voltage set by the SVC and SVD inputs:

$$t_{(SMPS-START)} = \frac{V_{BOOT}}{(1mV/\mu s)}$$

$$t_{(NBV\_BUF-START)} = \frac{V_{BOOT} R_{TIME} C_{NBV\_BUF}}{(7\mu A \times 143k\Omega)}$$

The soft-start circuitry does not use a variable current limit, so full output current is available immediately. PWRGD becomes high impedance approximately 20µs after the SMPS outputs reach regulation. The boot VID is stored the first time PWRGD goes high. The MAX17009 is in pulse-skipping mode during soft-start, and in forced-PWM mode soft-shutdown.

The NB regulator soft-start time is set by the NB regulator soft-start timer, or by $t_{(NBV\_BUF-START)}$, whichever is longer.

For automatic startup, the battery voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the V_{CC} power supply below 0.5V.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions and could also result in the stored boot VIDs being corrupted. As such, the MAX17009 immediately stops switching (DH_ and DL_ pulled low), latches off, and discharges the outputs using the internal 10Ω switches from CSL_ to GND. See Figure 6.

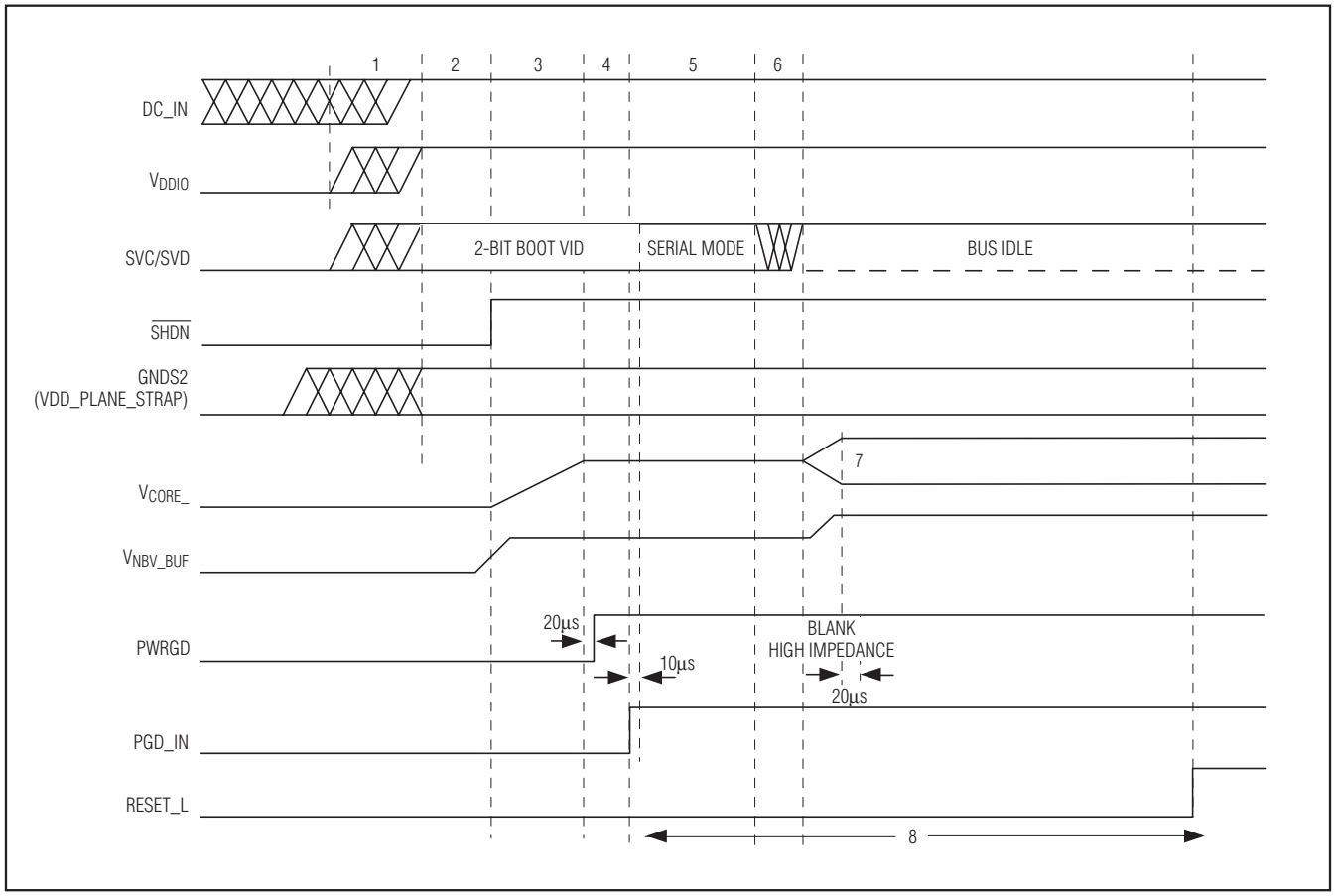

Figure 6. Startup Sequence

Notes:

1) The relationship between DC_IN and V_{DDIO} is not guaranteed. It is possible to have V_{DDIO} powered when DC_IN is not powered, and it is possible to have DC_IN power-up before V_{DDIO} powers up.
2) As the V_{DDIO} power rail comes within specification, VDD_Plane_Strap becomes valid and SVC and SVD are driven to the boot VID value by the processor. The system guarantees that V_{DDIO} is in specification and SVC and SVD are driven to the boot VID value for at least 10µs prior to $\overline{SHDN}$ being asserted to the MAX17009.
3) After $\overline{SHDN}$ is asserted, the MAX17009 samples and latches the VDD_Plane_Strap level at its GNDS2 pin when REF reaches the REFOK threshold, and ramps up the voltage-plane outputs to the level indicated by the 2-bit boot VID. The boot VID is stored in the MAX17009 for use when PGD_IN deasserts. The MAX17009 soft-starts the output rails to limit inrush current from the DC_IN rail.
4) The MAX17009 asserts PWRGD. After PWRGD is asserted and all system-wide voltage planes and free-running clocks are within specification, then the system asserts PGD_IN.
5) The processor holds the 2-bit boot VID for at least 10µs after PGD_IN is asserted.
6) The processor issues the set VID command through SVI.
7) The MAX17009 transitions the voltage planes to the set VID. The set VID may be greater than, or less than the boot VID voltage.
8) The chipset enforces a 1ms delay between PGD_IN assertion and RESET_L deassertion.

PWRGD

The MAX17009 features internal power-good fault comparators for each phase. The outputs of these individual power-good fault comparators are logically ORed to drive the gate of the open-drain PWRGD output transistor. Each phase's power-good fault comparator has an upper threshold of +200mV (typ) and a lower threshold of -300mV (typ). PWRGD goes low if the output of either phase exceeds its respective thresholds.

PWRGD is forced low during the startup sequence up to 20µs after both SMPS internal DACs reach the boot VID. The 2-bit boot VID is stored when PWRGD goes high during the startup sequence. PWRGD is immediately forced low when $\overline{SHDN}$ goes low.

PWRGD is blanked high impedance while either of the internal SMPS DACs are slewing during a VID transition, plus an additional 20µs after the DAC transition is completed. For downward VID transitions, the upper threshold of the power-good fault comparators remains blanked until the output reaches regulation again.

PWRGD goes low for a minimum of 20µs when PGD_IN goes low, and stays low until 20µs after both SMPS internal DACs reach the boot VID.

PGD_IN

After the SMPS outputs reach the boot voltage, the MAX17009 switches over to the serial-interface mode when PGD_IN goes high. Anytime during normal operation, a high-to-low transition on PGD_IN causes the MAX17009 to slew all three internal DACs back to the stored boot VIDs. PWRGD goes low for a minimum of 20µs when PGD_IN goes low, and stays low until 20µs after the SMPS outputs are within the PWRGD thresholds. The SVC and SVD inputs are disabled during the time that PGD_IN is low. The serial interface is reenabled when PGD_IN goes high again.

In debug mode ($\overline{PRO}$ = OPEN), the function of the SVC and SVD inputs depend on the PGD_IN level. If PGD_IN is low, the SVC and SVD inputs are used as 2-bit inputs to set the three internal DAC voltages. See Table 3. If PGD_IN is high, the MAX17009 switches over to serial-interface mode. A high-to-low transition on PGD_IN causes the MAX17009 to slew all three internal DACs back to the stored boot VIDs and revert to the 2-bit VID mode. See Figure 7.

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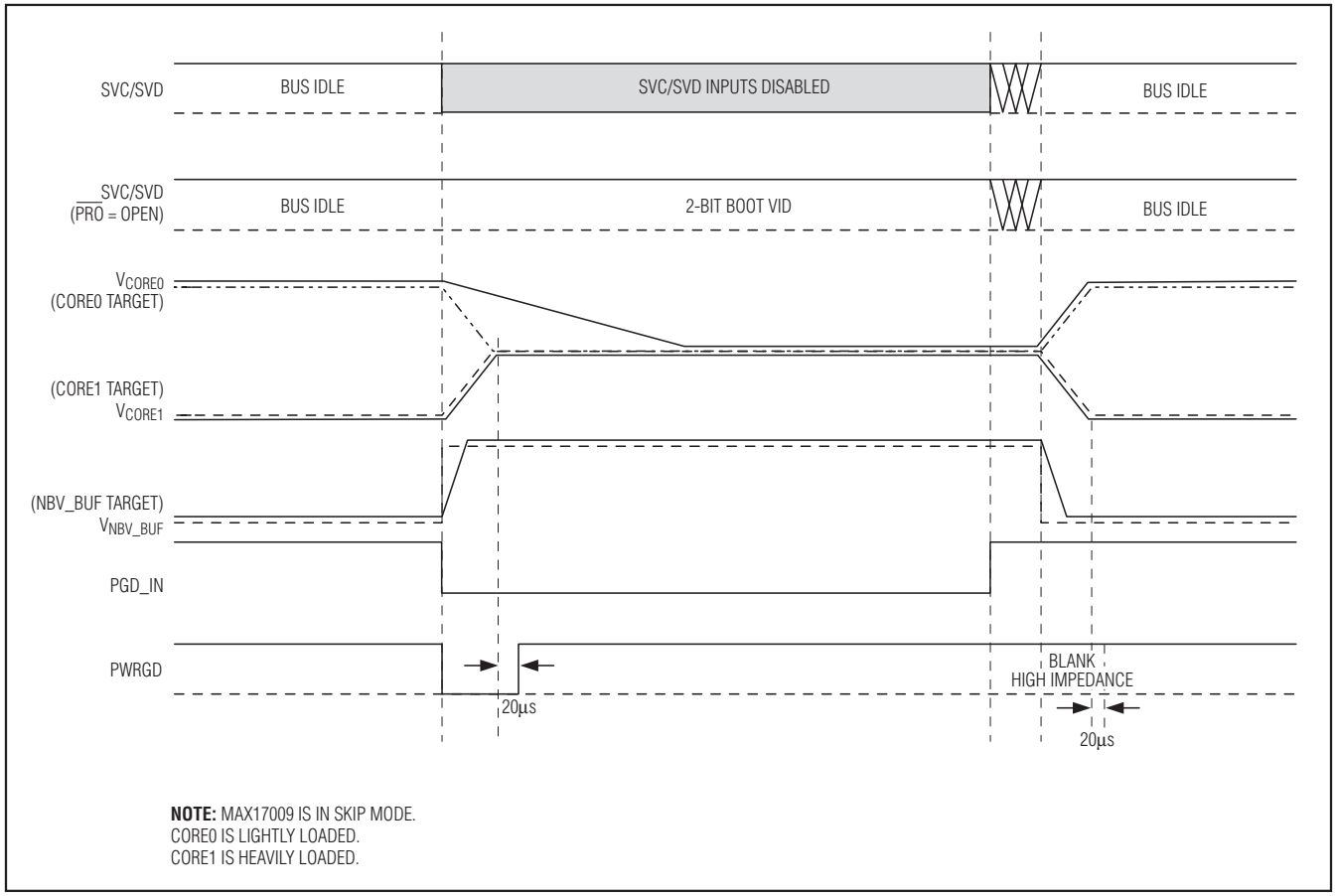

Figure 7. PGD_IN Timing Figure

Shutdown

When $\overline{SHDN}$ goes low, the MAX17009 enters the low-power shutdown mode. PWRGD is pulled low immediately, and the SMPS output voltages ramp down at 1mV/µs, while the NBV_BUF output slews at a rate set by R_{TIME}. At the end of the soft-shutdown sequence, DL_ is kept low, and the 10Ω switches from CSL_ to GND are enabled, holding the outputs low:

$$t_{(SMPS-SHDN)} = \frac{V_{OUT}}{(1mV/\mu s)}$$

$$t_{(NBV\_BUF-SHDN)} = \frac{V_{NBV\_BUF} R_{TIME} C_{NBV\_BUF}}{(7\mu A \times 143k\Omega)}$$

Slowly discharging the output capacitors by slewing the output over a long period of time keeps the average negative inductor current low (damped response), thereby eliminating the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion. The MAX17009 shuts down completely—the drivers are disabled, the reference turns off, and the supply currents drop to about 1µA (max)—20µs after the controller reaches the 0V target. When a fault condition—overvoltage or undervoltage—occurs on one SMPS, the other SMPS and the NBV_BUF immediately go through the soft-shutdown sequence. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle V_{CC} power below 0.5V.

Soft-shutdown for the NB regulator is determined by the particular NB regulator's shutdown behavior. In the typical application, the NB regulator's $\overline{SHDN}$ pin or enable pin is toggled at the same time as the MAX17009's $\overline{SHDN}$ pin.

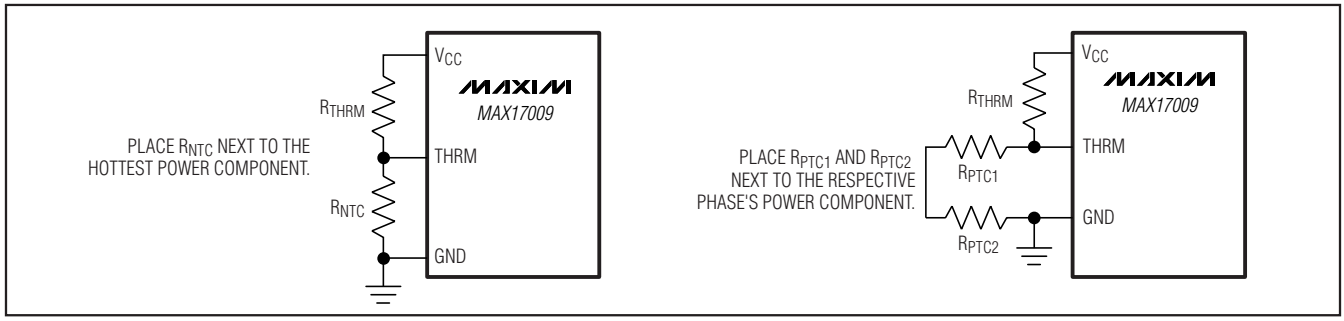

Figure 8. THRM Configuration

$\overline{VRHOT}$ Temperature Comparator

The MAX17009 features an independent comparator with an accurate threshold (V_{HOT}) that tracks the analog supply voltage (V_{HOT} = 0.3 x V_{CC}). Use a resistor- and thermistor-divider between V_{CC} and GND to generate a voltage-regulator overtemperature monitor. Place the thermistor as close to the MOSFETs and inductors as possible.

For combined-mode operations, the current-balance circuit balances the currents between phases. As such, the power loss and heat in each phase should be identical, apart from the effects of placement and airflow over each phase. A single thermistor can be placed near either of the phases and still be effective.

For separate mode operation, the load currents between phases may be very different. Using two "logic-level" thermistors (e.g., Murata PRF series POSITORS) allows the same $\overline{VRHOT}$ comparator to monitor the temperature of both phases. Figure 8 is the THRM configuration.

Fault Protection (Latched)

$\overline{PRO}$ Selectable Overvoltage Protection and Debug Mode

The MAX17009 features a tri-level $\overline{PRO}$ pin that enables the overvoltage protection feature, or puts the MAX17009 in debug mode. Table 5 shows the $\overline{PRO}$-selectable options. Debug mode is intended for applications where the serial interface is not properly functioning, and the output voltage needs to be adjusted to different levels. The DAC voltage settings in debug mode further depend on the PGD_IN level to switch between the 2-bit VID setting or the serial interface operation.

Table 5. $\overline{PRO}$ Settings

$\overline{PRO}$	DESCRIPTION
V_{CC}	OVP disabled
OPEN	Debug mode, OVP disabled
GND	OVP enabled

Output Overvoltage Protection

The overvoltage-protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX17009 continuously monitors the output for an overvoltage fault. The controller detects an OVP fault if the output voltage exceeds the set VID DAC voltage by more than 300mV. The OVP threshold tracks the VID DAC voltage except during a downward VID transition. During a downward VID transition, the OVP threshold is set at 1.80V (min), until the output reaches regulation, when the OVP threshold is reset back to 300mV above the VID setting.

When the OVP circuit detects an overvoltage fault, it immediately forces the external low-side driver high on the faulted side and initiates the soft-shutdown for the other SMPS and the NBV_BUF. The synchronous-rectifier MOSFETs of the faulted side are turned on with 100% duty, which rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

When in combined mode, the synchronous-rectifier MOSFETs of both phases are turned on with 100% duty in response to an overvoltage fault.

Overvoltage protection can be disabled by setting $\overline{PRO}$ to high or open.

Output Undervoltage Protection

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX17009 output voltage is 400mV below the target voltage, the controller activates the shutdown sequence for both SMPS and NBV_BUF, and sets the fault latch. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

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Thermal-Fault Protection

The MAX17009 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch and shuts down, immediately forcing DH and DL low, without going through the soft-shutdown sequence. Toggle SHDN or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH) source and sink 2.2A, and the low-side gate drivers (DL) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH floating high-side MOSFET drivers are powered by internal boost switch charge pumps at BST, while the DL synchronous-rectifier drivers are powered directly by the 5V bias supply (V_{DD}).

Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17009 interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.25Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces may require rising LX edges that do not pull up the low-side MOSFETs’ gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET’s gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Typically, adding a 4700pF between DL and power ground (C_{NL} in Figure 9), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents can be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 9). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

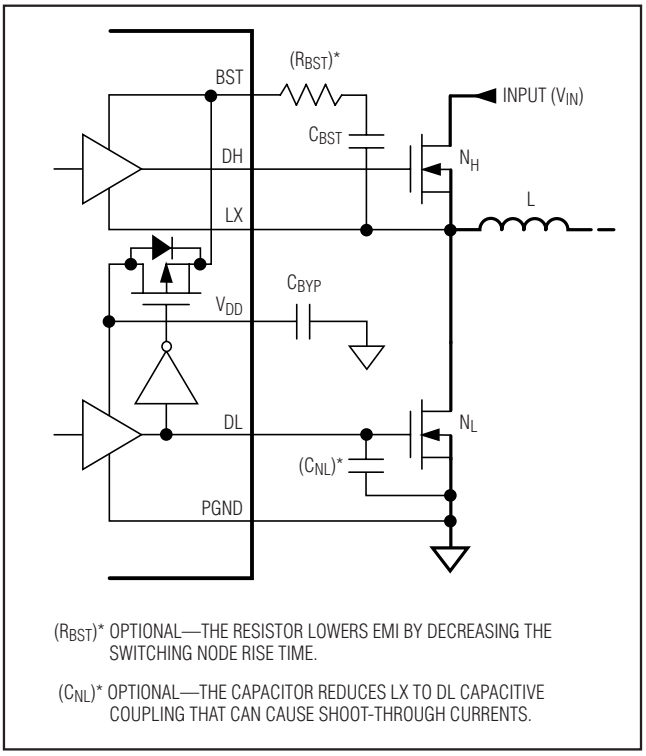

Figure 9. Gate Drive Circuit

Table 6. OPTION Pin Settings

OPTION	OFFSET ENABLED	TRANSIENT-PHASE REPEAT ENABLED
V_{CC}	0	0
OPEN	0	1
REF	1	0
GND	1	1

Offset and Transient-Phase Repeat (OPTION)

The +12.5mV offset and the transient-phase repeat features of the MAX17009 can be selectively enabled and disabled by the OPTION pin setting. Table 6 shows the OPTION pin voltage levels and the features that are enabled. See the *Transient Phase Repeat* section for a detailed description of the respective features. When the offset is enabled, setting the PSI_L bit low disables the offset reducing power consumption in the low-power state.

SMPS Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

  For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{\eta_{PH}}$$

  where η_{PH} is the total number of active phases.
- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

  When selecting a switching frequency, the minimum on-time at the highest input voltage and lowest output voltage must be greater than the 185ns (max) minimum on-time specification in the *Electrical Characteristics* table:

$$V_{OUT(MIN)} / V_{IN(MAX)} \times T_{SW} > t_{ONMIN}$$

  A good rule is to choose a minimum on-time of at least 200ns.

  When in pulse-skipping operation SKIP_ = GND, the minimum on-time must take into consideration the time needed for proper skip-mode operation. The on-time for a skip pulse must be greater than the 185ns (max) minimum on-time specification in the *Electrical Characteristics* table:

$$t_{ONMIN} \le \frac{LV_{IDLE}}{R_{SENSE}\left(V_{IN(MAX)} - V_{OUT(MIN)}\right)}$$

- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

By design, the AMD Mobile Serial VID application should regard each of the MAX17009 SMPSs as independent, single-phase regulators. The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

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$$L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where $I_{LOAD(MAX)}$ is the maximum current per phase, and f_{SW} is the switching frequency per phase.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. If using a swinging inductor (where the inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} L}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{\eta_{PH}}\right) + \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

Peak-Inductor Current Limit (ILIM)

The MAX17009 overcurrent protection employs a peak current-sensing algorithm that uses either current-sense resistors or the inductor's DCR as the current-sense element (see the *Current Sense* section). Since the controller limits the peak inductor current, the maximum average load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and input-to-output voltage difference. When combined with the output undervoltage-protection circuit, the system is effectively protected against excessive overload conditions.

The peak current-limit threshold is set by voltage difference between ILIM and REF using an external resistor-divider:

$$V_{CS(PK)} = V_{CSP\_} - V_{CSN\_} = 0.05 \times (V_{REF} - V_{ILIM})$$

$$I_{LIMIT(PK)} = V_{CS(PK)} / R_{SENSE}$$

where R_{SENSE} is the resistance value of the current-sense element (inductors' DCR or current-sense resistor), and $I_{LIMIT(PK)}$ is the desired peak current limit (per phase). The peak current-limit threshold voltage-adjustment range is from 10mV to 50mV.

Output-Capacitor Selection

The output filter capacitor must have low-enough ESR to meet output ripple and load-transient requirements. In CPU V_{CORE} converters and other applications where the output is subject to large-load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output-ripple voltage (V_{RIPPLE}) by reducing the total inductor ripple current. For nonoverlapping, multiphase operation ($V_{IN} \ge V_{OUT}$), the maximum ESR to meet the output-ripple-voltage requirement is:

$$R_{ESR} \le \left[\frac{V_{IN} f_{SW} L}{(V_{IN} - V_{OUT}) V_{OUT}}\right] V_{RIPPLE}$$

where f_{SW} is the switching frequency per phase. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor selection is usually limited by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

The capacitance value required is determined primarily by the output transient-response requirements. Low inductor values allow the inductor current to slew faster, replenishing charge removed from or added to the output filter capacitors by a sudden load step. Therefore, the amount of output soar when the load is removed is a function of the output voltage and inductor value. The minimum output capacitance required to prevent overshoot (V_{SOAR}) due to stored inductor energy can be calculated as:

$$C_{OUT} \ge \frac{(\Delta I_{LOAD(MAX)})^2 L}{2 V_{OUT} V_{SOAR}}$$

When using low-capacity ceramic-filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem.

Input-Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. For a dual, 180° interleaved controller, the out-of-phase operation reduces the RMS input ripple current, effectively lowering the input capacitance requirements. When both outputs operate with a duty cycle less than 50% (V_{IN} > 2 x V_{OUT}), the RMS input-ripple current is defined by the following equation:

$$I_{RMS} = \sqrt{\left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1}(I_{OUT1} - I_{IN}) + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}(I_{OUT2} - I_{IN})}$$

where I_{IN} is the average input current:

$$I_{IN} = \left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1} + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}$$

In combined mode (GNDS2 = V_{DDIO}) with both phases active, the input RMS current simplifies to:

$$I_{RMS} = I_{OUT} \sqrt{\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{2} - \frac{V_{OUT}}{V_{IN}}\right)}$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX17009 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than 10°C temperature rise at the RMS input current for optimal circuit longevity.

Voltage Positioning and Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power-dissipation requirements. The controller uses two transconductance amplifiers to set the transient and DC output-voltage droop (Figure 3). The transient-compensation (TRC) amplifier determines how quickly the MAX17009 responds to the load transient. The FBDC_ amplifier adjusts the steady-state regulation voltage as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Steady-State Voltage Positioning

Connect a resistor ($R_{FBDC\_}$) between FBDC_ and the remote-sense point to set the steady-state DC droop (load line) based on the required voltage-positioning slope ($R_{DROOPDC}$):

$$R_{FBDC\_} = R_{DROOPDC} / (R_{SENSE\_} \times G_{m(FBDC\_)})$$

where $R_{DROOPDC}$ is the desired steady-state droop, $G_{m(FBDC\_)}$ is typically 1ms as defined in the *Electrical Characteristics* table, and $R_{SENSE\_}$ is the value of the current-sense resistor that is used to provide the (CSP_, CSN_) current-sense voltage.

When the inductors' DCR is used as the current-sense element (R_{SENSE} = R_{DCR}), the inductor DCR circuit should include an NTC thermistor to cancel the temperature dependence of the inductor DCR, maintaining a constant voltage-positioning slope.

Transient Droop

Connect a resistor ($R_{FBAC\_}$) between FBAC_ and the remote-sense point to set the DC transient AC droop (load-line) based on the required voltage-positioning slope ($R_{DROOPAC}$):

$$R_{FBAC\_} = R_{DROOPAC} / (R_{SENSE\_} \times G_{m(FBAC\_)})$$

where $R_{DROOPAC}$ is the desired steady-state droop, $G_{m(FBAC\_)}$ is typically 1mS as defined in the *Electrical Characteristics* table, and $R_{SENSE\_}$ is the value of the current-sense resistor that is used to provide the (CSP_, CSN_) current-sense voltage.

When the inductors' DCR is used as the current-sense element (R_{SENSE} = R_{DCR}), the inductor DCR circuit should include an NTC thermistor to cancel the temperature dependence of the inductor DCR, maintaining a constant voltage-positioning slope.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but with higher C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at

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$V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ to lower C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D^2PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur (see the *MOSFET Gate Drivers* section).

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD(NHResistive) = \left(\frac{V_{OUT}}{V_{IN}}\right) I_{LOAD}^2 R_{DS(ON)}$$

where I_{LOAD} is the per-phase current.

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFET (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(NHSwitching) = \left(V_{IN(MAX)}\right)^2 \left(\frac{C_{RSS} f_{SW}}{I_{GATE}}\right) I_{LOAD}$$

where C_{RSS} is the reverse transfer capacitance of N_H and I_{GATE} is the peak gate-drive source/sink current (1A typ), and I_{LOAD} is the per-phase current.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the C x V_{IN}^2 x f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low-battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD(NLResistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right] \left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "overdesign" the circuit to tolerate:

$$I_{LOAD(MAX)} = I_{PEAK(MAX)} - \frac{\Delta I_{INDUCTOR}}{2}$$

$$= I_{PEAK(MAX)} - \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{PEAK(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good-size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current per phase. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

SVI Applications Information

I²C-Bus-Compatible Interface

The MAX17009 is a receive-only device. The 2-wire serial bus (pins SVC and SVD) is designed to attach on a low-voltage, I²C-like bus. In the AMD mobile application, the CPU directly drives the bus at a speed of 3.4MHz. The CPU has a push-pull output driving to the V_{DDIO} voltage level. External pullup resistors may be required during the initial power-up sequence before the CPU's push-pull drivers are active. Refer to AMD for specific implementation.

When not used in the specific AMD application, the serial interface can be driven to as high as 2.5V, and operate at the lower speeds (100kHz, 400kHz, or 1.7MHz). At lower clock speeds, external pullup resistors can be used for open-drain outputs. Connect both SVC and SVD lines to V_{DDIO} through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \le \frac{t_R}{C_{BUS}}$$

where t_R is the rise time, and should be less than 10% of the clock period. C_{BUS} is the total capacitance on the bus.

The MAX17009 is compatible with the standard SVI interface protocol as defined in the following subsections.

Bus Not Busy

The SVI bus is not busy when both data and clock lines remain HIGH. Data transfers can be initiated only when the bus is not busy.

Start Data Transfer (S)

Starting from an idle bus state (both SVC and SVD are high), a HIGH to LOW transition of the data (SVD) line while the clock (SVC) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (P)

A LOW to HIGH transition of the SDA line while the clock (SVC) is HIGH determines a STOP condition. All operations must be ended with a STOP condition. Figure 10 shows the SVI bus START, STOP, and data change conditions

Slave Address

After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (110xxxx) for the MAX17009. Since the MAX17009 is a write-only device, the eighth bit of the slave address is zero. The MAX17009 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

SVD Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

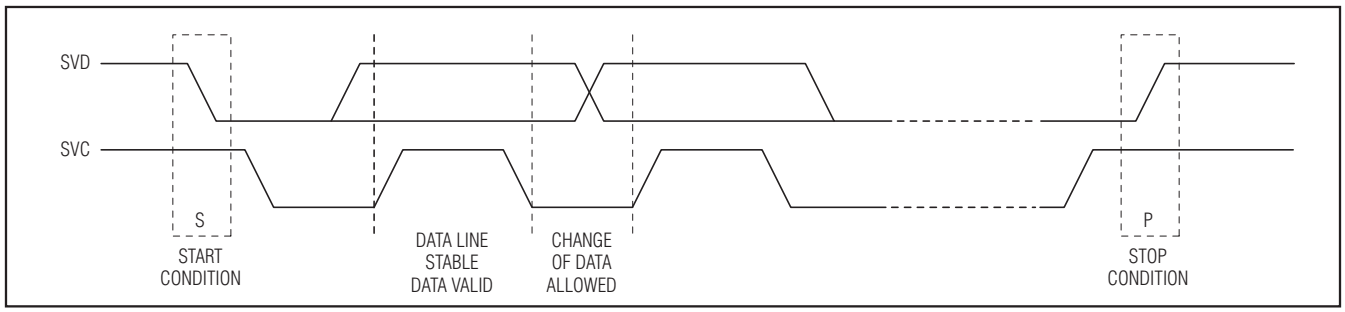

Figure 10. SVI Bus START, STOP, and Data Change Conditions

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Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. The device that acknowledges has to pull down the SVD line during the acknowledge clock pulse so the SVD line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. See Figure 11. Figure 12 shows the SVI bus data transfer summary.

Command Byte

A complete command consists of a START condition (S) followed by the MAX17009's slave address and a data phase, followed by a STOP condition (P).

SMPS Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by stability requirements, not the minimum off-time ($t_{OFF(MIN)}$). The MAX17009 does not include slope compensation, so the controller becomes unstable with duty cycles greater than 50% per phase:

$$V_{IN(MIN)} \geq 2 \times V_{OUT(MAX)}$$

However, the controller can briefly operate with duty cycles over 50% during heavy load transients.

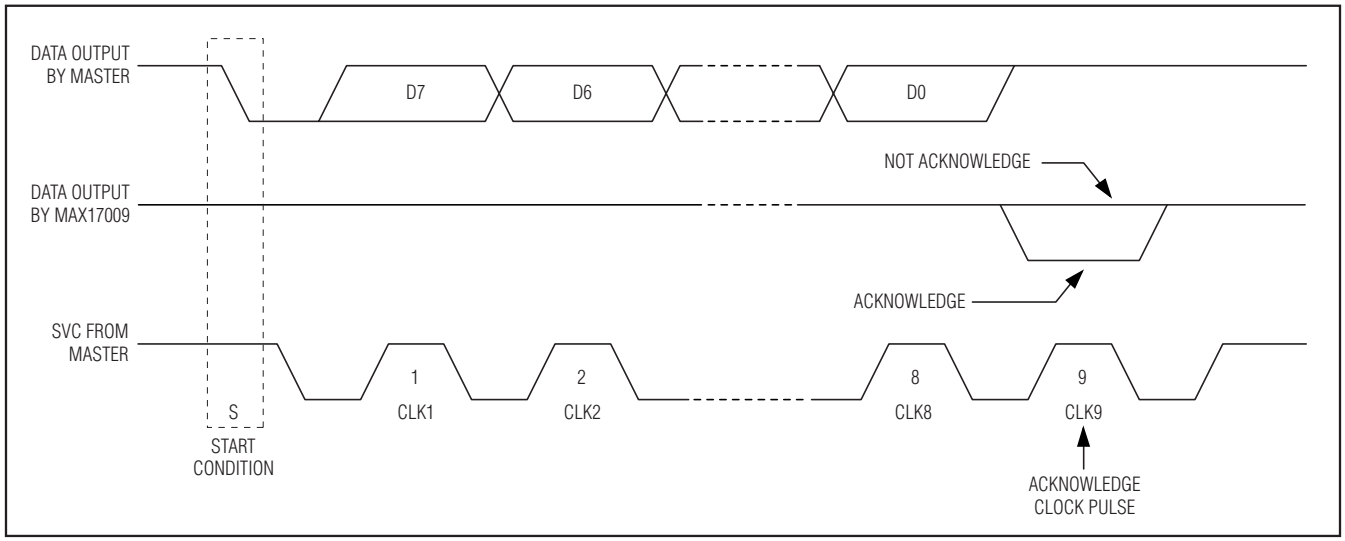

Figure 11. SVI Bus Acknowledge

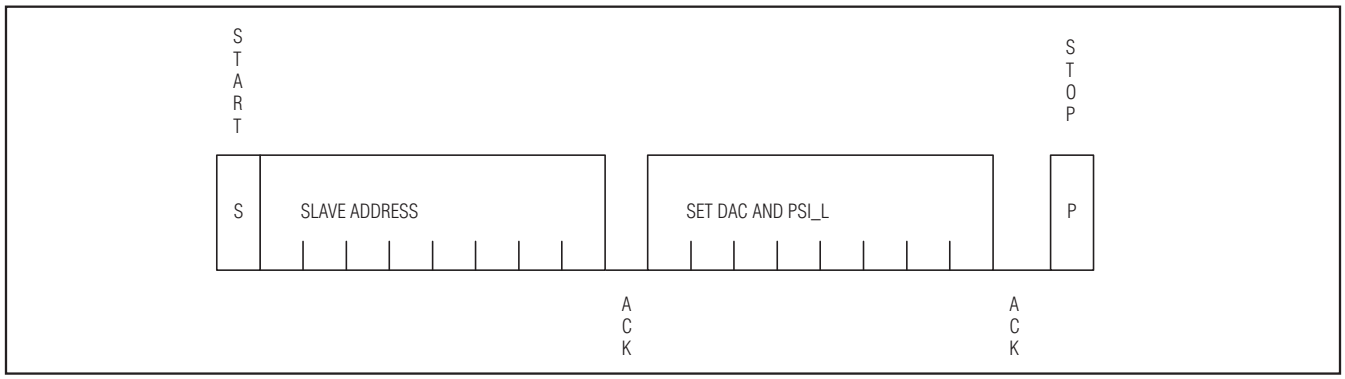

Figure 12. SVI Bus Data Transfer Summary

Table 7. SVI Send Byte Address Description

BITS	DESCRIPTION
6:4	Always 110b
3	X = don't care
2	V_{DAC2}, if set, then the following data byte contains the VID for V_{DAC2}; bit 2 is ignored in combined mode (GNDS2 = V_{DDIO})
1	V_{DAC1}, if set, then the following data byte contains the VID for V_{DAC1} in separate mode, and the unified VDD in combined mode
0	V_{DAC_NB}, if set then the following data byte contains the VID for V_{DAC_NB}

Table 8. Serial VID 8-Bit Data Field Encoding

BITS	DESCRIPTION
7	PSI_L: Power-Save Indicator: • 0 means the processor is at an optimal load and the regulator(s) can enter power-saving mode. Offset is disabled if previously enabled through the OPTION pin. The MAX17009 enters 1-phase operation if in combined mode (GNDS2 = H). • 1 means the processor is at a high current-consumption state. Offset is enabled if previously enabled through the OPTION pin. The MAX17009 returns to 2-phase operation if in combined mode (GNDS2 = H).
6:0	SVID[6:0] as defined in Table 7.

Maximum Input Voltage

The MAX17009 controller has a minimum on-time, which determines the maximum input operating voltage that maintains the selected switching frequency. With higher input voltages, each pulse delivers more energy than the output is sourcing to the load. At the beginning of each cycle, if the output voltage is still above the feedback threshold voltage, the controller does not trigger an on-time pulse, resulting in pulse-skipping operation. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT}\left(\frac{1}{f_{SW}t_{ONMIN}}\right)$$

where f_{SW} is the per-phase switching frequency set by the OSC resistor, and t_{ONMIN} is 185ns (max) minus the driver's turn-on delay (DL low to DH high). For the best high-voltage performance, use the slowest switching frequency setting (100kHz per phase, R_{OSC} = 432kΩ).

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 13). If possible, mount all the power components on the top side of the board with their ground terminals flush against one another, and mount the controller and analog components on the bottom layer so the internal ground layers shield the analog components from any noise generated by the power components. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid copper plane, then connect the analog ground to the GND pins of the controller. The following sensitive components connect to analog ground: V_{CC}, V_{DDIO}, and REF bypass capacitors, remote-sense and GNDS bypass capacitors, and the resistive connections (ILIM, OSC, TIME).
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- Connections for current limiting (CSP_, CSN_) and voltage positioning (FBS, GNDS) must be made using Kelvin-sense connections to guarantee the current-sense accuracy. Place current-sense filter capacitors and voltage-positioning filter capacitors as close to the IC as possible.
- Route high-speed switching nodes and driver traces away from sensitive analog areas (REF, V_{CC}, FBAC, FBDC, etc.). Make all pin-strap control input connections ($\overline{SHDN}$, PGD_IN, OPTION) to analog ground or V_{CC} rather than power ground or V_{DD}.
- Route the high-speed serial-interface signals (SVC, SVD) in parallel, keeping the trace lengths identical. Keep the SVC and SVD away from the high-current switching paths.

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- Keep the drivers close to the MOSFET, with the gate-drive traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and DL anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the driver IC adjacent to the low-side MOSFETs. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the driver IC).
3) Group the gate-drive components (BST capacitors, V_{DD} bypass capacitor) together near the driver IC.
4) Make the DC-DC controller ground connections as shown in the standard application circuit in Figure 2. This diagram can be viewed as having three separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin, V_{DD} bypass capacitor, and driver IC ground connection go; and the controller's analog ground plane where sensitive analog components, the master's GND pin, and V_{CC} bypass capacitor go. The controller's analog ground plane (GND) must meet the power ground plane (PGND) only at a single point directly beneath the IC. The power ground plane should connect to the high-power output ground with a short, thick metal trace from PGND to the source of the low-side MOSFETs (the middle of the star ground).
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output-filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical. Figure 13 is a PCB layout example.

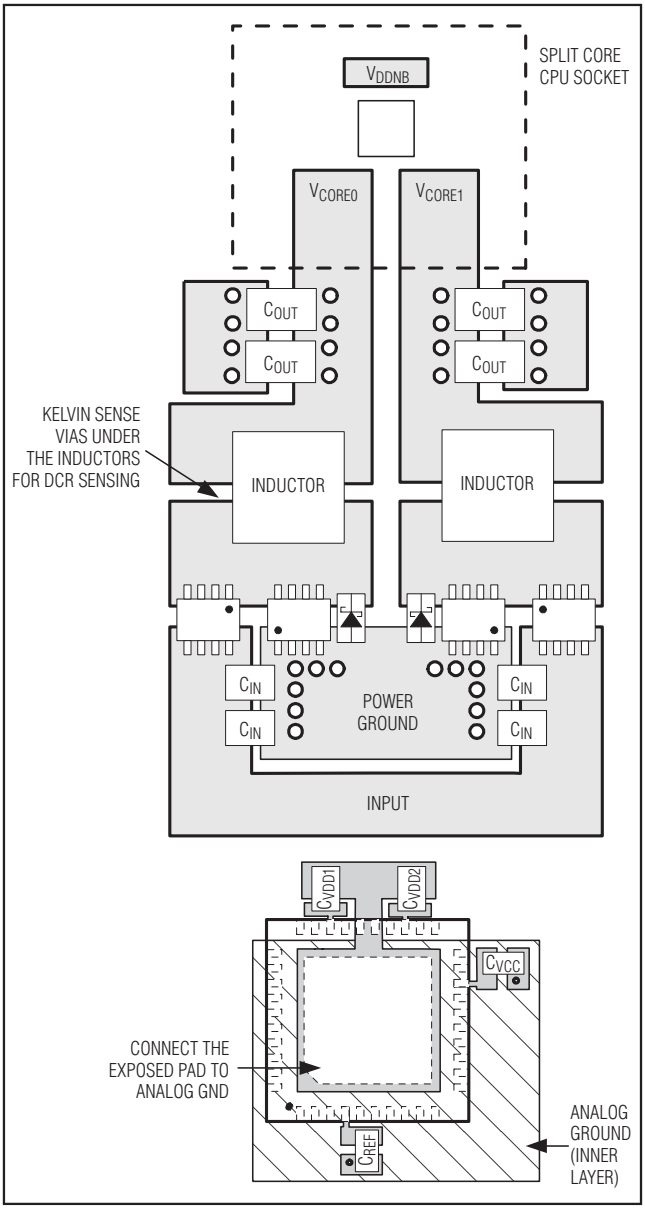
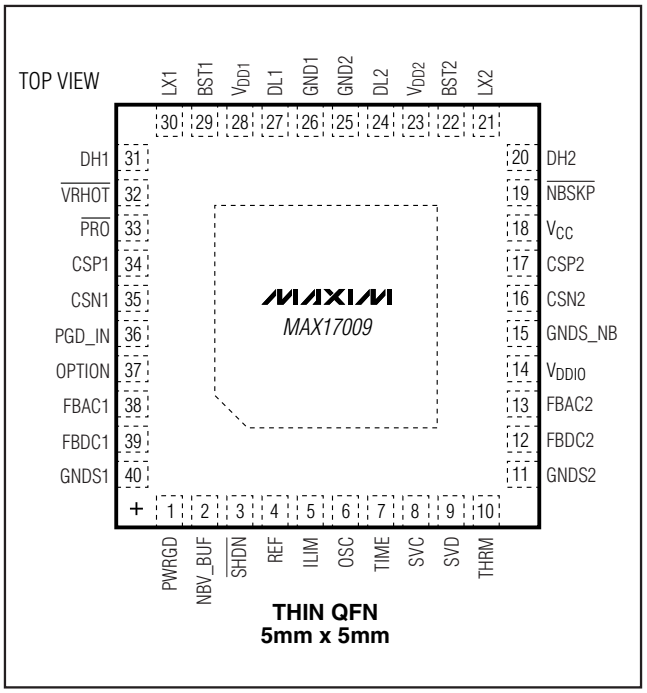


Figure 13. PCB Layout Example

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Pin Configuration



Chip Information

TRANSISTOR COUNT: 14,497

PROCESS: BiCMOS

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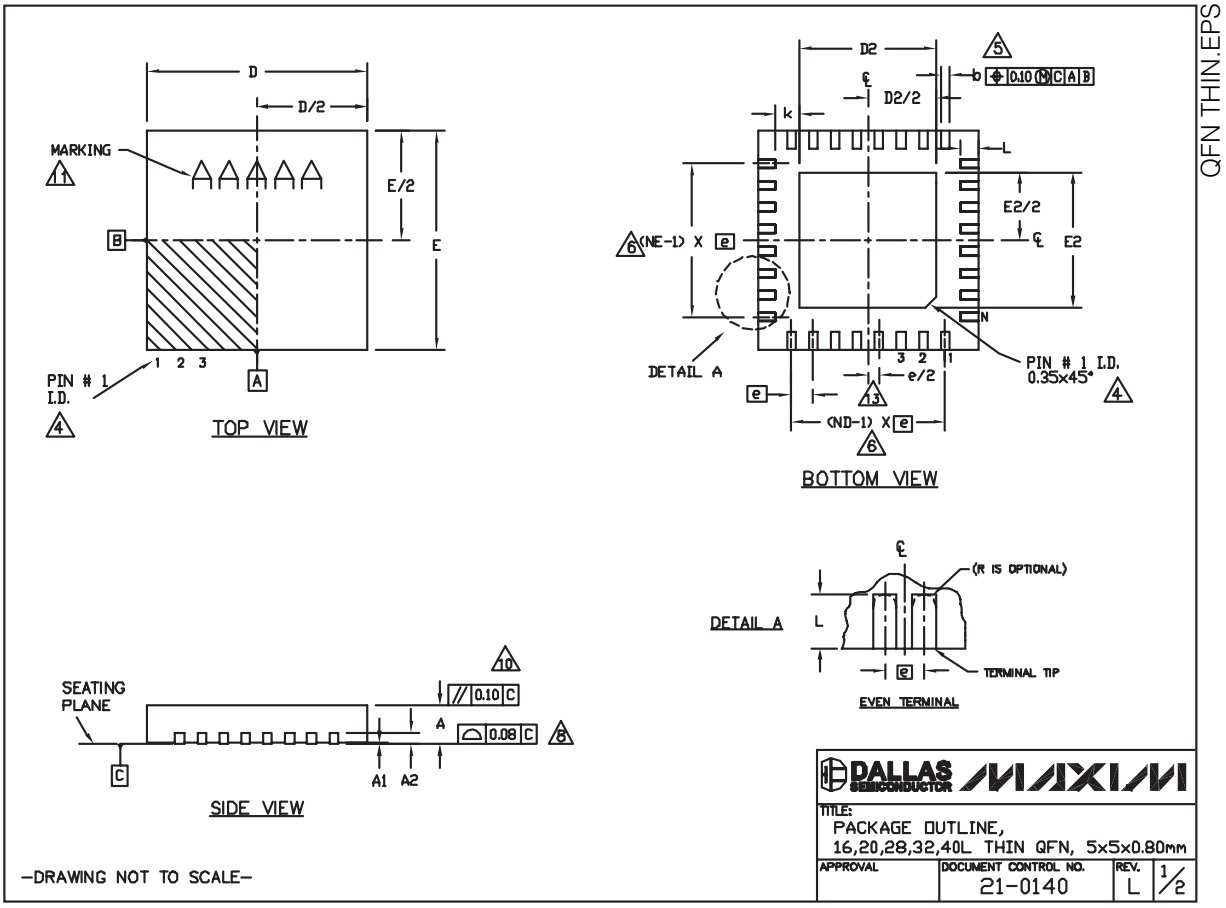
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	L	2/2