

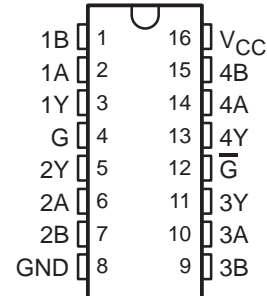
# AM26LV32

## LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202D – MAY 1995 – REVISED APRIL 2000

- Switching Rates up to 32 MHz
- Operates from a Single 3.3-V Supply
- Ultra-Low Power Dissipation . . . 27 mW Typ
- Open-Circuit, Short-Circuit, and Terminated Fail-Safe
- –0.3-V to 5.5-V Common-Mode Range With  $\pm 200$  mV Sensitivity
- Accepts 5-V Logic Inputs With a 3.3-V  $V_{CC}$
- Input Hysteresis . . . 50 mV Typ
- 235 mW With Four Receivers at 32 MHz
- Pin-to-Pin Compatible With AM26C32, AM26LS32, and MB570

D OR NS† PACKAGE  
(TOP VIEW)



† The NS package is only available left-ended taped and reeled.

### description

The AM26LV32, BiCMOS, quadruple, differential line receiver with 3-state outputs is designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 receivers with reduced common-mode voltage range due to reduced supply voltage.

The device is optimized for balanced bus transmission at switching rates up to 32 MHz. The enable function is common to all four receivers and offers a choice of active-high or active-low inputs. The 3-state outputs permit connection directly to a bus-organized system. Each device features receiver high input impedance and input hysteresis for increased noise immunity, and input sensitivity of  $\pm 200$  mV over a common-mode input voltage range from –0.3 V to 5.5 V. When the inputs are open circuited, the outputs are in the high logic state. This device is designed using the Texas Instruments (TI™) proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed.

This device offers optimum performance when used with the AM26LV31 quadruple line drivers.

The AM26LV32C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
	G	$\bar{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2$ V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
Open, shorted, or terminated‡	H	X	H
	X	L	H
X	L	H	Z

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off), ? = indeterminate  
‡ See application information attached.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

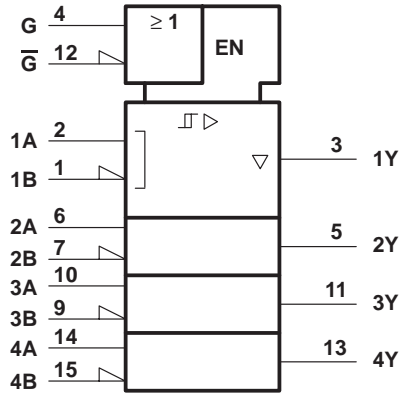
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AM26LV32

LOW-VOLTAGE HIGH-SPEED  
QUADRUPLE DIFFERENTIAL LINE RECEIVER

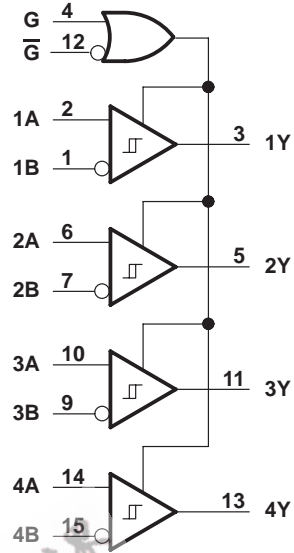
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logic symbol†

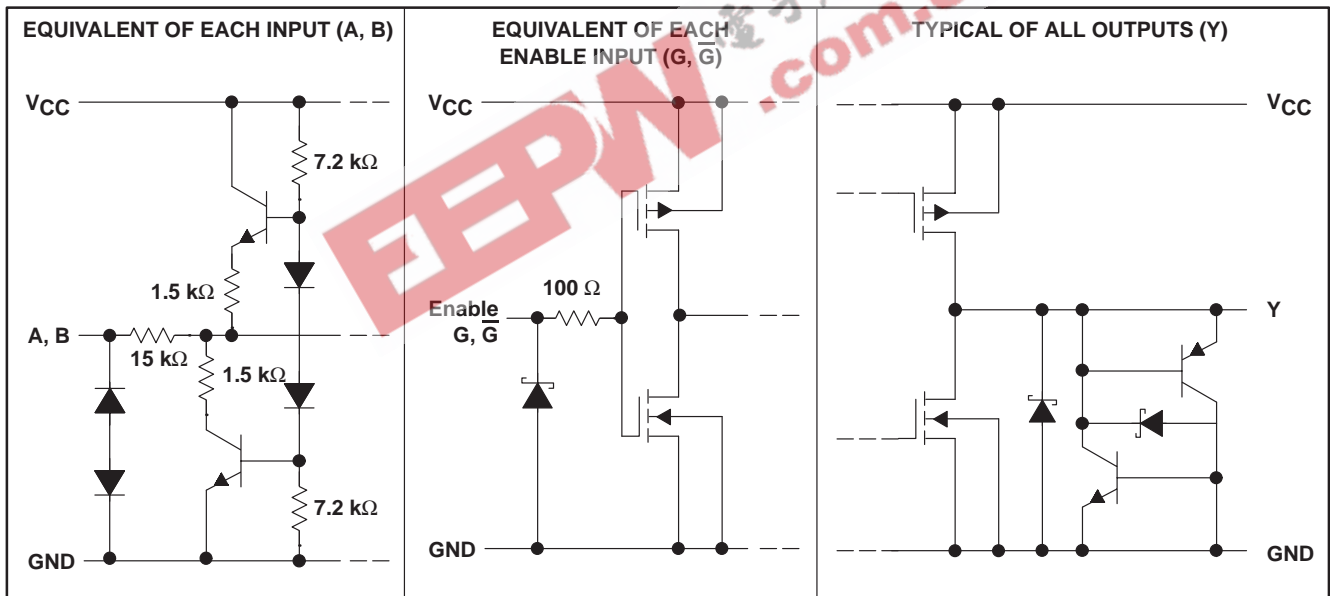


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of equivalent inputs and outputs



**AM26LV32**  
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SLLS202D – MAY 1995 – REVISED APRIL 2000

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Input voltage range, $V_I$ (A or B inputs)	–4 V to 8 V
Differential input voltage, $V_{ID}$ (see Note 2)	±12 V
Enable input voltage range	–0.3 V to 6 V
Output voltage range, $V_O$	–0.3 V to 6 V
Maximum output current, $I_O$	±25 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	73°C/W
NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the GND terminal.  
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions**

	MIN	NOM	MAX	UNIT	
Supply voltage, $V_{CC}$	3	3.3	3.6	V	
High-level input voltage, $V_{IH}(EN)$	2			V	
Low-level input voltage, $V_{IL}(EN)$			0.8	V	
Common-mode input voltage, $V_{IC}$	–0.3		5.5	V	
Differential input voltage, $V_{ID}$			±5.8		
High-level output current, $I_{OH}$			–5	mA	
Low-level output current, $I_{OL}$			5	mA	
Operating free-air temperature, $T_A$		AM26LV32C	0	70	°C

LOW-VOLTAGE HIGH-SPEED  
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202D – MAY 1995 – REVISED APRIL 2000

electrical characteristics over recommended supply-voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IT+</sub> Differential input high-threshold voltage				0.2	V
V <sub>IT-</sub> Differential input low-threshold voltage		-0.2			V
V <sub>IK</sub> Enable input clamp voltage	I <sub>I</sub> = -18 mA		-0.8	-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 200 mV, I <sub>OH</sub> = -5 mA	2.4	3.2		V
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -200 mV, I <sub>OL</sub> = 5 mA		0.17	0.5	V
I <sub>OZ</sub> High-impedance-state output current	V <sub>O</sub> = 0 to V <sub>CC</sub>			±50	µA
I <sub>IH(E)</sub> High-level enable input current	V <sub>CC</sub> = 0 or 3 V, V <sub>I</sub> = 5.5 V			10	µA
I <sub>IL(E)</sub> Low-level enable input current	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 V			-10	
r <sub>I</sub> Input resistance		7	12		kΩ
I <sub>I</sub> Input current	V <sub>I</sub> = 5.5 V or -0.3 V, All other inputs GND			±700	µA
I <sub>CC</sub> Supply current	V <sub>I(E)</sub> = V <sub>CC</sub> or GND, No load, line inputs open		8	17	mA
C <sub>pd</sub> Power dissipation capacitance‡	One channel		150		pF

† All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C.

‡ C<sub>pd</sub> determines the no-load dynamic current: I<sub>S</sub> = C<sub>pd</sub> × V<sub>CC</sub> × f + I<sub>CC</sub>.

switching characteristics, V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C

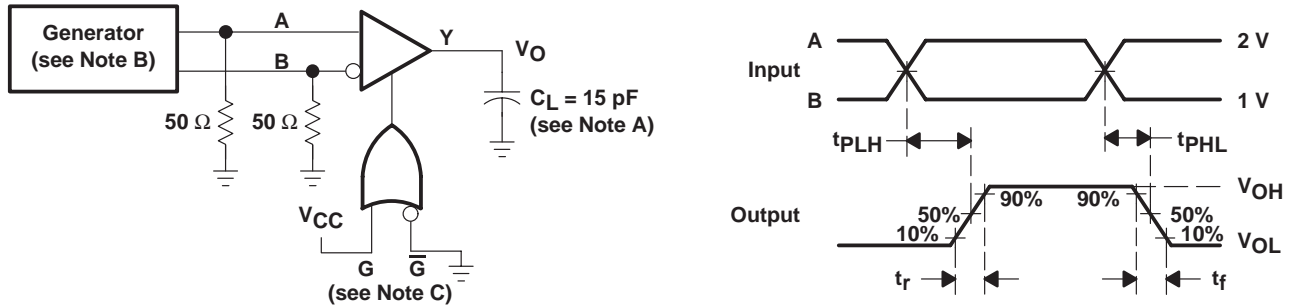
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low- to high-level output	See Figure 1	8	16	20	ns
t <sub>PHL</sub> Propagation delay time, high- to low-level output		8	16	20	ns
t <sub>t</sub> Transistion time (t <sub>r</sub> or t <sub>f</sub> )	See Figure 1		5		ns
t <sub>PZH</sub> Output-enable time to high level	See Figure 2		17	40	ns
t <sub>PZL</sub> Output-enable time to low level	See Figure 3		10	40	ns
t <sub>PHZ</sub> Output-disable time from high level	See Figure 2		20	40	ns
t <sub>PLZ</sub> Output-disable time from low level	See Figure 3		16	40	ns
t <sub>sk(p)</sub> § Pulse skew			4	6	ns
t <sub>sk(o)</sub> ¶ Pulse skew			4	6	ns
t <sub>sk(pp)</sub> # Pulse skew (device to device)			6	9	ns

§ t<sub>sk(p)</sub> is |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

¶ t<sub>sk(o)</sub> is the maximum difference in propagation delay times between any two channels of the same device switching in the same direction.

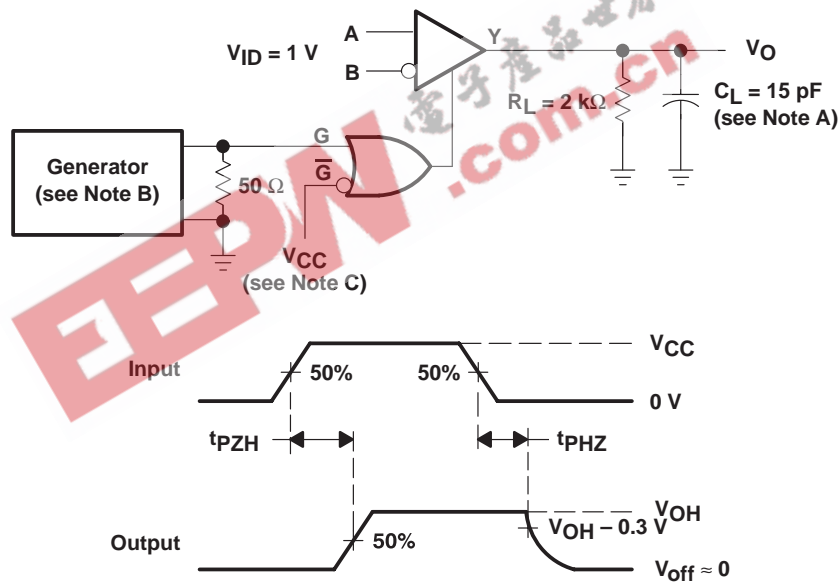
# t<sub>sk(pp)</sub> is the maximum difference in propagation delay times between any two channels of any two devices switching in the same direction.

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $Z_O = 50 \Omega$ , PRR = 10 MHz,  $t_r$  and  $t_f$  (10% to 90%)  $\leq 2$  ns, 50% duty cycle.  
 C. To test the active-low enable  $\bar{G}$ , ground G and apply an inverted waveform  $\bar{G}$ .

**Figure 1.  $t_{PLH}$  and  $t_{PHL}$  Test Circuit and Voltage Waveforms**



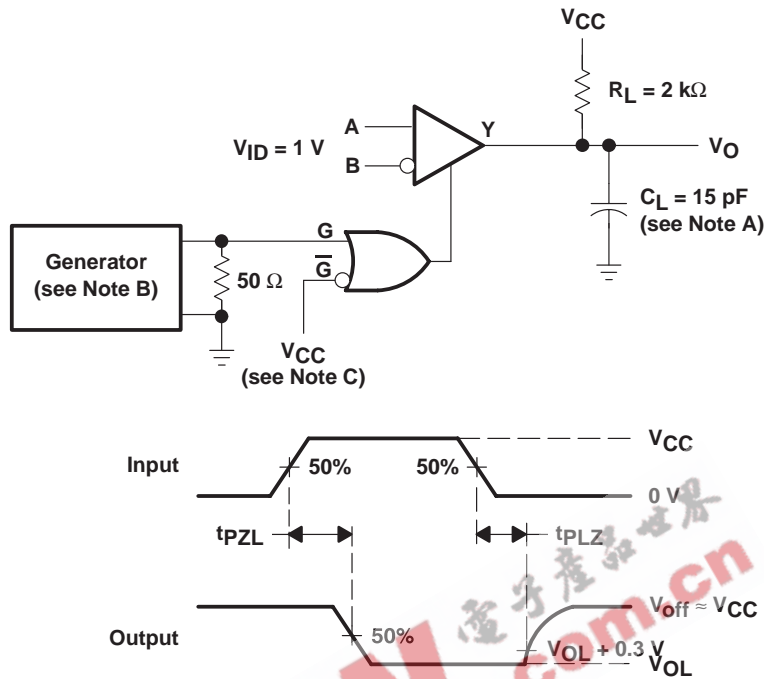
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $Z_O = 50 \Omega$ , PRR = 10 MHz,  $t_r$  and  $t_f$  (10% to 90%)  $\leq 2$  ns, 50% duty cycle.  
 C. To test the active-low enable  $\bar{G}$ , ground G and apply an inverted waveform  $\bar{G}$ .

**Figure 2.  $t_{PZH}$  and  $t_{PHZ}$  Test Circuit and Voltage Waveforms**

LOW-VOLTAGE HIGH-SPEED  
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202D – MAY 1995 – REVISED APRIL 2000

PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $Z_O = 50\ \Omega$ , PRR = 10 MHz,  $t_r$  and  $t_f$  (10% to 90%)  $\leq 2\text{ ns}$ , 50% duty cycle.  
 C. To test the active-low enable  $\bar{G}$ , ground  $\bar{G}$  and apply an inverted waveform  $\bar{G}$ .

Figure 3.  $t_{PZL}$  and  $t_{PLZ}$  Test Circuit and Voltage Waveforms

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## APPLICATION INFORMATION

### fail-safe conditions

The AM26LV32 quadruple differential line receiver is designed to function properly when appropriately connected to active drivers. Applications do not always have ideal situations where all bits are being used, the receiver inputs are never left floating, and fault conditions don't exist. In actuality, most applications have the capability to either place the drivers in a high-impedance mode or power down the drivers altogether, and cables may be purposely (or inadvertently) disconnected, both of which lead to floating receiver inputs. Furthermore, even though measures are taken to avoid fault conditions like a short between the differential signals, this does occur. The AM26LV32 has an internal fail-safe circuitry which prevents the device from putting an unknown voltage signal at the receiver outputs. In the following three cases, a high-state is produced at the respective output:

1. Open fail-safe – Unused input pins are left open. Do not tie unused pins to ground or any other voltage. Internal circuitry places the output in the high state.
2. 100-ohm terminated fail-safe – Disconnected cables, drivers in high-impedance state, or powered-down drivers will not cause the AM26LV32 to malfunction. The outputs will remain in a high state under these conditions. When the drivers are either turned-off or placed into the high-impedance state, the receiver input may still be able to pick up noise due to the cable acting as an antenna. To avoid having a large differential voltage being generated, the use of twisted-pair cable will induce the noise as a common-mode signal and will be rejected.
3. Shorted fail-safe – Fault conditions that short the differential input pairs together will not cause incorrect data at the outputs. A differential voltage ( $V_{ID}$ ) of 0 V will force a high state at the outputs. Shorted fail-safe, however, is not supported across the recommended common-mode input voltage ( $V_{IC}$ ) range. An unwanted state can be induced to all outputs when an input is shorted and is biased with a voltage between  $-0.3$  V and 5.5 V. The shorted fail-safe circuitry will function properly when an input is shorted, but with no external common-mode voltage applied.

### fail-safe precautions

The internal fail-safe circuitry was designed such that the input common-mode ( $V_{IC}$ ) and differential ( $V_{ID}$ ) voltages must be observed. In order to ensure the outputs of unused or inactive receivers remain in a high state when the inputs are open-circuited, shorted, or terminated, extra precaution must be taken on the active signal. In applications where the drivers are placed in a high-impedance mode or are powered-down, it is recommended that for 1, 2, or 3 active receiver inputs, the low-level input voltage ( $V_{IL}$ ) should be greater than 0.4 V. As in all data transmission applications, it is necessary to provide a return ground path between the two remote grounds (driver and receiver ground references) to avoid ground differences. Table 1 and Figures 4 through 7 are examples of active input voltages with their respective waveforms and the effect each have on unused or inactive outputs. Note that the active receivers behave as expected, regardless of the input levels.

LOW-VOLTAGE HIGH-SPEED  
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202D – MAY 1995 – REVISED APRIL 2000

APPLICATION INFORMATION

Table 1. Active Receiver Inputs vs Outputs

1, 2, OR 3 ACTIVE INPUTS			SEE FIGURE	1, 2, OR 3 ACTIVE OUTPUTS	3, 2, OR 1 UNUSED OR INACTIVE OUTPUTS
$V_{IL}^\dagger$	$V_{ID}$	$V_{IC}^\dagger$			
900 mV	200 mV	1 V	4	Known state	High state
-100 mV	200 mV	0 V	5	Known state	?
600 mV	800 mV	1 V	6	Known state	High state
0	800 mV	400 mV	7	Known state	?

$^\dagger$  Measured with respect to ground.

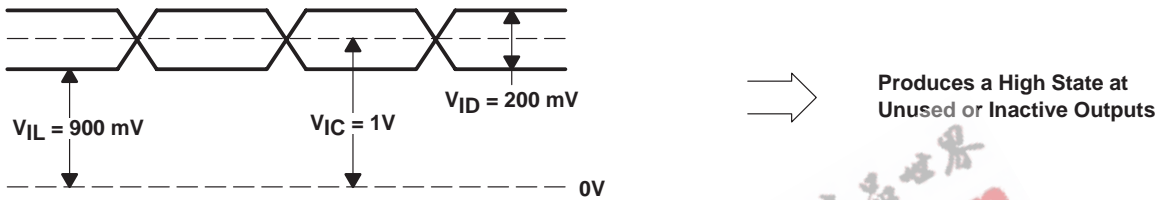


Figure 4. Waveform One

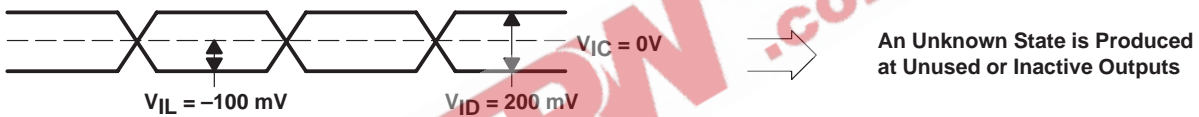


Figure 5. Waveform Two

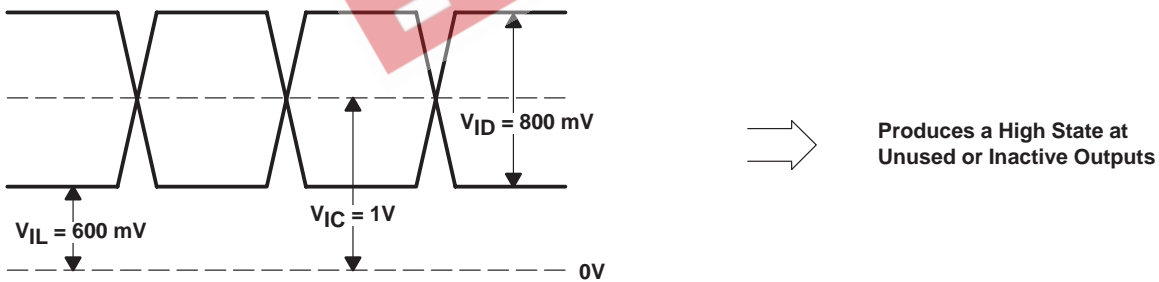


Figure 6. Waveform Three

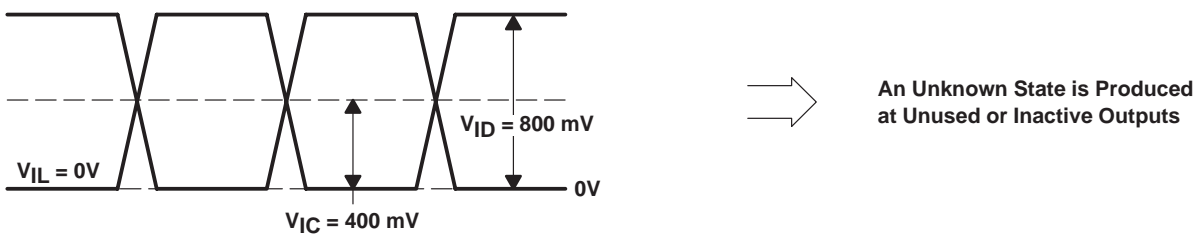


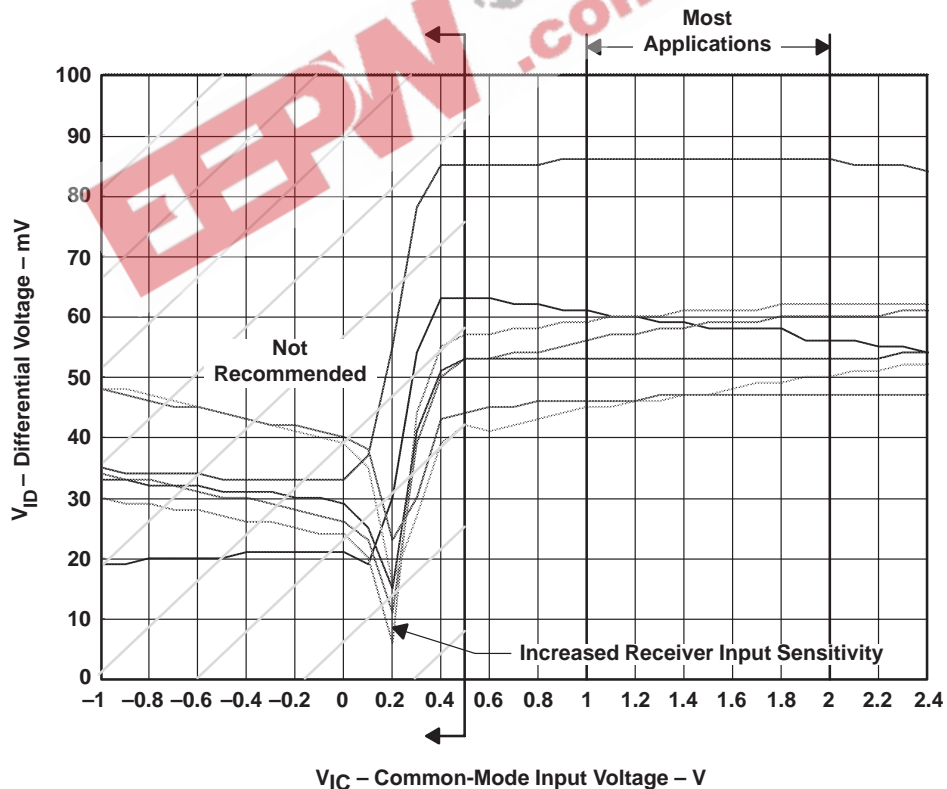
Figure 7. Waveform Four



**APPLICATION INFORMATION**

In most applications, it is not customary to have a common-mode input close to ground and to have a differential voltage larger than 2 V. Since the common-mode input voltage is typically around 1.5 V, a 2-V  $V_{ID}$  would result in a  $V_{IL}$  of 0.5 V, thus satisfying the recommended  $V_{IL}$  level of greater than 0.4 V.

Figure 8 plots seven different input threshold curves from a variety of production lots and shows how the fail-safe circuitry behaves with the input common-mode voltage levels. These input threshold curves are representative samples of production devices. The curves specifically illustrate a typical range of input threshold variation. The AM26LV32 is specified with  $\pm 200$  mV of input sensitivity to account for the variance in input threshold. Each data point represents the input's ability to produce a known state at the output for a given  $V_{IC}$  and  $V_{ID}$ . Applying a differential voltage at or above a certain point on a curve would produce a known state at the output. Applying a differential voltage less than a certain point on a curve would activate the fail-safe circuit and the output would be in a high state. For example, inspecting the top input threshold curve reveals that for a  $V_{IC} = 1.6$  V,  $V_{ID}$  yields around 87 mV. Applying 90 mV of differential voltage to this particular production lot generates a known receiver output voltage. Applying a  $V_{ID}$  of 80 mV activates the input fail-safe circuitry and the receiver output is placed in the high state. Texas Instruments specifies the input threshold at  $\pm 200$  mV, since normal process variations affect this parameter. Note that at common-mode input voltages around 0.2 V, the input differential voltages are low compared to their respective data points. This phenomenon points to the fact that the inputs are very sensitive to small differential voltages around 0.2 V  $V_{IC}$ . It is recommended that  $V_{IC}$  levels be kept greater than 0.5 V to avoid this increased sensitivity at  $V_{IC} \approx 0.2$  V. In most applications, since  $V_{IC}$  typically is 1.5 V, the fail-safe circuitry functions properly to provide a high state at the receiver output.



**Figure 8.  $V_{IC}$  Versus  $V_{ID}$  Receiver Sensitivity Levels**

LOW-VOLTAGE HIGH-SPEED  
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202D – MAY 1995 – REVISED APRIL 2000

APPLICATION INFORMATION

Figure 9 represents a typical application where two receivers are not used. In this case, there is no need to worry about the output voltages of the unused receivers since they are not connected in the system architecture.

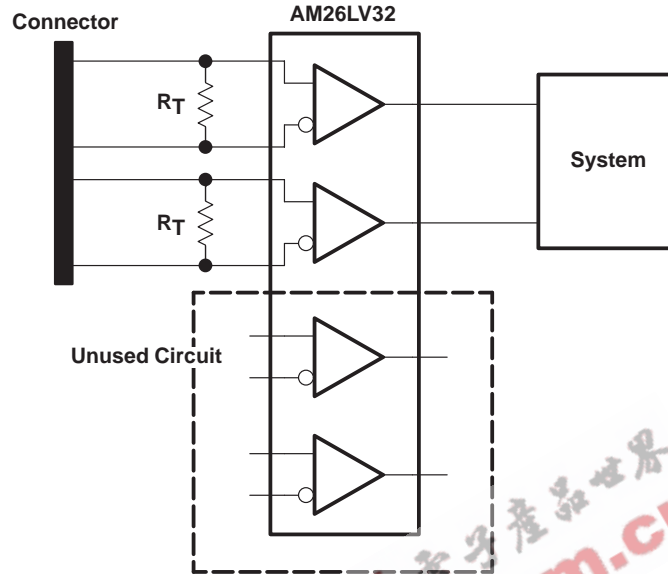


Figure 9. Typical Application with Unused Receivers

Figure 10 shows a common application where one or more drivers are either disabled or powered down. To ensure the inactive receiver outputs are in a high state, the active receiver inputs must have  $V_{IL} > 0.4\text{ V}$  and  $V_{IC} > 0.5\text{ V}$ .

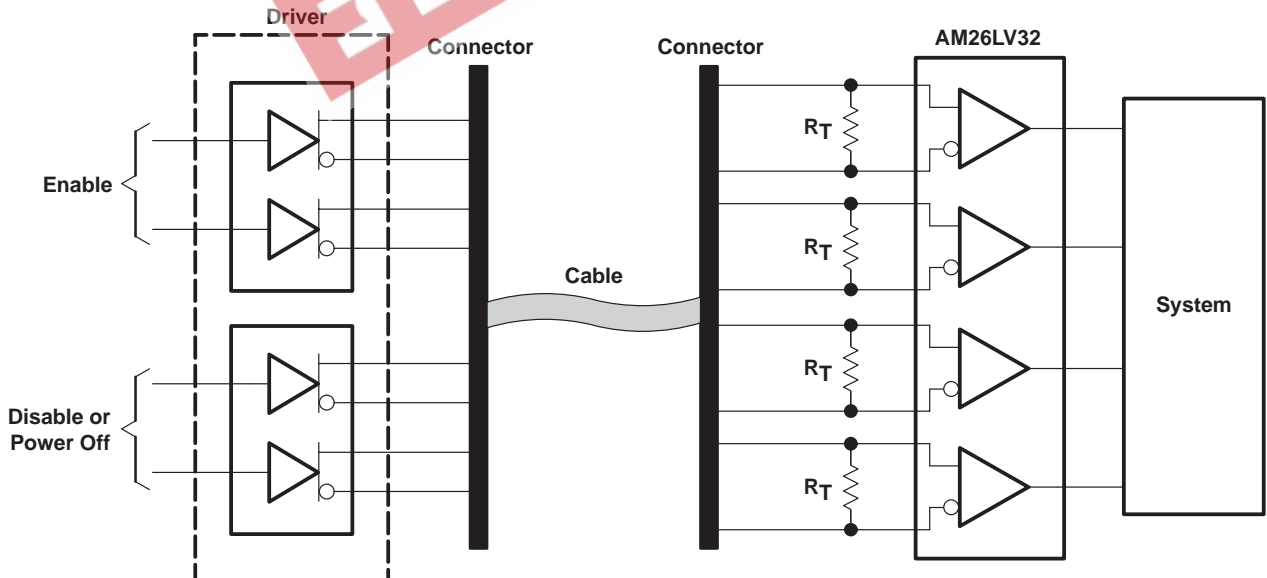


Figure 10. Typical Application Where Two or More Drivers are Disabled

APPLICATION INFORMATION

Figure 11 is an alternative application design to replace the application in Figure 10. This design uses two AM26LV32 devices, instead of one. However, this design does not require the input levels be monitored to ensure the outputs are in the correct state, only that they comply to the RS-232 standard.

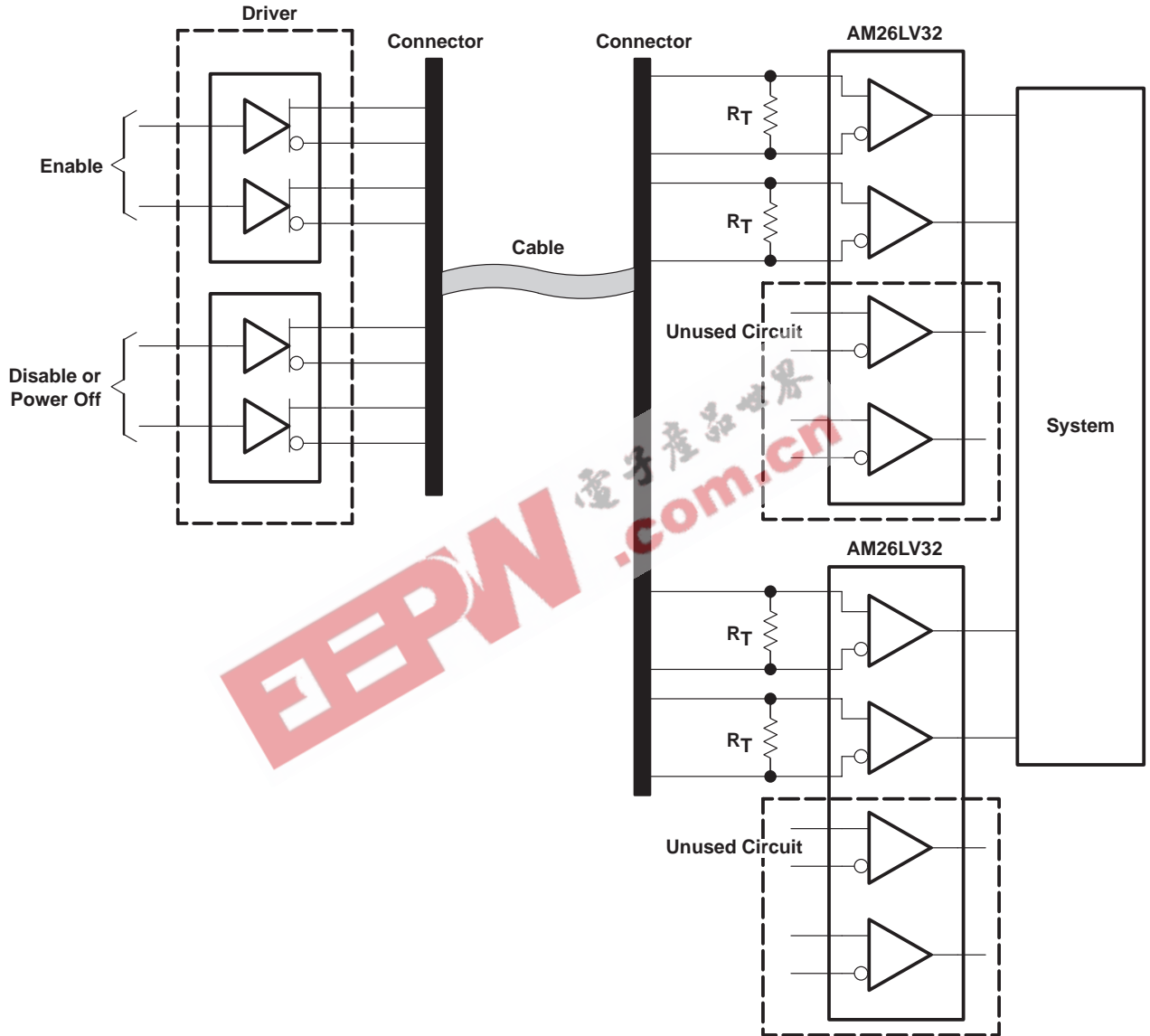


Figure 11. Alternative Solution for Figure 10

APPLICATION INFORMATION

Figures 12 and 13 show typical applications where a disconnected cable occurs. Figure 12 illustrates a typical application where a cable is disconnected. Similar to Figure 10, the active input levels must be monitored to make sure the inactive receiver outputs are in a high state. An alternative solution is shown in Figure 13.

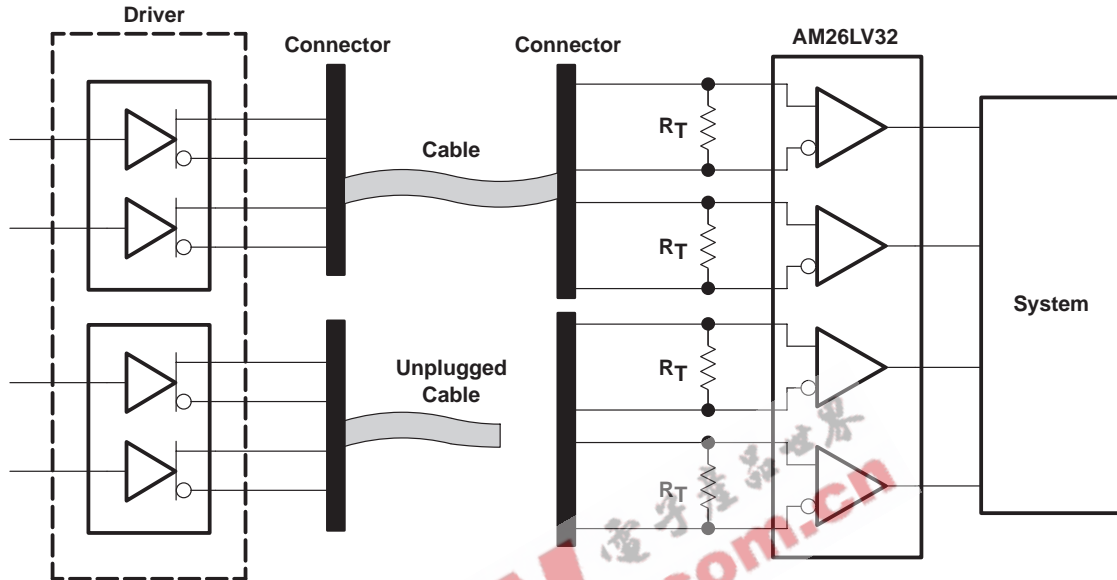
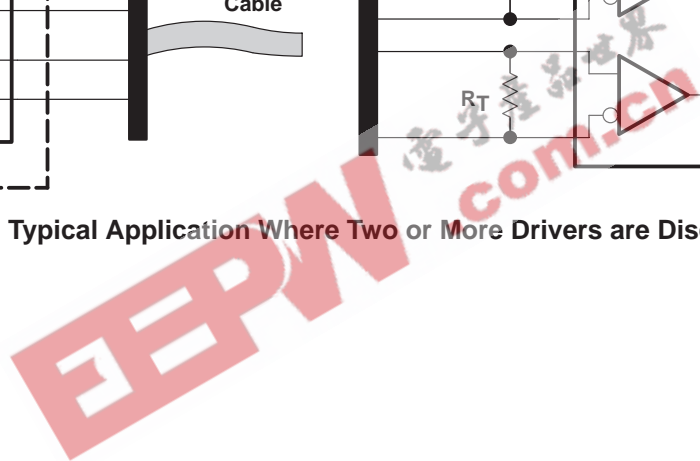


Figure 12. Typical Application Where Two or More Drivers are Disconnected



**APPLICATION INFORMATION**

Figure 13 is an alternative solution so the receiver inputs do not have to be monitored. This solution also requires the use of two AM26LV32 devices, instead of one.

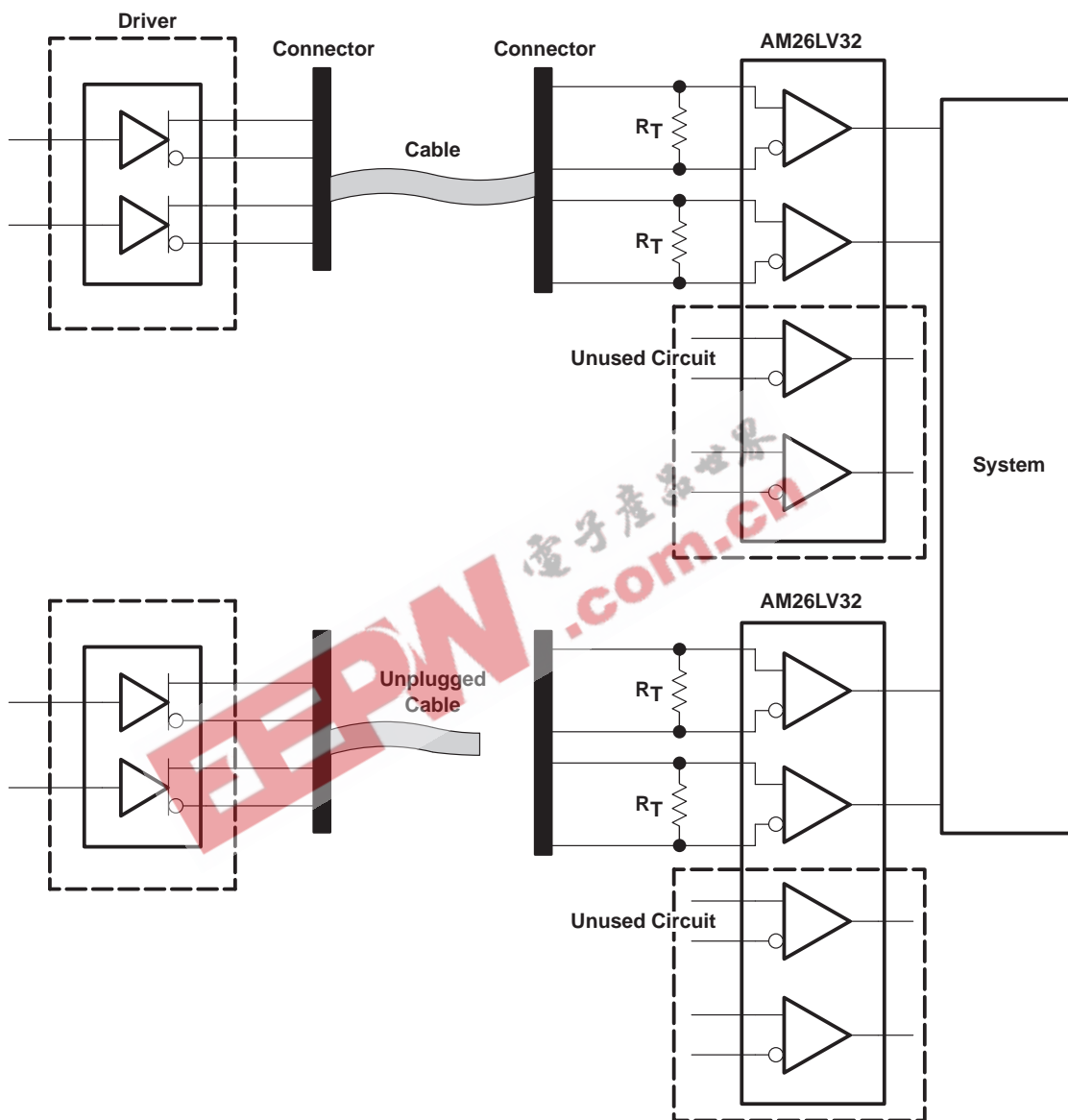


Figure 13. Alternative Solution to Figure 12

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AM26LV32

## LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202D – MAY 1995 – REVISED APRIL 2000

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### APPLICATION INFORMATION

When designing a system using the AM26LV32, the device provides a robust solution where fail-safe and fault conditions are of concern. The RS-422-like inputs accept common-mode input levels from  $-0.3\text{ V}$  to  $5.5\text{ V}$  with a specified sensitivity of  $\pm 200\text{ mV}$ . As previously shown, care must be taken with active input levels since they can affect the outputs of unused or inactive bits. However, most applications meet or exceed the requirements to allow the device to perform properly.

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
AM26LV32CD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
AM26LV32CDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
AM26LV32CNSLE	OBSOLETE	SO	NS	16		None	Call TI	Call TI
AM26LV32CNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

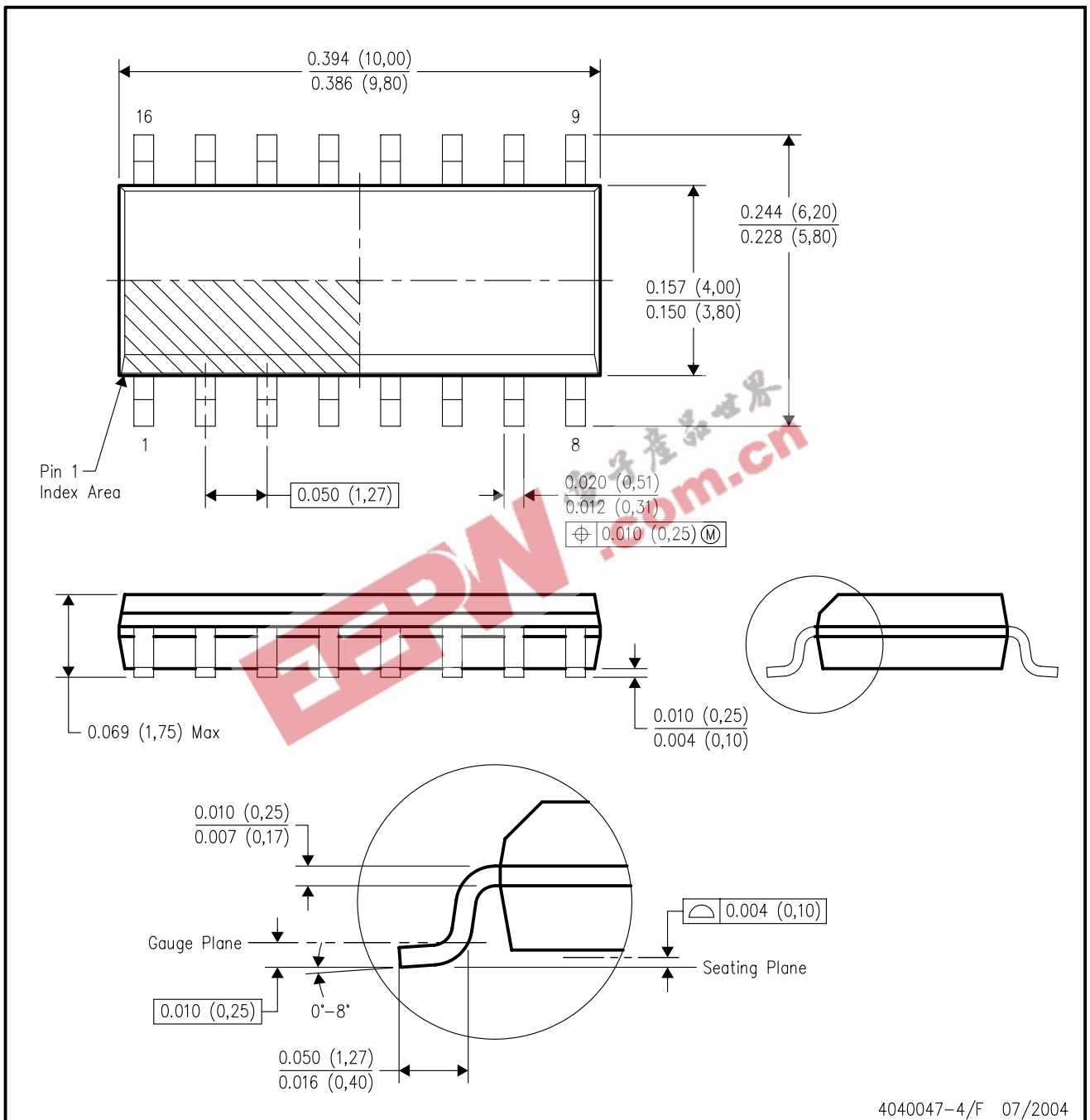
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AC.

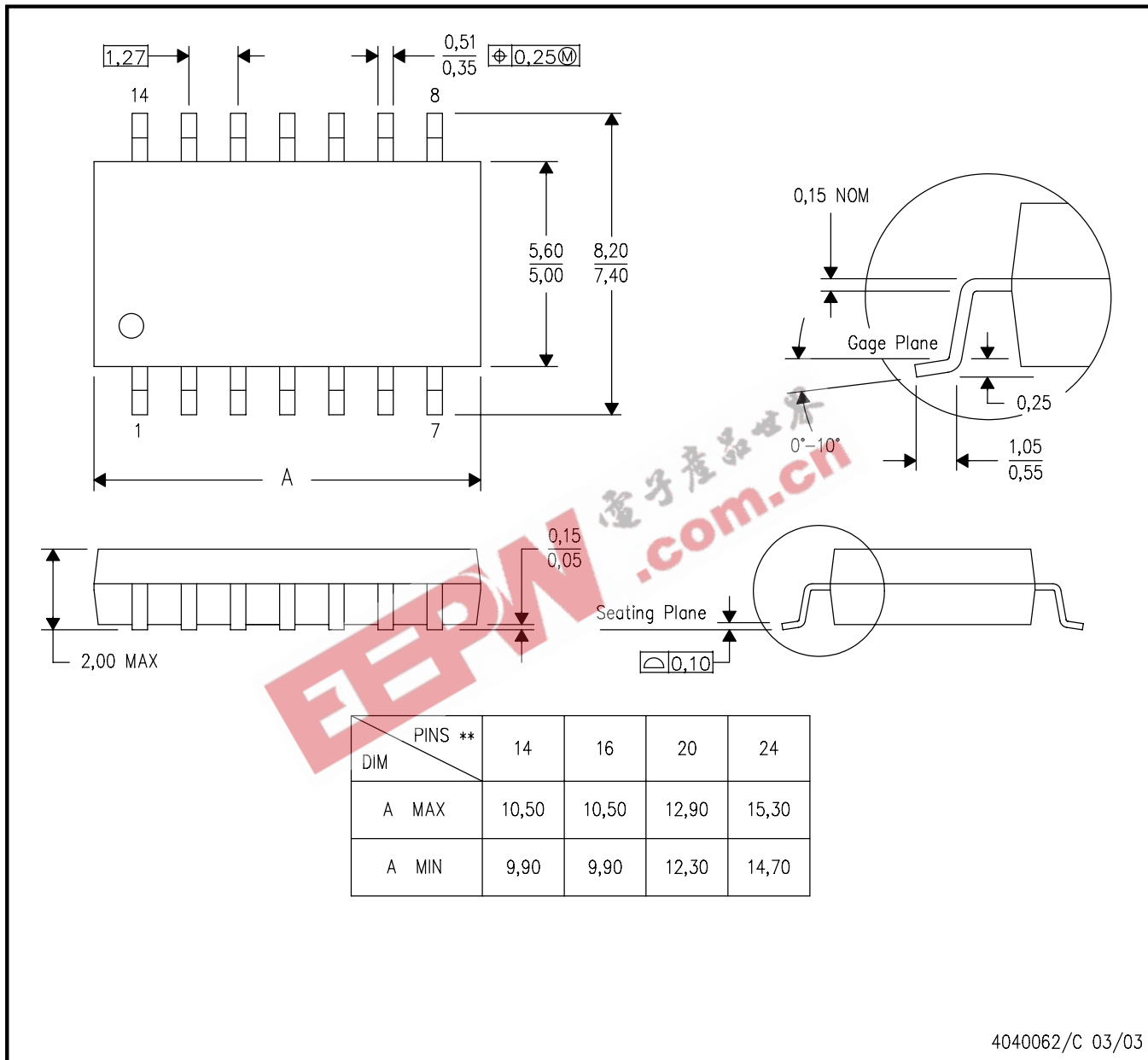


MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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