DUAL 4-A HIGH-SPEED LOW-SIDE MOSFET DRIVERS WITH ENABLE

Check for Samples: UCC27423-Q1, UCC27424-Q1, UCC27425-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Industry-Standard Pinout**
- **Enable Functions for Each Driver**
- **High Current Drive Capability of ±4 A**
- **Unique Bipolar and CMOS True Drive Output Stage Provides High Current at MOSFET Miller Thresholds**
- **TTL/CMOS Compatible Inputs Independent of Supply Voltage**
- **20-ns Typical Rise and 15-ns Typical Fall Times With 1.8-nF Load**
- **Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising**
- **4-V to 15-V Supply Voltage**
- **Dual Outputs Can Be Paralleled for Higher Drive Current**
- **Rated From –40°C to 125°C**

APPLICATIONS

- **Switch Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Line Drivers**
- **Class D Switching Amplifiers**

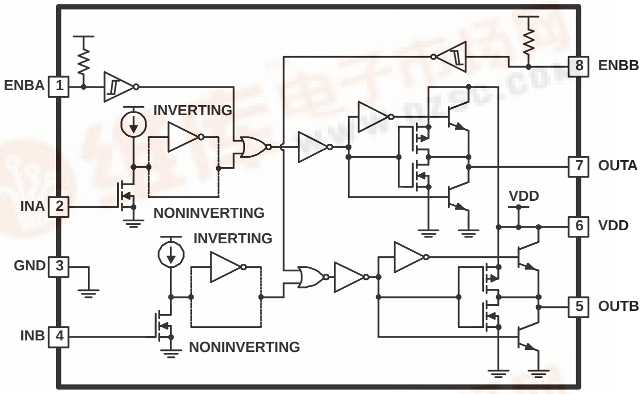
DESCRIPTION

The UCC2742x high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. Two standard logic options are offered – dual inverting and dual noninverting drivers. They are offered in the standard SOIC-8 (D) package.

Using a design that inherently minimizes shoot-through current, these drivers deliver 4-A current where it is needed most, at the Miller plateau region, during the MOSFET switching transition. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

The UCC2742x provide enable (ENBL) functions to have better control of the operation of the driver applications. ENBA and ENBB are implemented on pins 1 and 8, which were previously left unused in the industry standard pinout. They are internally pulled up to V_{DD} for active-high logic and can be left open for standard operation.

BLOCK DIAGRAM



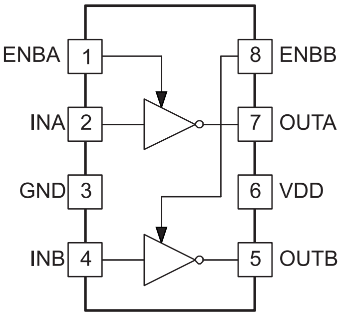
ORDERING INFORMATION(1)(2)

T_A	CONFIGURATION	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Dual Inverting	SOIC – D	Reel of 2500	UCC27423QDRQ1	27423Q
	Dual Noninverting			UCC27424QDRQ1	27424Q
	One Inverting, One Noninverting			UCC27425QDRQ1	27425Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

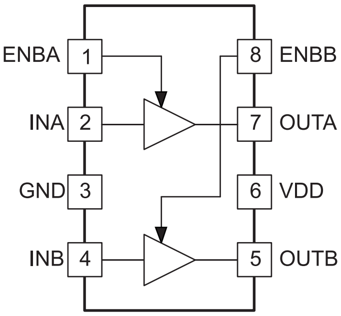
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

UCC27423
D PACKAGE
(TOP VIEW)



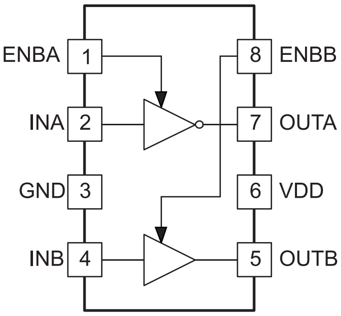
(DUAL INVERTING)

UCC27424
D PACKAGE
(TOP VIEW)



(DUAL NON-INVERTING)

UCC27425
D PACKAGE
(TOP VIEW)



(ONE INVERTING,
ONE NON-INVERTING)

Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ENBA	1	I	Enable input for the driver A with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. The output state when the device is disabled is low, regardless of the input state.
INA	2	I	Input A. Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
GND	3		Common ground. This ground should be connected very closely to the source of the power MOSFET which the driver is driving.
INB	4	I	Input B. Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
OUTB	5	O	Driver output B. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
VDD	6		Supply voltage and the power input connection for this device.
OUTA	7	O	Driver output A. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
ENBB	8	I	Enable input for the driver B with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. The output state when the device is disabled is low, regardless of the input state.

Table 2. INPUT/OUTPUT TABLE

ENBA	ENBB	INPUTS (V_{IN_L}, V_{IN_H})		UCC27423		UCC27424		UCC27425	
		INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H	H	L	L	H	H	L	L	H	L
H	H	L	H	H	L	L	H	H	H
H	H	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage		–0.3 V to 16 V
I_{OUT}	Output current	DC	0.3 A
		Pulsed, 0.5 μs	4.5 A
V_{IN}	Input voltage	INA, INB	–5 V to 6 V or (V_{DD} + 0.3) (whichever is larger)
V_{EN}	Enable voltage	ENBA, ENBB	–0.3 V to 6 V or (V_{DD} + 0.3) (whichever is larger)
P_D	Power dissipation	T_A = 25°C	650 mW
T_J	Junction operating temperature range		–55°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND. Currents are positive into, negative out of, the specified terminal.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING T_A = 70°C (mW)(1)	DERATING FACTOR ABOVE T_A = 70°C (mW/°C)(1)
D (SOIC-8)	42	84 to 160(2)	344 to 655(2)	6.25 to 11.9(2)

(1) 125°C operating junction temperature is used for power rating calculations.

(2) The range of values indicates the effect of the PCB. These values are intended to give the system designer an indication of the best- and worst-case conditions. In general, the system designer should attempt to use larger traces on the PCB, where possible, to spread the heat away form the device more effectively.

ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V, T_A = –40°C to 125°C, $T_A = T_J$ (unless otherwise noted)

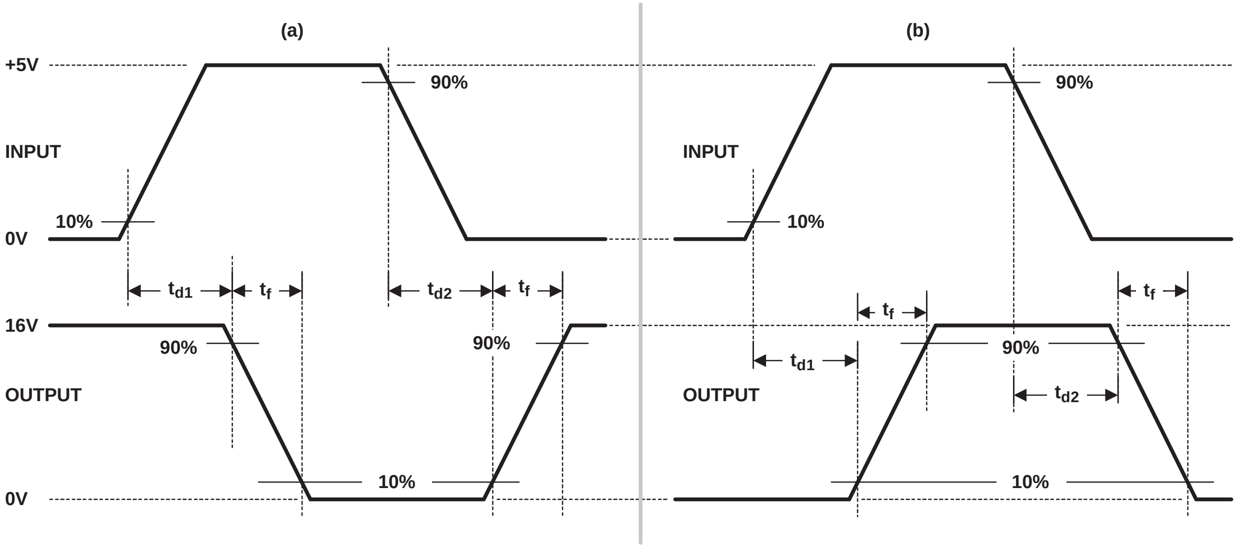
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input (INA, INB)							
V_{IH}	Logic 1 input threshold			2			V
V_{IL}	Logic 0 input threshold					1	V
I_{IN}	Input current	V_{IN} = 0 V to V_{DD}		–10	0	10	µA
Output (OUTA, OUTB)							
I_{OUT}	Output current	V_{DD} = 14 V(1) (2)			4		A
V_{OH}	High-level output voltage	$V_{OH} = V_{DD} – V_{OUT}$, I_{OUT} = –10 mA, V_{DD} = 14 V			330	450	mV
V_{OL}	Low-level output voltage	I_{OUT} = 10 mA, V_{DD} = 14 V			22	40	mV
R_{OH}	Output resistance high	T_A = 25°C, I_{OUT} = –10 mA, V_{DD} = 14 V(3)		25	30	35	Ω
		T_A = full range, I_{OUT} = –10 mA, V_{DD} = 14 V(3)		18		45	
R_{OL}	Output resistance low	T_A = 25°C, I_{OUT} = 10 mA, V_{DD} = 14 V(3)		1.9	2.2	2.5	Ω
		T_A = full range, I_{OUT} = 10 mA, V_{DD} = 14 V(3)		1.2		4	
	Latch-up protection(1)			500			mA
Switching Time							
t_r	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			20	40	ns
t_f	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF(1)			15	40	ns
t_{D1}	Delay time, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF(1)			25	50	ns
t_{D2}	Delay time, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF(1)	UCC27423, UCC27424		35	60	ns
			UCC27425		35	70	
Enable (ENBA, ENBB)							
V_{IN_H}	High-level input voltage	Low to high transition		1.7	2.4	2.9	V
V_{IN_L}	Low-level input voltage	High to low transition		1.1	1.8	2.2	V
	Hysteresis			0.15	0.55	0.90	V
R_{ENBL}	Enable impedance	V_{DD} = 14 V, ENBL = GND		75	100	145	kΩ
t_{D3}	Propagation delay time (see Figure 2)	C_{LOAD} = 1.8 nF(1)(4)			30	60	ns
t_{D4}	Propagation delay time (see Figure 2)	C_{LOAD} = 1.8 nF(1)(4)			100	150	ns

(1) Specified by design
(2) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the Rds(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.
(4) Not production tested

ELECTRICAL CHARACTERISTICS (continued)

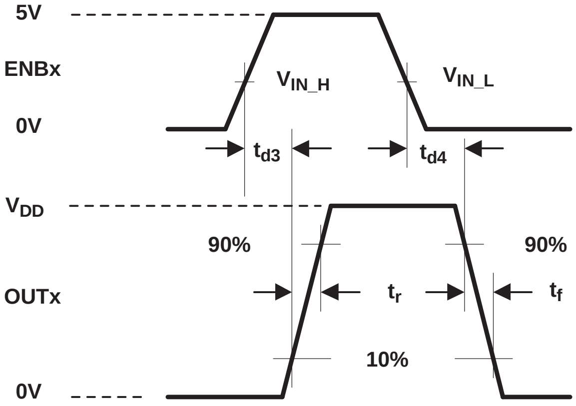
V_{DD} = 4.5 V to 15 V, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
Overall									
I_{DD}	Operating current	Static, V_{DD} = 15 V, ENBA = ENBB = 15 V	UCC27423	INA = 0 V	INB = 0 V		900	1350	μA
					INB = High		750	1100	
				INA = High	INB = 0 V		750	1100	
					INB = High		600	900	
			UCC27424	INA = 0 V	INB = 0 V		300	450	
					INB = High		750	1100	
				INA = High	INB = 0 V		750	1100	
					INB = High		1200	1800	
			UCC27425	INA = 0 V	INB = 0 V		600	900	
					INB = High		1050	1600	
				INA = High	INB = 0 V		450	700	
					INB = High		900	1350	
		Disabled, V_{DD} = 15 V, ENBA = ENBB = 0 V	All	INA = 0 V	INB = 0 V		300	450	
					INB = High		450	700	
				INA = High	INB = 0 V		450	700	
					INB = High		600	900	



A. The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver



A. The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 2. Switching Waveform for Enable to Output

TYPICAL CHARACTERISTICS

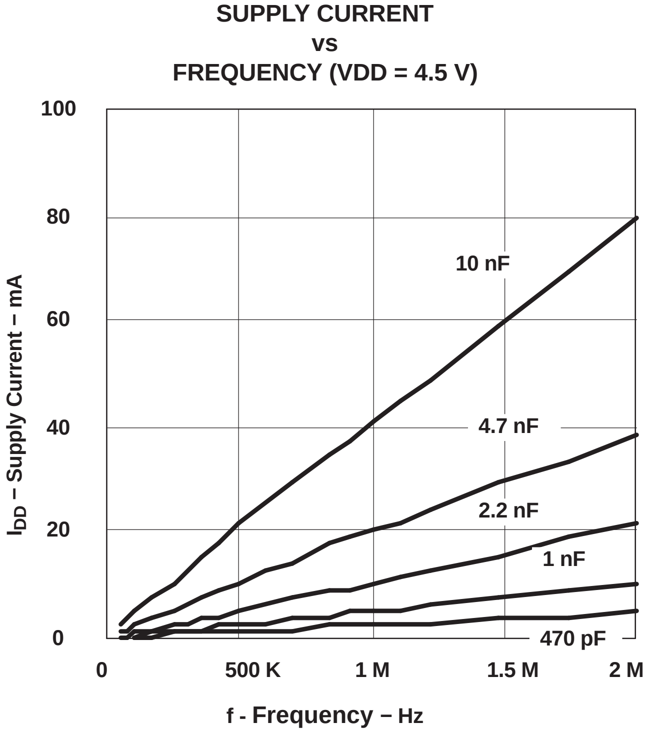


Figure 3.

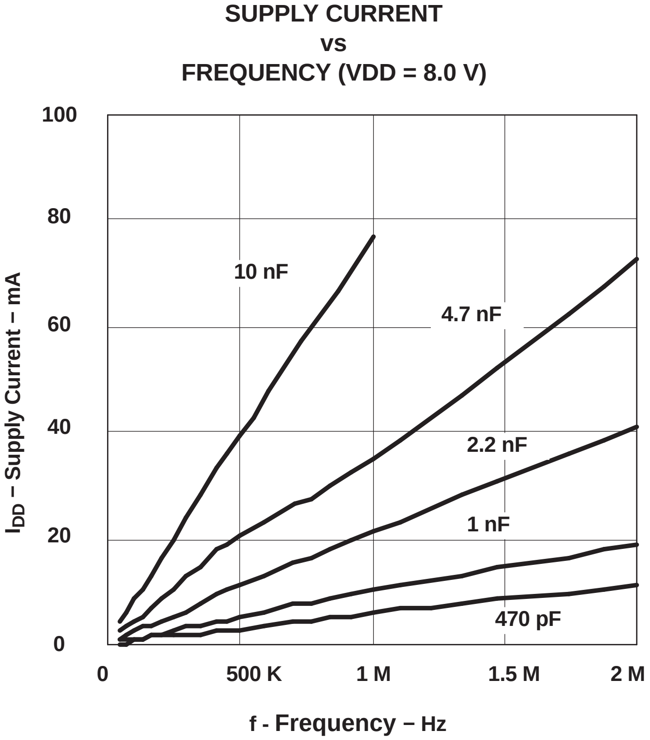


Figure 4.

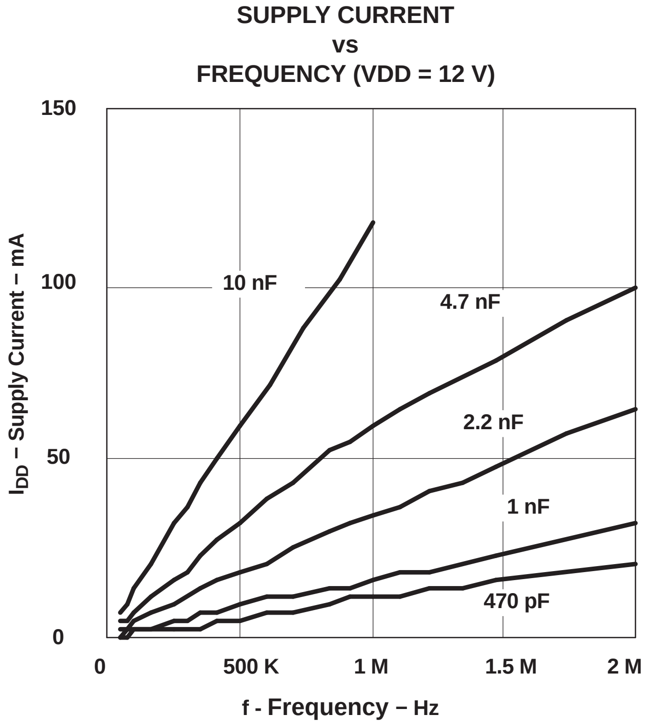


Figure 5.

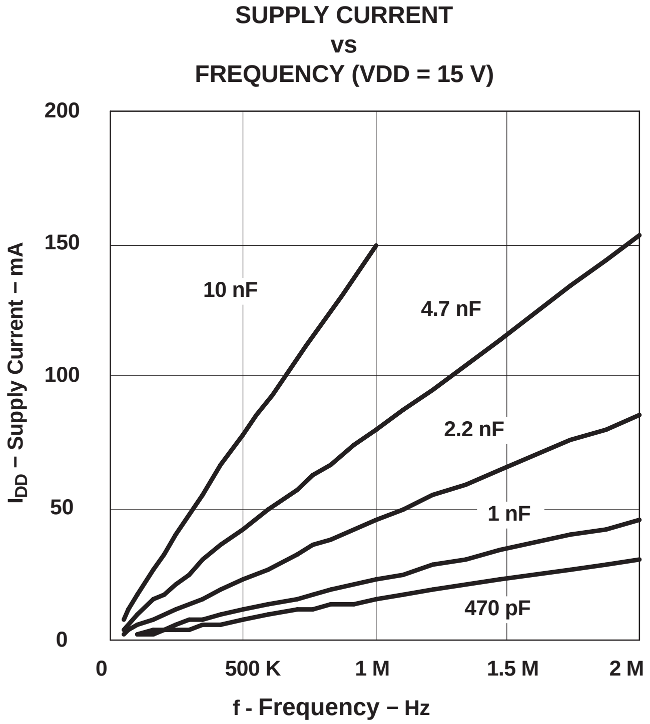
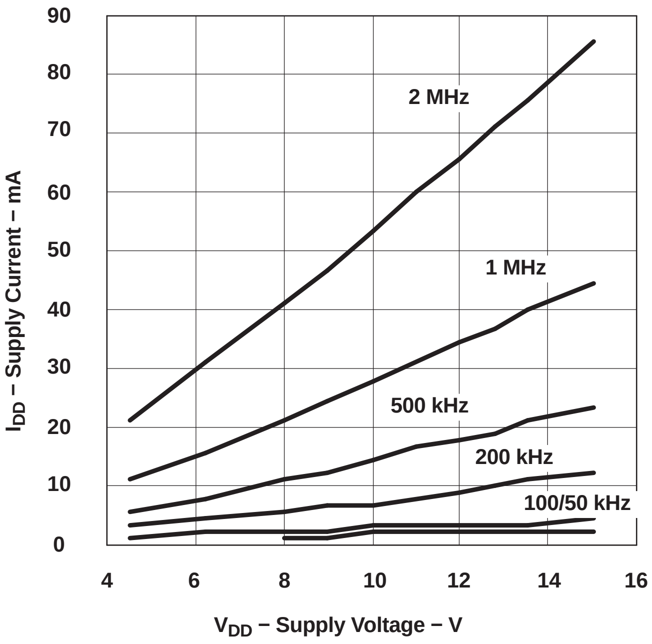


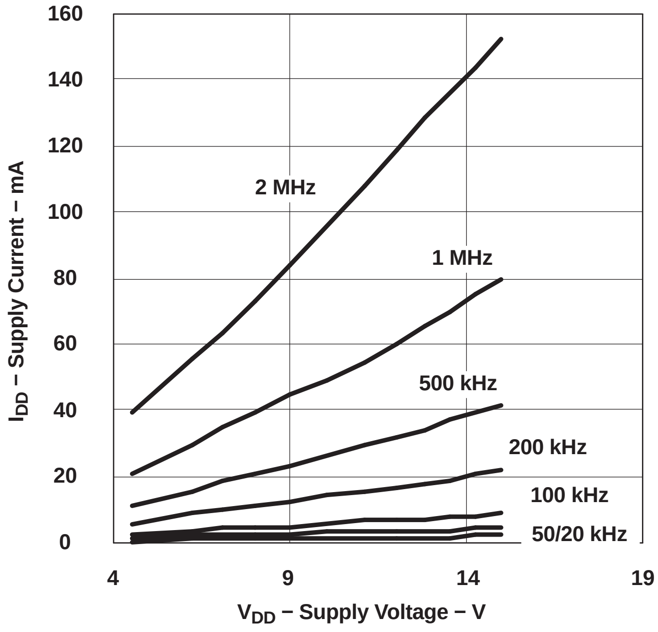
Figure 6.

TYPICAL CHARACTERISTICS (continued)



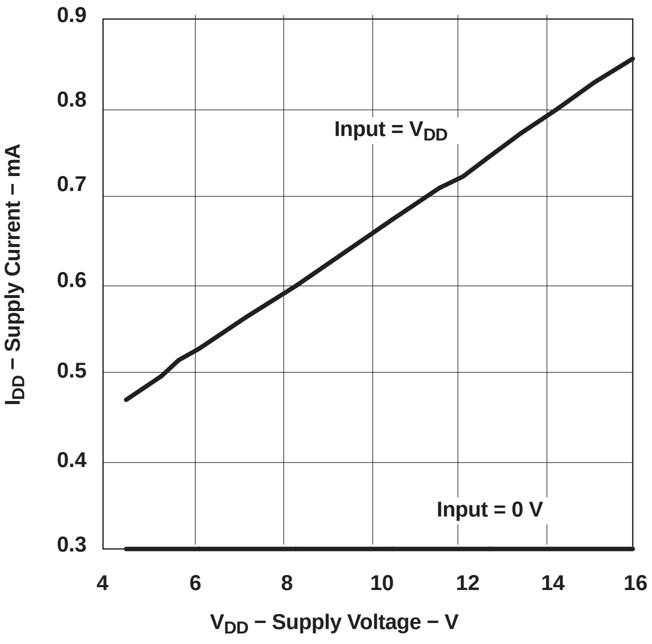
SUPPLY CURRENT vs SUPPLY VOLTAGE (C_{LOAD} = 2.2 nF)

Figure 7.



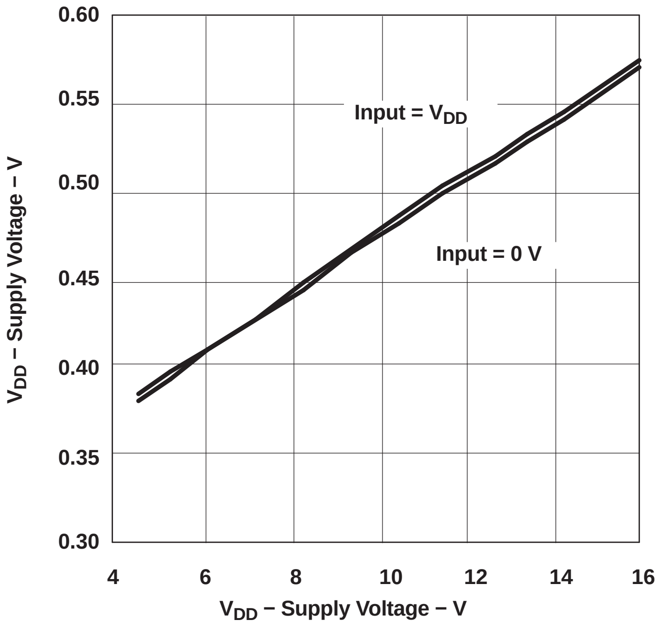
SUPPLY CURRENT vs SUPPLY VOLTAGE (C_{LOAD} = 4.7 nF)

Figure 8.



SUPPLY CURRENT vs SUPPLY VOLTAGE (UCC27423)

Figure 9.



SUPPLY CURRENT vs SUPPLY VOLTAGE (UCC27424)

Figure 10.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE (UCC27425)

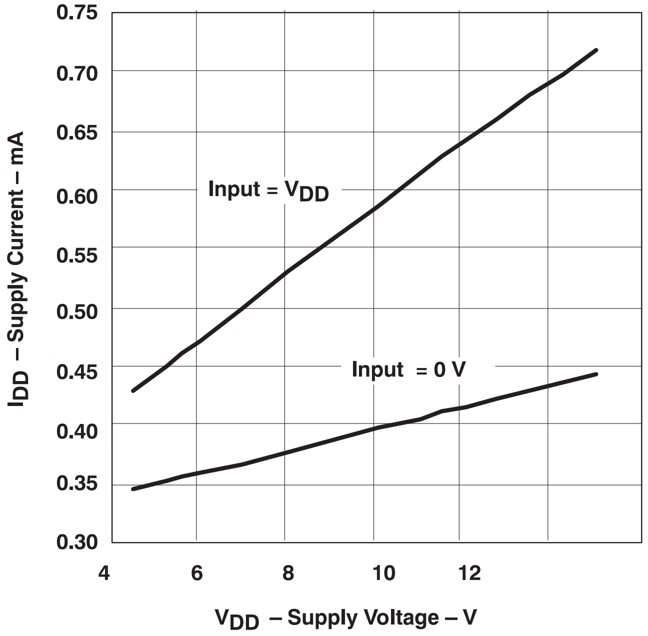


Figure 11.

RISE TIME/FALL TIME
vs
TEMPERATURE (UCC27423)

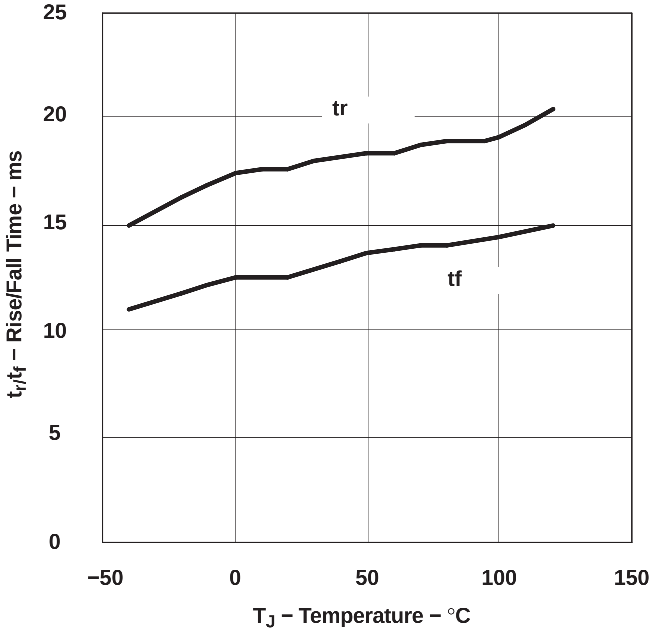


Figure 12.

RISE TIME
vs
SUPPLY VOLTAGE

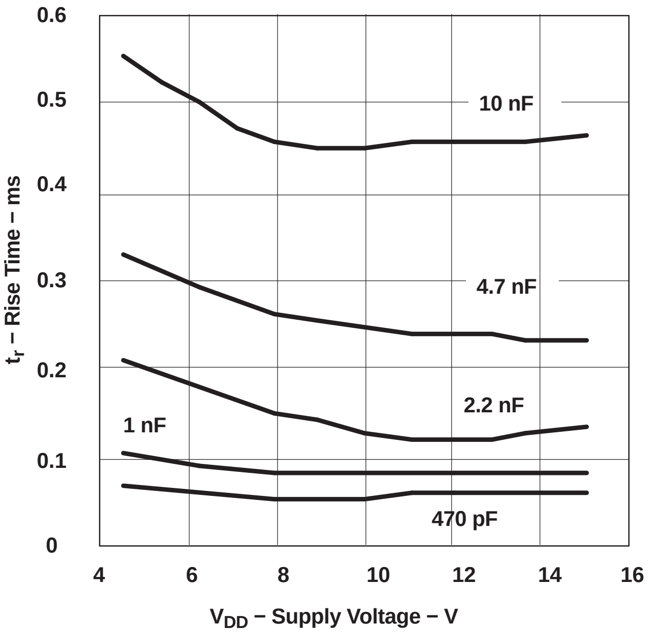


Figure 13.

FALL TIME
vs
SUPPLY VOLTAGE

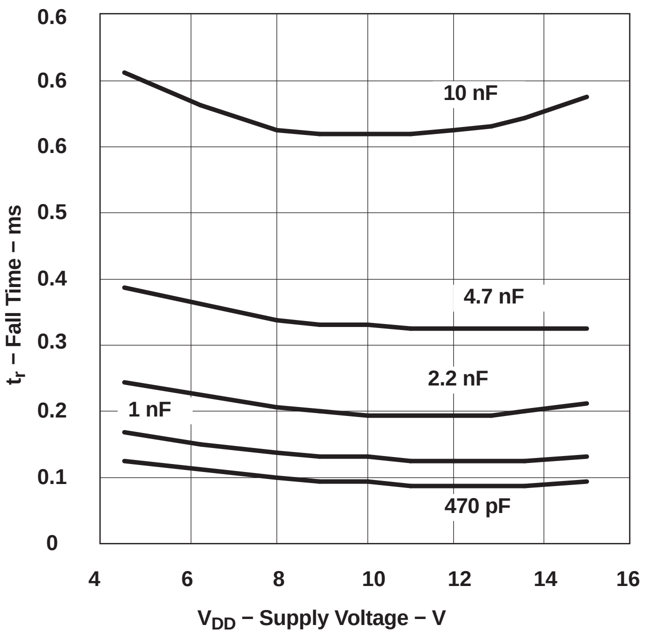
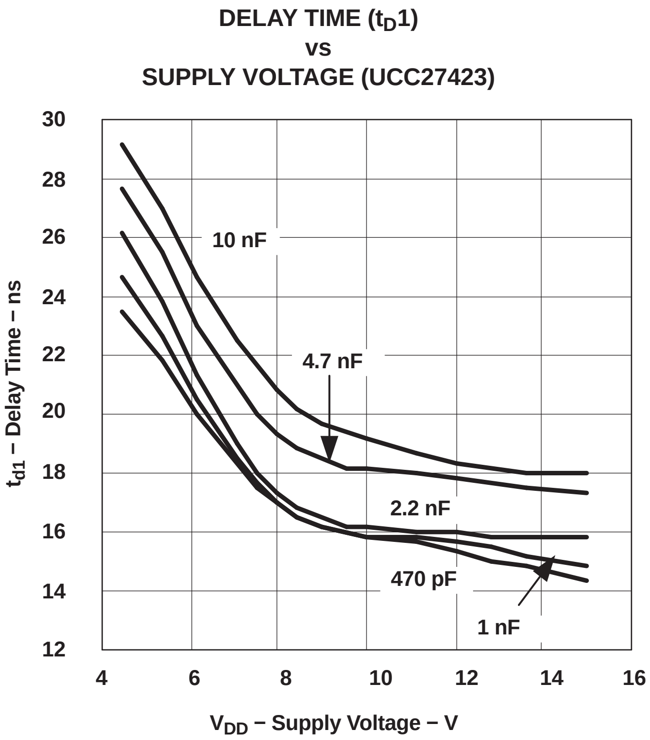


Figure 14.

TYPICAL CHARACTERISTICS (continued)



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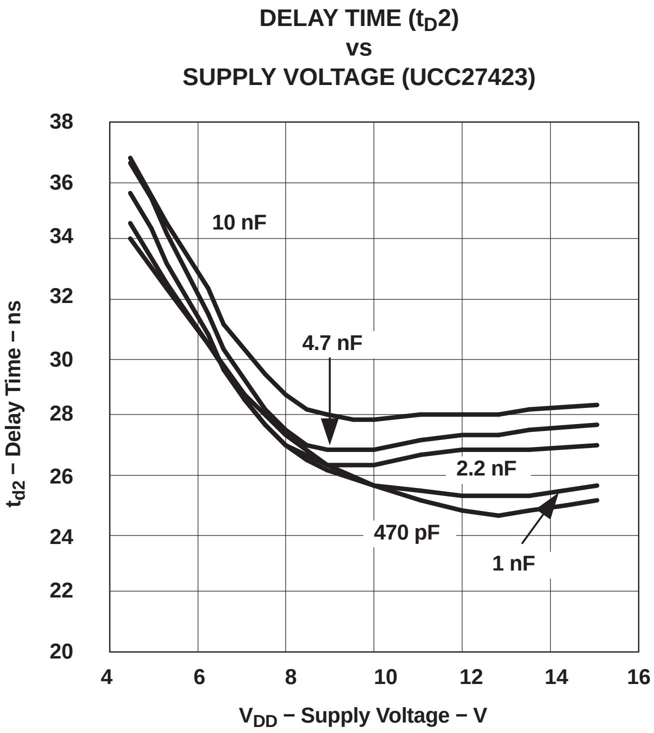

Figure 16.

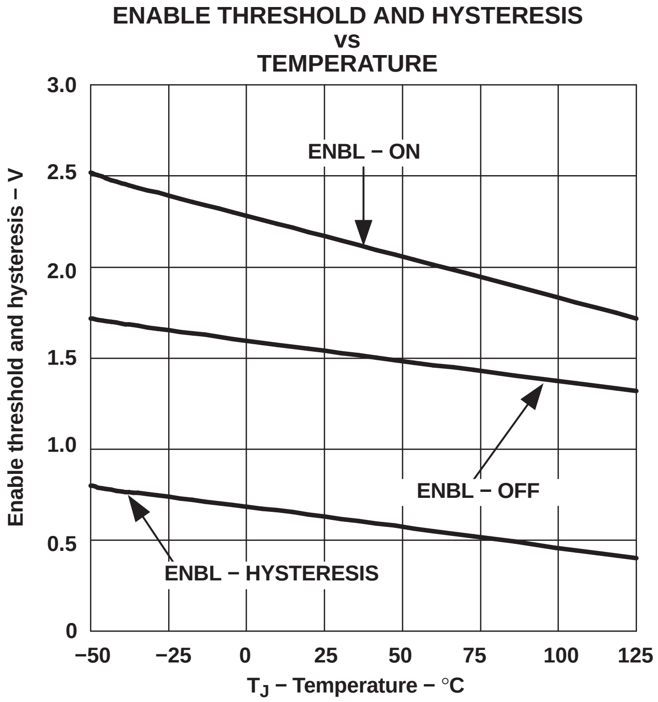

Figure 17.

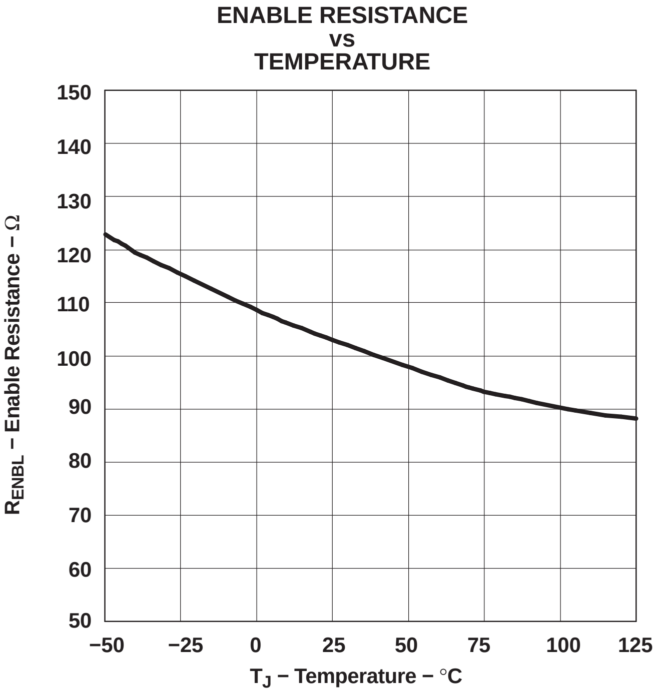

Figure 18.

TYPICAL CHARACTERISTICS (continued)

OUTPUT BEHAVIOR vs SUPPLY VOLTAGE (INVERTING)

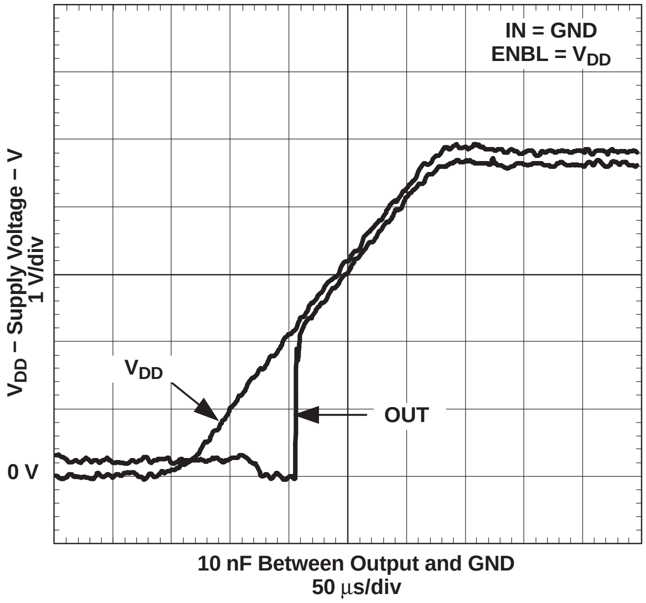

Figure 19.

OUTPUT BEHAVIOR vs SUPPLY VOLTAGE (INVERTING)

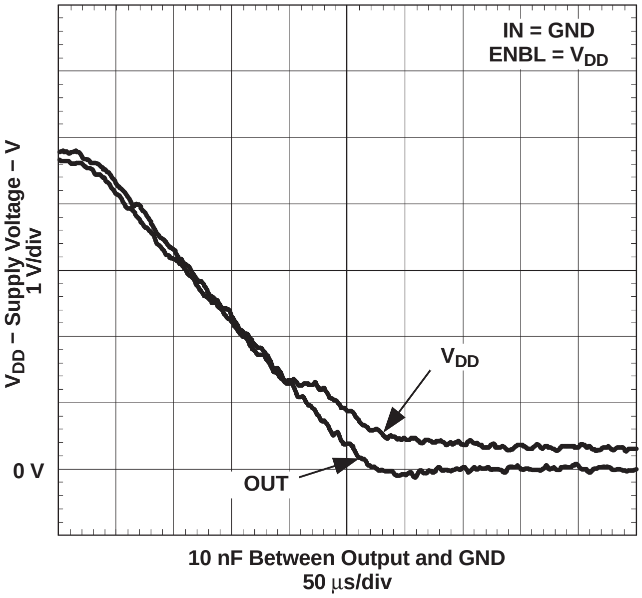

Figure 20.

OUTPUT BEHAVIOR vs VDD (INVERTING)

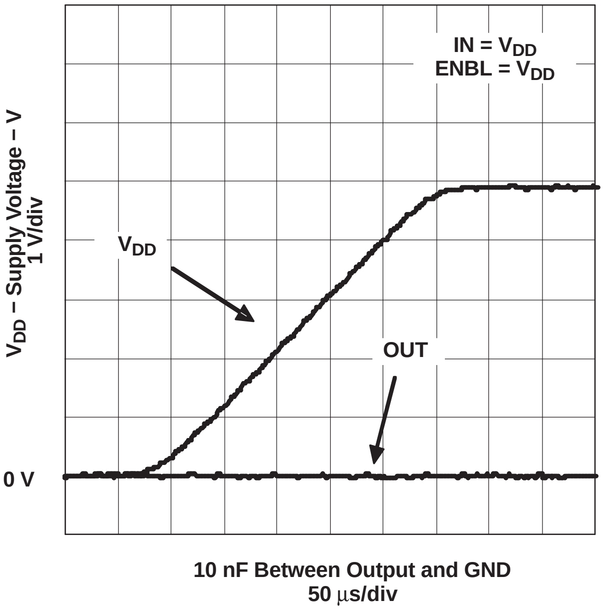

Figure 21.

OUTPUT BEHAVIOR vs VDD (INVERTING)

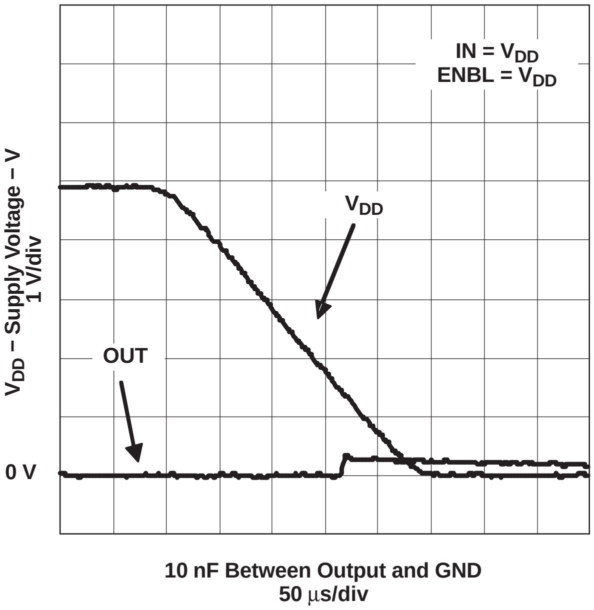

Figure 22.

TYPICAL CHARACTERISTICS (continued)

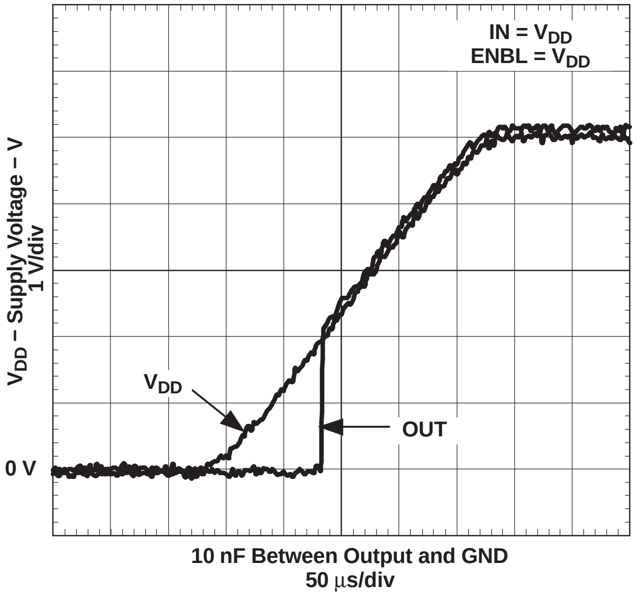
OUTPUT BEHAVIOR
vs
VDD (NONINVERTING)

Figure 23.

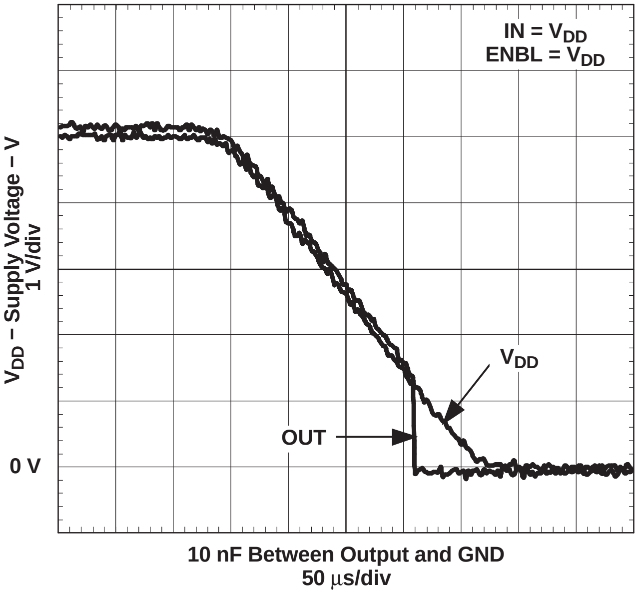
OUTPUT BEHAVIOR
vs
VDD (NONINVERTING)

Figure 24.

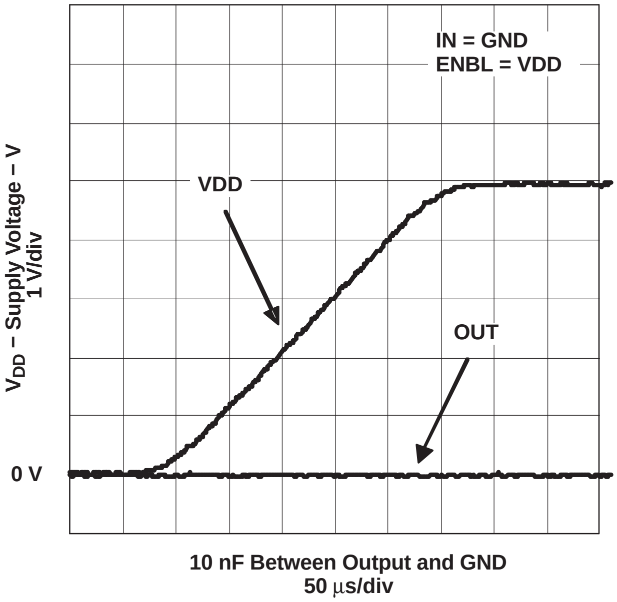
OUTPUT BEHAVIOR
vs
VDD (NONINVERTING)

Figure 25.

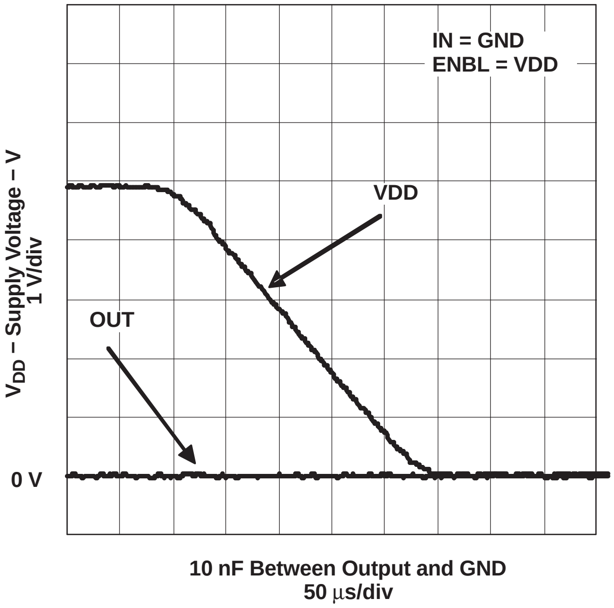
OUTPUT BEHAVIOR
vs
VDD (NONINVERTING)

Figure 26.

TYPICAL CHARACTERISTICS (continued)

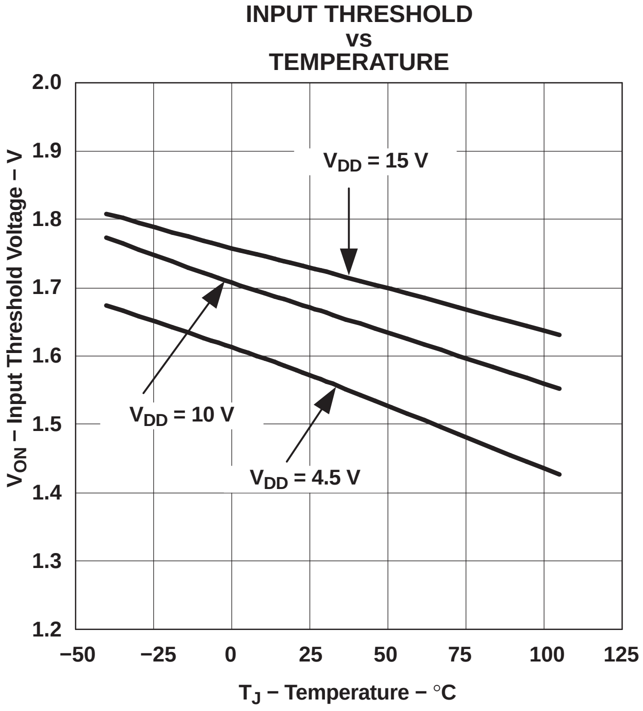

Figure 27.

APPLICATION INFORMATION

General Information

High frequency power supplies often require high-speed, high-current drivers such as the UCC27423/UCC27424. A leading application is the need to provide a high power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is utilized to drive the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

Driver ICs are utilized when it is not feasible to have the primary PWM regulator IC directly drive the switching devices for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC27423/UCC27424. Finally, the control IC may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltages; yet it is equally compatible with 0 to V_{DD} signals. The inputs of UCC2742x drivers are designed to withstand 500-mA reverse current without either damage to the IC for logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in the section on Thermal Considerations.

Output Stage

Inverting outputs of the UCC2742x are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC2742x are intended to drive external N-channel MOSFETs.

Each output stage is capable of supplying ±4-A peak current pulses and swings to both V_{DD} and GND. The pullup/ pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the RDS(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external Schottky-clamp diodes are not required.

The UCC2742x family delivers the 4-A gate drive where it is most needed during the MOSFET switching transition – at the Miller plateau region – providing improved efficiency gains. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2742x drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. [1]

Two circuits are used to test the current capabilities of the UCC27423 driver. In each case external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 28 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC27423 is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

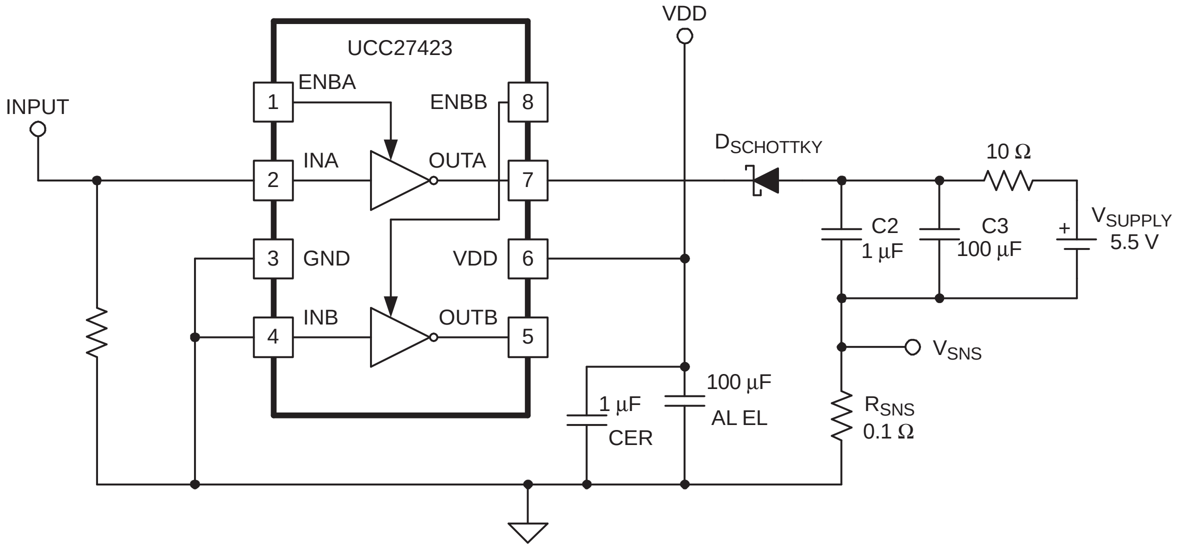

Figure 28. Current Sinking

The circuit shown in Figure 29 is used to test the current source capability with the output clamped to around 5 V with a string of Zener diodes. The UCC27423 is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

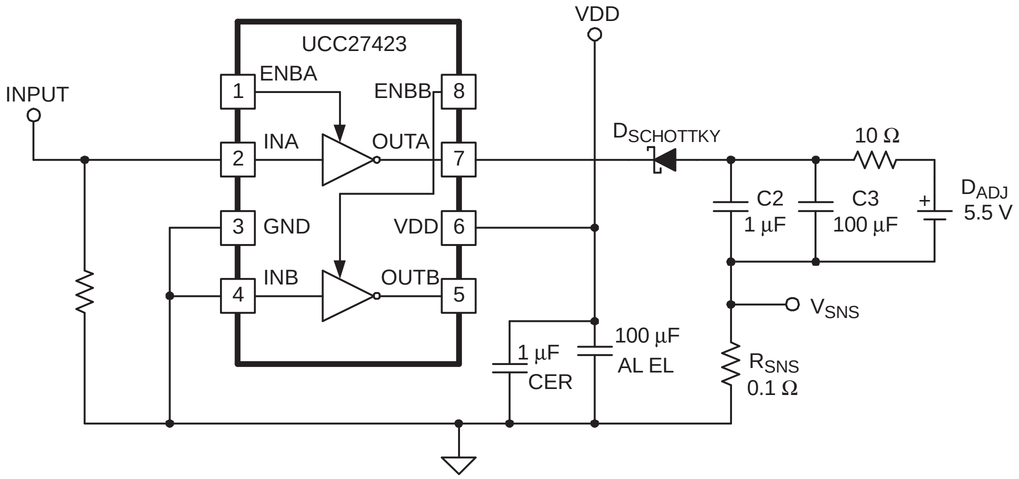

Figure 29. Current Sourcing

The current sink capability is slightly stronger than the current source capability at lower V_{DD}. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps to ensure that the MOSFET is held OFF during common power supply transients which may turn the device back ON.

Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together and the OUTA/OUTB outputs together. Then, a single signal can control the paralleled combination as shown in Figure 30.

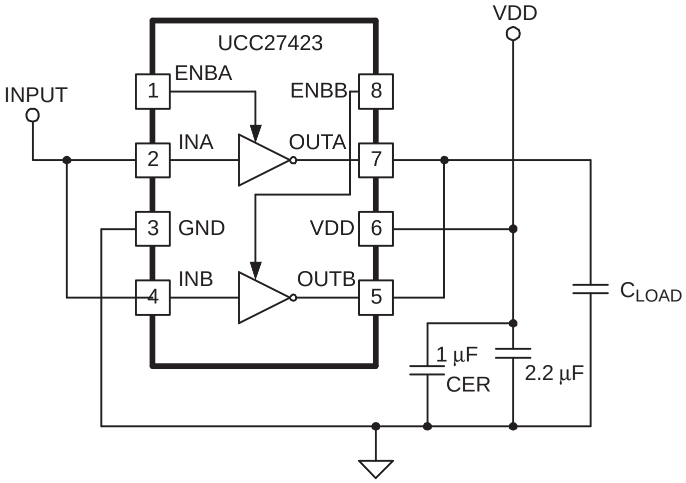

Figure 30. Parallel Outputs

Operational Waveforms and Circuit Layout

Figure 31 shows the circuit performance achievable with a single driver (half of the 8-pin IC) driving a 10-nF load. The input pulse width (not shown) is set to 300 ns to show both transitions in the output waveform. Note the linear rise and fall edges of the switching waveforms. This is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

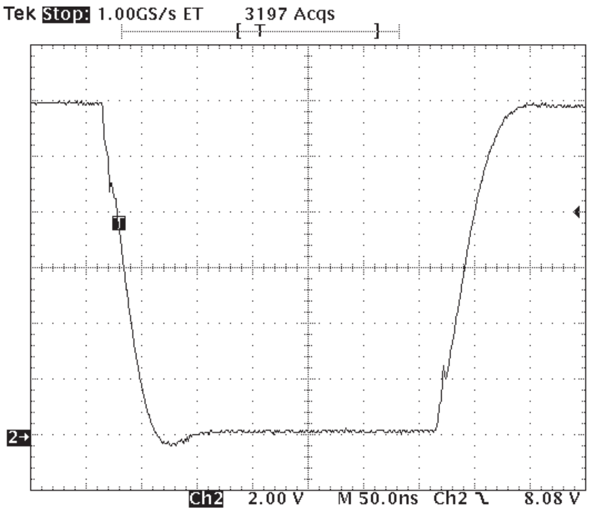

Figure 31. Pulse Response

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver IC as close as possible to the leads. The driver IC layout has ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections should also be made with a small enclosed loop area to minimize the inductance.

VDD

Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from:

$I_{OUT} = Q_g \times f$, where f is frequency

For the best high-speed circuit performance, two VDD bypass capacitors are recommended tp prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 1-µF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application.

Drive Current and Power Requirements

The UCC2742x drivers are capable of delivering 4 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

References 1 and 2 discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 2 includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$E = ½CV^2$, where C is the load capacitor, and V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$P = 2 \times ½CV^2f$, where f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W$

With a 12-V supply, this would equate to a current of:

$I = P / V = 0.432\ W / 12\ V = 0.036\ A$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load, the IC current draw is 0.0027 A. Under this condition, the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable, current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high-frequency switching spikes and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to that expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Q_g = CeffV to provide the following equation for power:

$P = C \times V^2 \times f = Q_g \times f$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

Enable

UCC2742x provide dual enable inputs for improved control of each driver channel operation. The inputs incorporate logic compatible thresholds with hysteresis. They are internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. When ENBA and ENBB are driven high, the drivers are enabled; when ENBA and ENBB are low, the drivers are disabled. The default state of the enable pin is to enable the driver and, therefore, can be left open for standard operation. The output states when the drivers are disabled is low, regardless of the input state. See Table 2 for operation using enable logic.

Enable inputs are compatible with both logic signals and slowly changing analog signals. They can be directly driven, or a power-up delay can be programmed with a capacitor between ENBA/ENBB and GND. ENBA and ENBB control input A and input B, respectively.

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits.

As shown in the power dissipation rating table, the SOIC-8 (D) package has a power rating of approximately 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in the previous example is 0.432 W with a 10-nF load, 12-V V_{DD}, switched at 300 kHz. Thus, only one load of this size could be driven using the D package, even if the two onboard drivers are paralleled.

References

[1] Laszlo Balogh, *Power Supply Seminar SEM-1400 Topic 2: Design And Application Guide For High Speed MOSFET Gate Drive Circuits* (SLUP133)

[2] Bill Andreycak, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* (SLUA105)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC27423QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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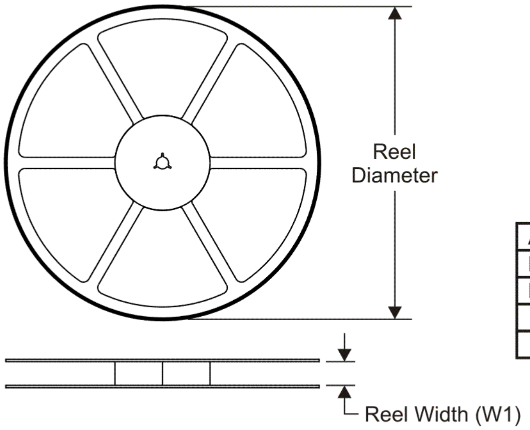
- Catalog: UCC27423, UCC27424, UCC27425
- Enhanced Product: UCC27424-EP

NOTE: Qualified Version Definitions:

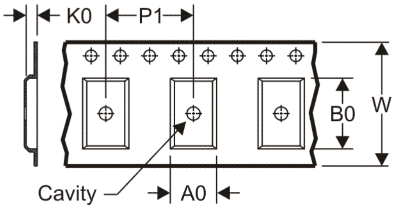
  - Catalog - TI's standard catalog product
  - Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

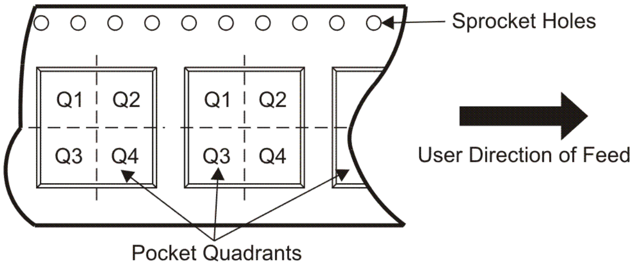


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

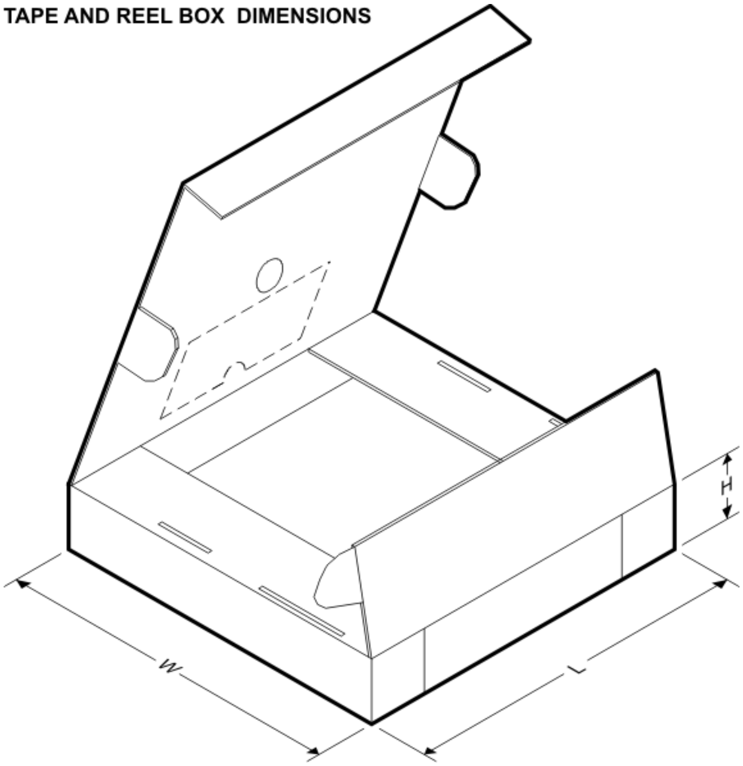
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27425QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

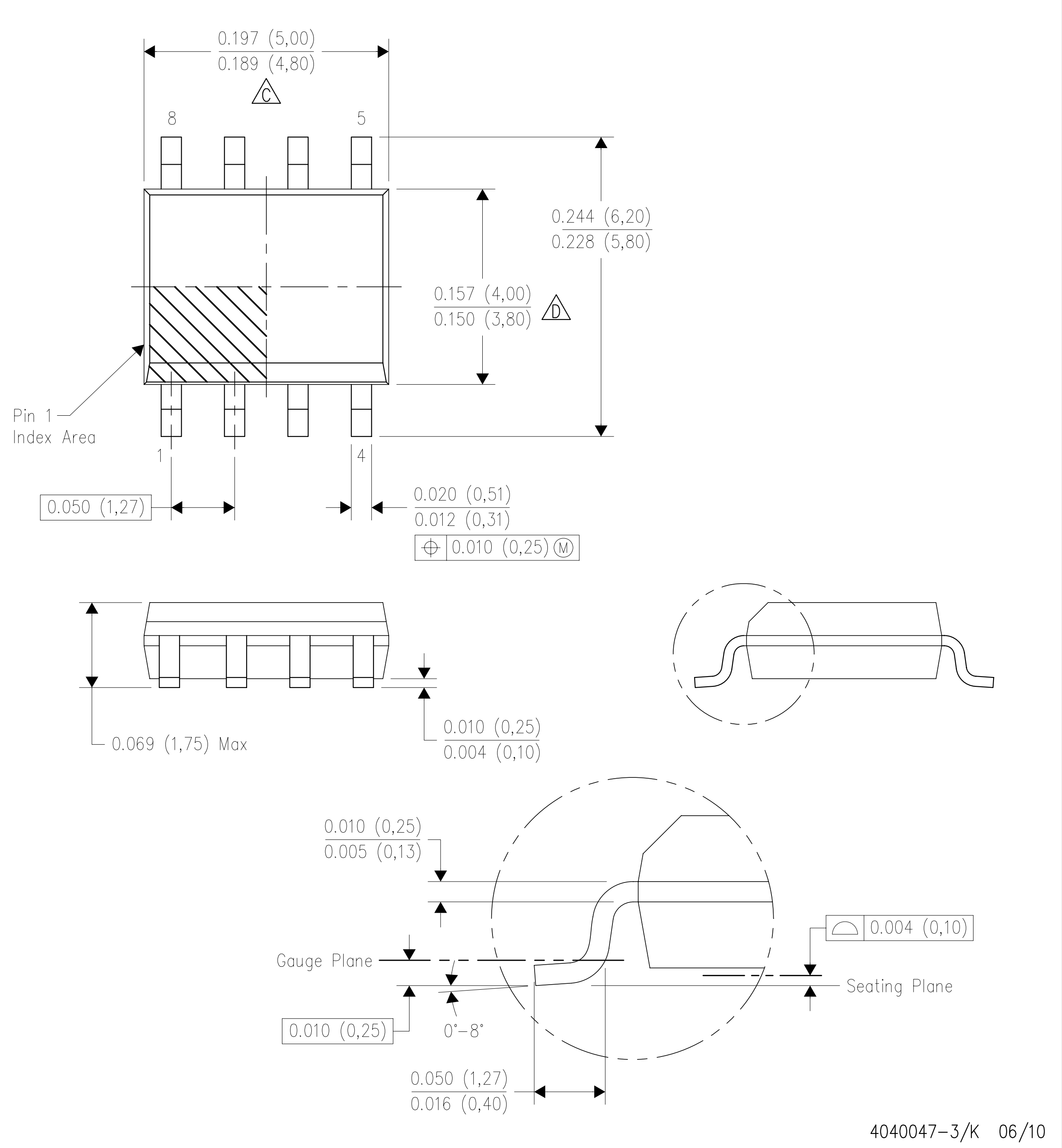
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

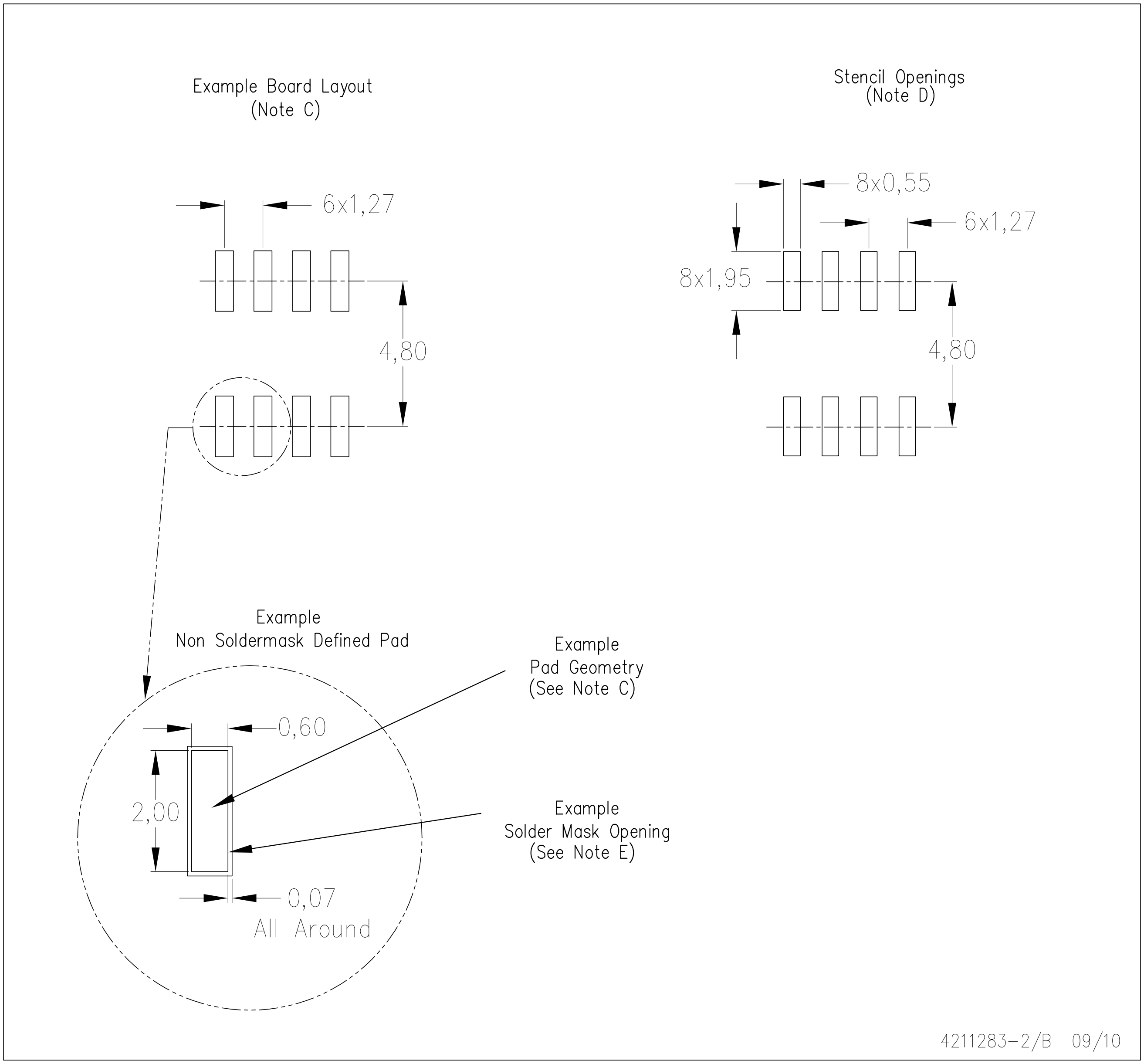
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27425QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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