MJD112 (NPN)
MJD117 (PNP)

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

ON Semiconductor®

http://onsemi.com

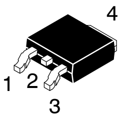
Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

Features

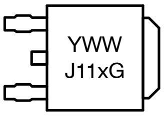
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series
- Pb−Free Packages are Available

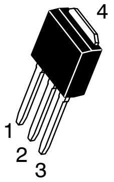
SILICON
POWER TRANSISTORS
2 AMPERES
100 VOLTS, 20 WATTS

MARKING DIAGRAMS

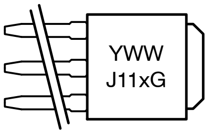


DPAK
CASE 369C





DPAK−3
CASE 369D



Y = Year
WW = Work Week
x = 2 or 7
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous − Peak	I_C	2 4	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation (Note1) @ $T_A = 25°C$ Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	71.4	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

July, 2010 − Rev. 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	–	20	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	–	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	–	2	mAdc
Collector−Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	–	10	μAdc
Emitter−Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	–	2	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3 Vdc)		500	–	
(I_C = 2 Adc, V_{CE} = 3 Vdc)		1000	12,000	
(I_C = 4 Adc, V_{CE} = 3 Vdc)		200	–	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 2 Adc, I_B = 8 mAdc)		–	2	
(I_C = 4 Adc, I_B = 40 mAdc)		–	3	
Base−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	–	4	Vdc
Base−Emitter On Voltage (I_C = 2 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	25	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}			pF
MJD117		–	200	
MJD112		–	100	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

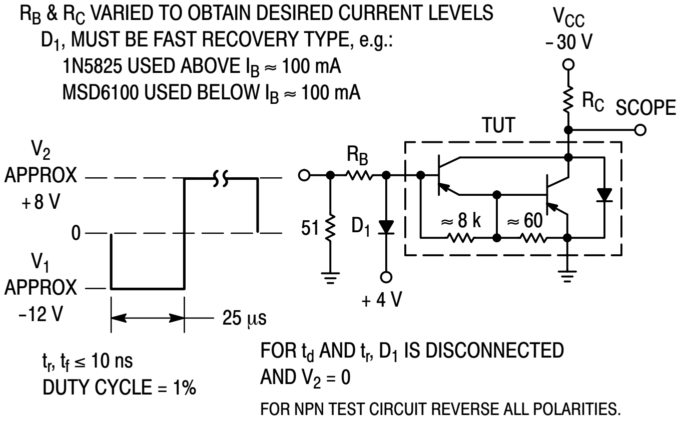


Figure 1. Switching Times Test Circuit

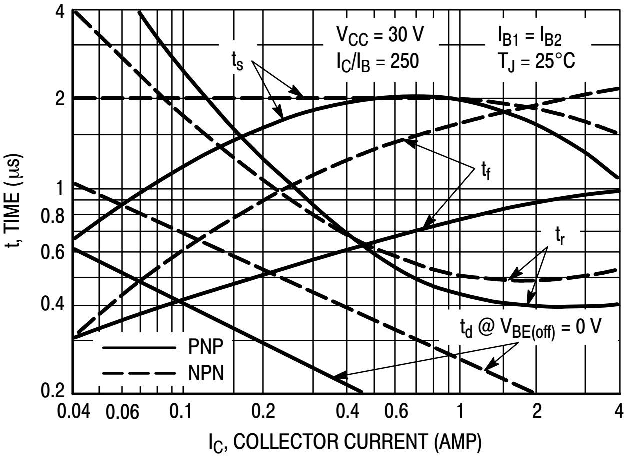


Figure 2. Switching Times

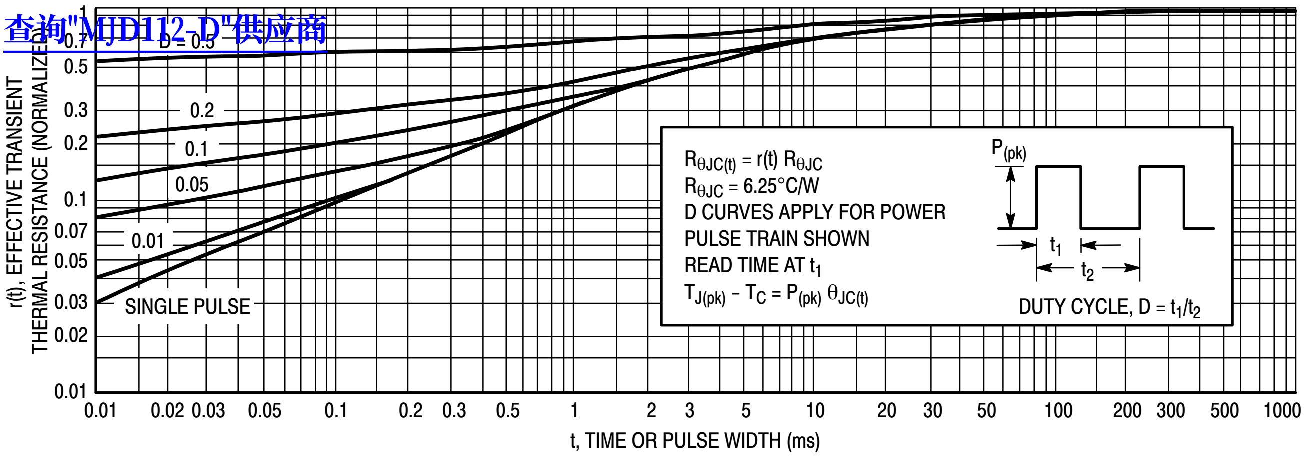


Figure 3. Thermal Response

ACTIVE–REGION SAFE–OPERATING AREA

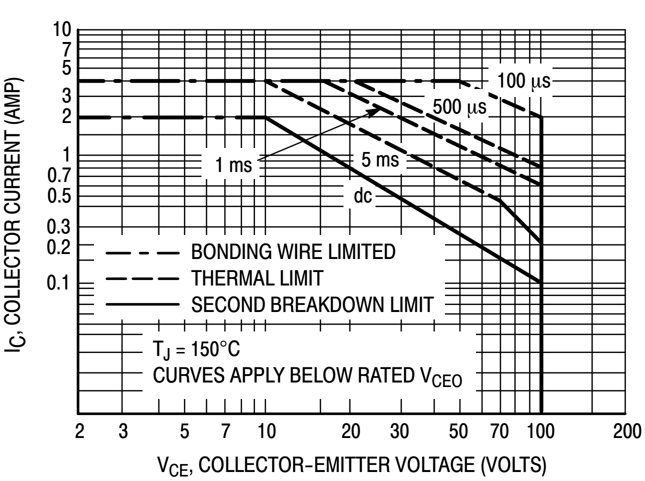


Figure 4. Maximum Rated Forward Biased Safe Operating Area

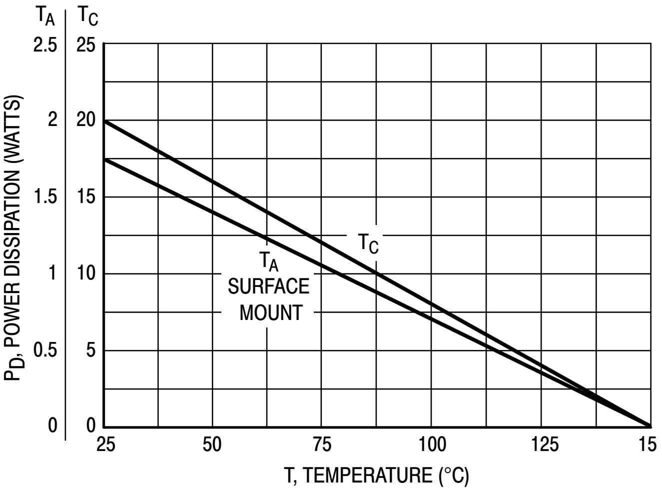


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

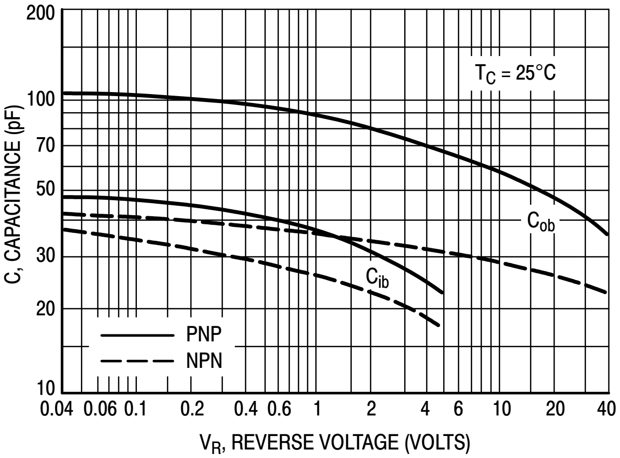


Figure 6. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

NPN MJD112 **PNP MJD117**

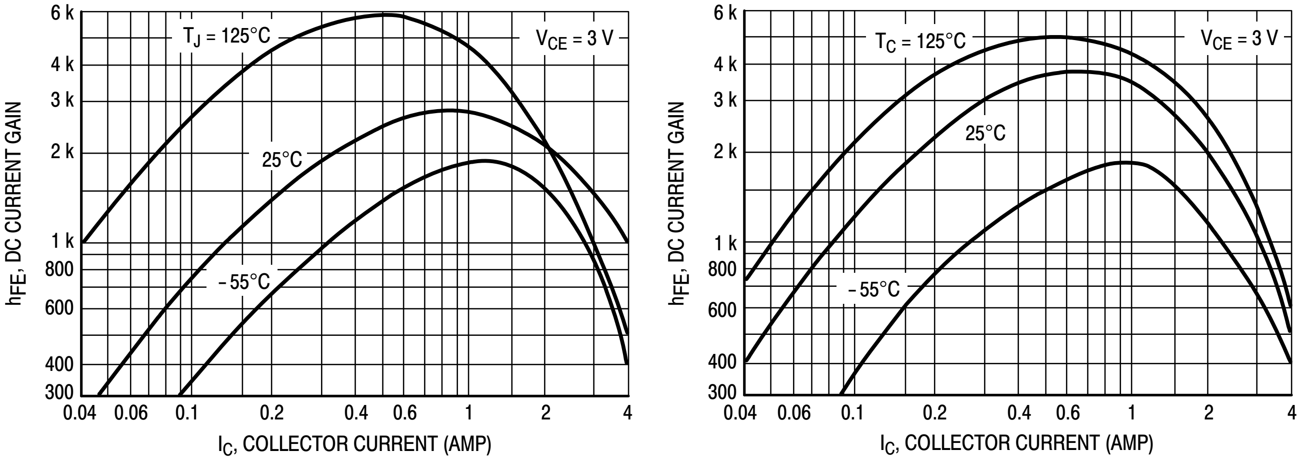


Figure 7. DC Current Gain

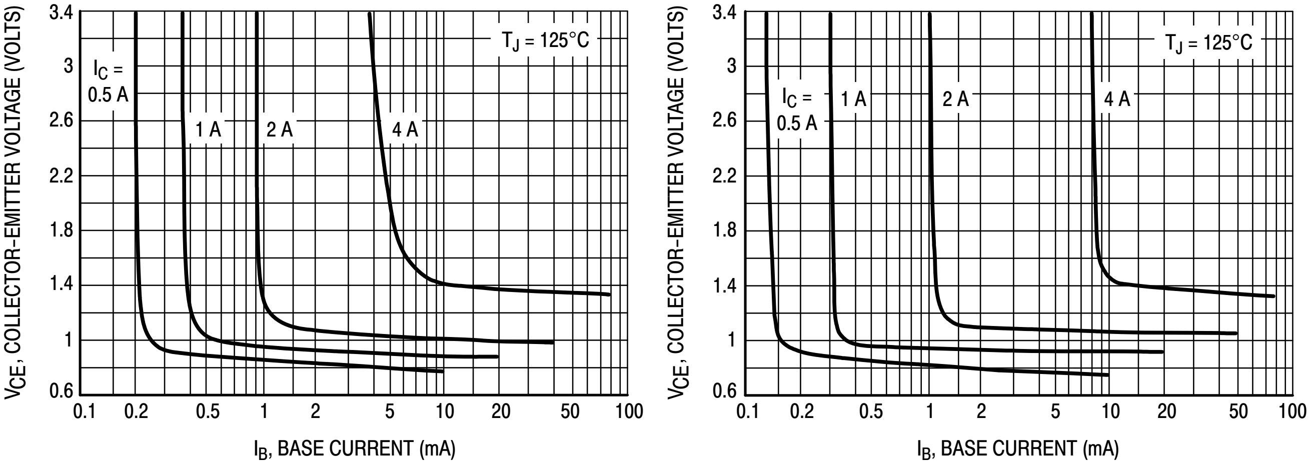


Figure 8. Collector Saturation Region

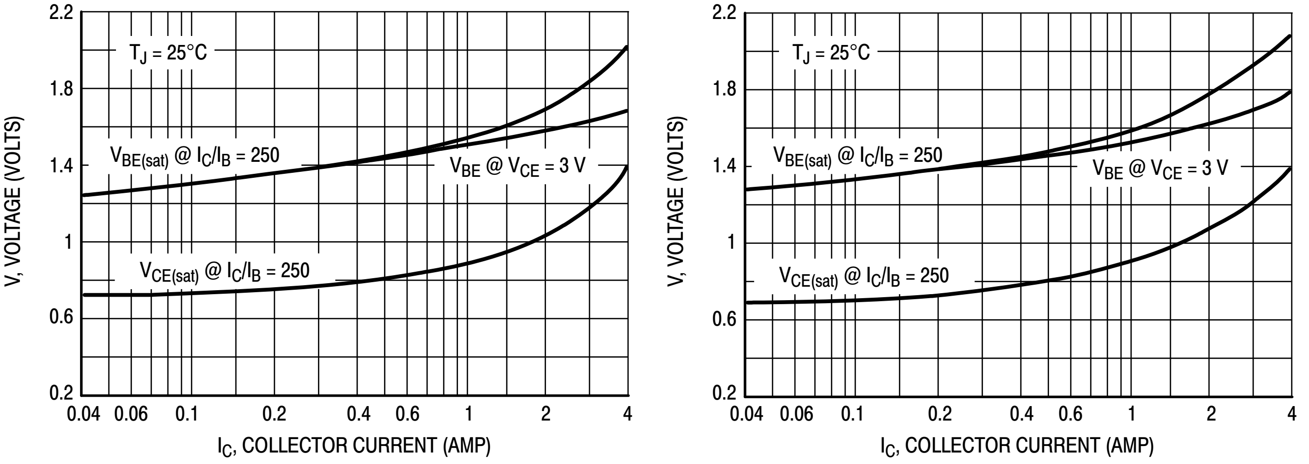


Figure 9. “On Voltages

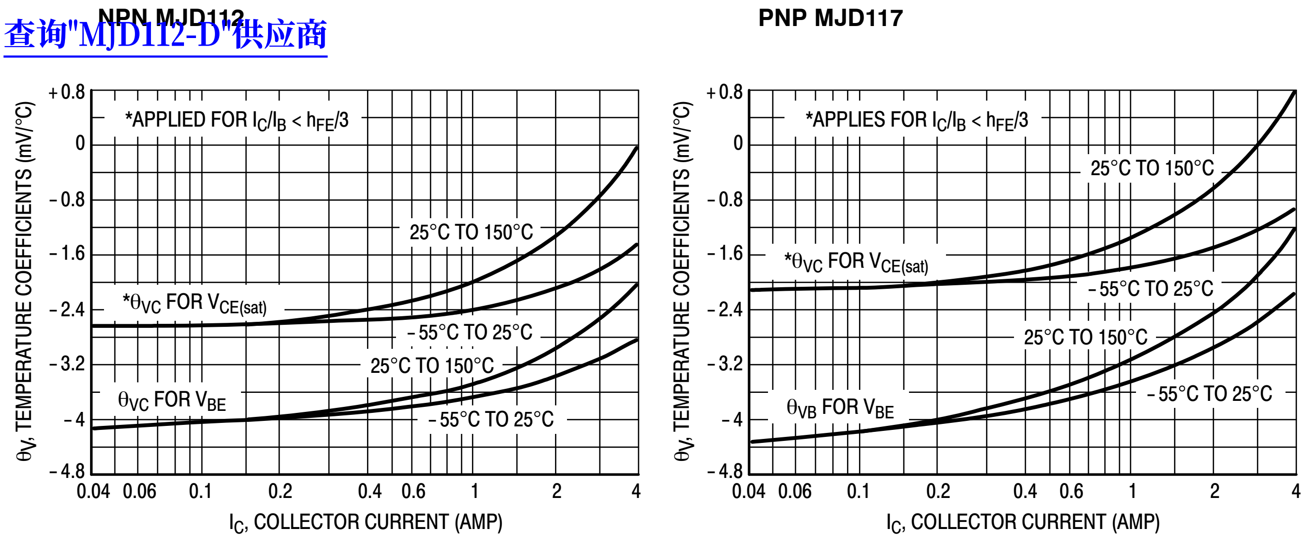


Figure 10. Temperature Coefficients

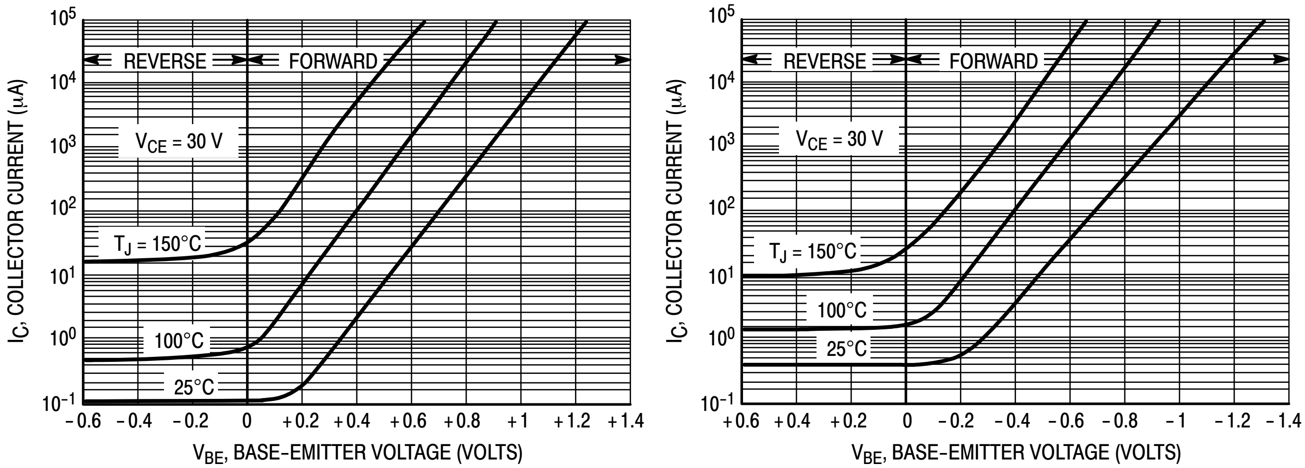


Figure 11. Collector Cut−Off Region

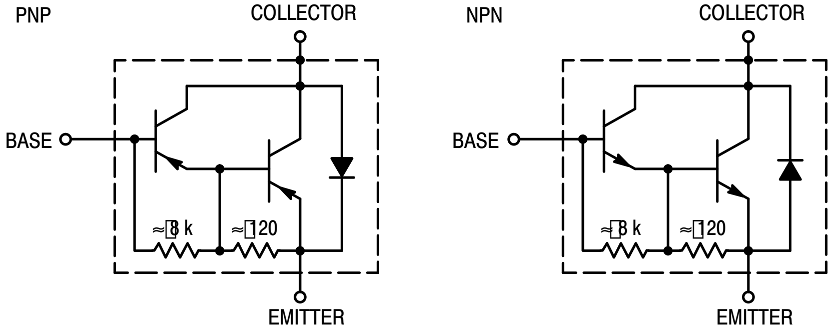


Figure 12. Darlington Schematic

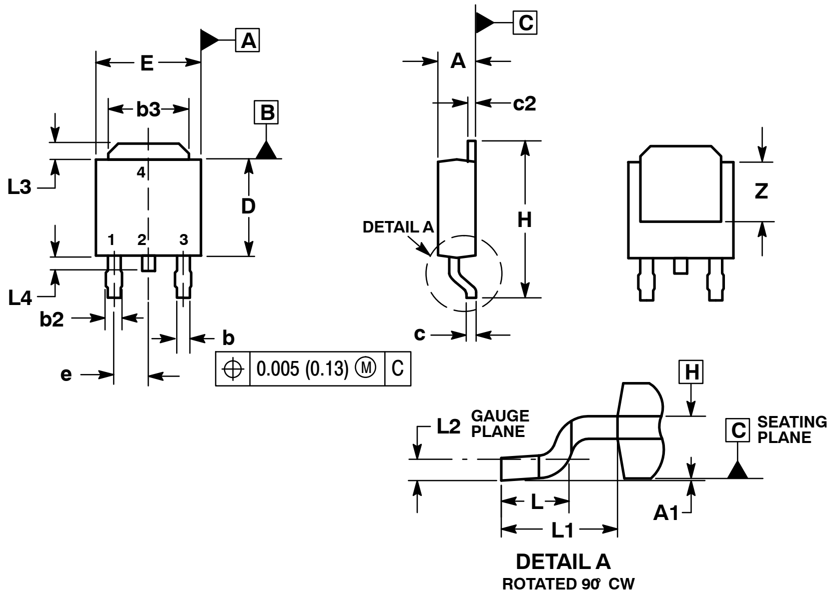
ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD112	DPAK	369C	75 Units / Rail
MJD112G	DPAK (Pb−Free)		
MJD112−001	DPAK−3	369D	
MJD112−1G	DPAK−3 (Pb−Free)		
MJD112RL	DPAK	369C	1800 Tape & Reel
MJD112RLG	DPAK (Pb−Free)		
MJD112T4	DPAK		2500 Tape & Reel
MJD112T4G	DPAK (Pb−Free)		
MJD117	DPAK		75 Units / Rail
MJD117G	DPAK (Pb−Free)		
MJD117−001	DPAK−3	369D	
MJD117−1G	DPAK−3 (Pb−Free)		
MJD117T4	DPAK	369C	2500 Tape & Reel
MJD117T4G	DPAK (Pb−Free)		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK
CASE 369C−01
ISSUE D



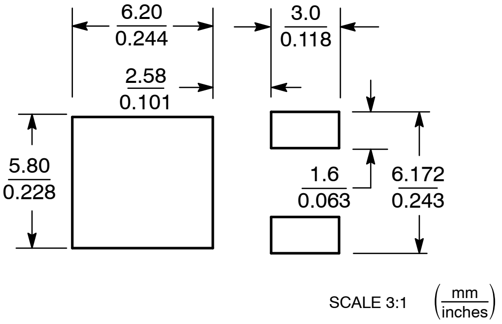
DETAIL A
ROTATED 90° CW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



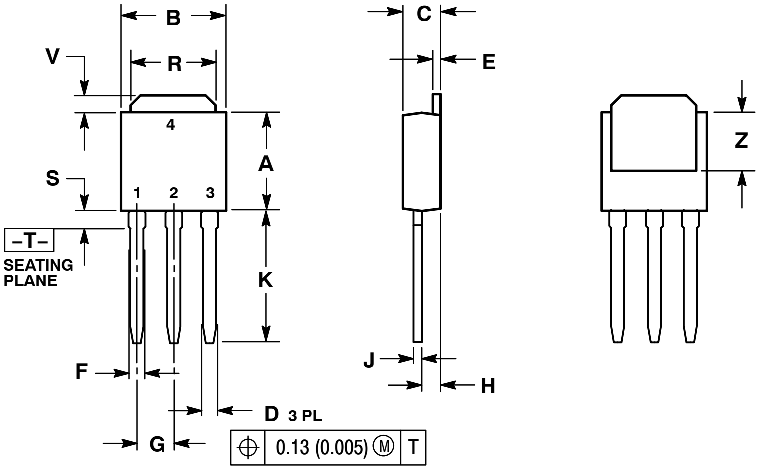
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

查询"MJD112-D"供应商

PACKAGE DIMENSIONS

DPAK−3

CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

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