National Semiconductor

August 1998

54AC109 • 54ACT109
Dual JK̄ Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT109 consists of two high-speed completely independent transition clocked JK̄ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK̄ design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and K̄ inputs together.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

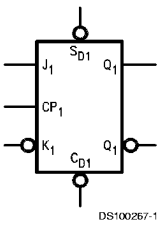
Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- 'ACT109 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC109: 5962-89551
  - — 'ACT109: 5962-88534

Logic Symbol



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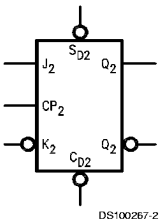

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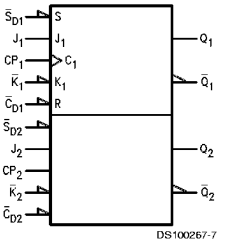
IEEE/IEC



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Pin Names	Description
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

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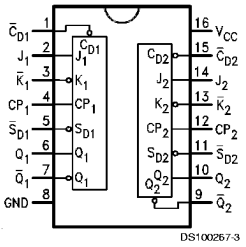
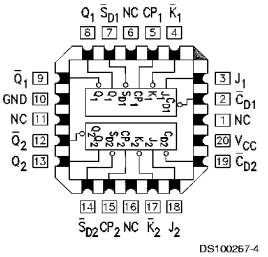
Connection Diagrams

Pin Assignment for DIP and Flatpak



Pin Assignment for LCC



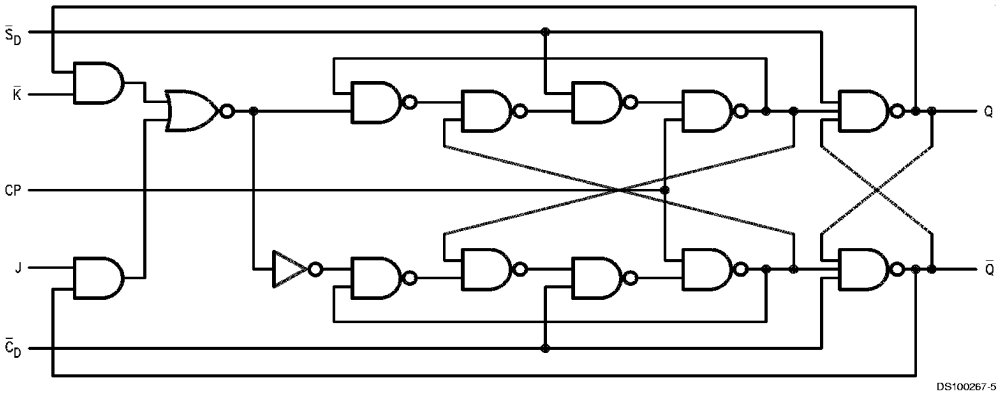
Truth Table

(each half)

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	L	L	L	H
H	H	⌐	H	L	Toggle	
H	H	⌐	L	H	Q_0	$\overline{Q}_0$
H	H	⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
⌐ = LOW-to-HIGH Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous Q_0 ($\overline{Q}_0$) before LOW-to-HIGH Transition of Clock

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 μA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		I_{OH} = −12 mA
		4.5	3.7	V	I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 μA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.5		I_{OL} = 12 mA
		4.5	0.5	V	I_{OL} = 24 mA
		5.5	0.5		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	40.0	µA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
		4.5 5.5	3.70 4.70	V	(Note 5) $V_{IN} = V_{IL}$ or V_{IH} I_{OH} = −24 mA I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5	0.50 0.50	V	(Note 5) $V_{IN} = V_{IL}$ or V_{IH} I_{OL} = 24 mA I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	(Note 6) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	40.0	µA	$V_{IN} = V_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	54AC T_A = −55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	3.3	65		MHz	
		5.0	95			
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	1.0	17.5	ns	
		5.0	1.0	12.0		
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	1.0	13.5	ns	
		5.0	1.0	10.0		
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	1.0	13.0	ns	
		5.0	1.0	9.5		
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	1.0	14.0	ns	
		5.0	1.0	10.5		

Note 8: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC T_A = −55°C to +125°C C_L = 50 pF	Units	Fig. No.
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3	8.0	ns	
		5.0	5.5		
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3	0	ns	
		5.0	0.5		
t_w	Pulse Width $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ or CP_n	3.3	8.0	ns	
		5.0	5.5		
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	3.3	0.5	ns	
		5.0	0.5		

Note 9: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 10)	54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Units
			Min	Max	
f_{max}	Maximum Clock Frequency	5.0	85		MHz
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	14.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	12.0	ns
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	11.5	ns
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	12.5	ns

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

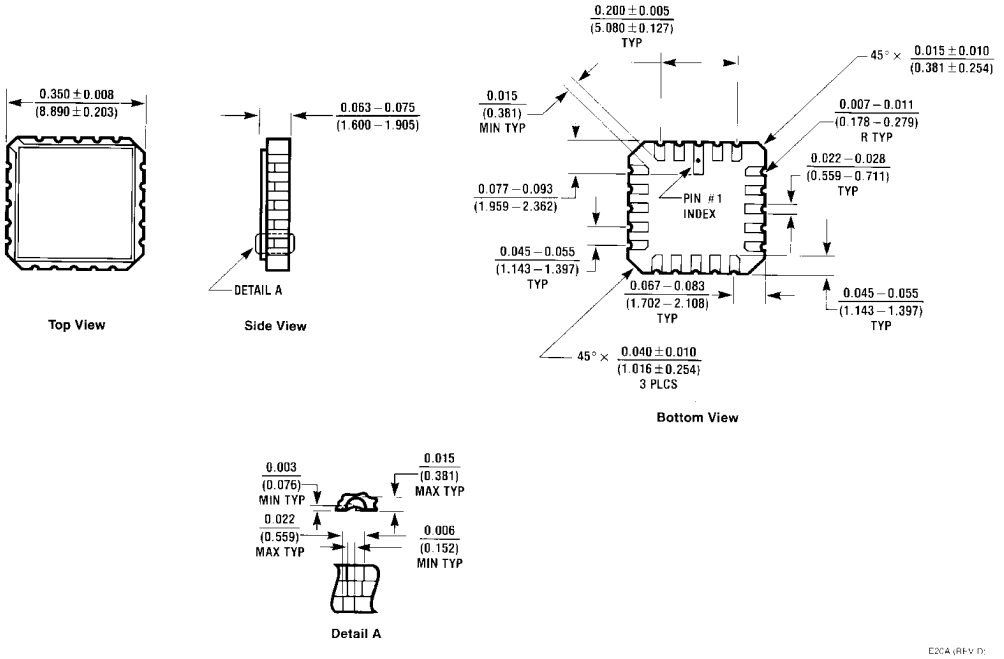
Symbol	Parameter	V_{CC} (V) (Note 11)	54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	Units
			Guaranteed Minimum	
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	2.5	ns
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	2.0	ns
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	5.0	ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	5.0	0.5	ns

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

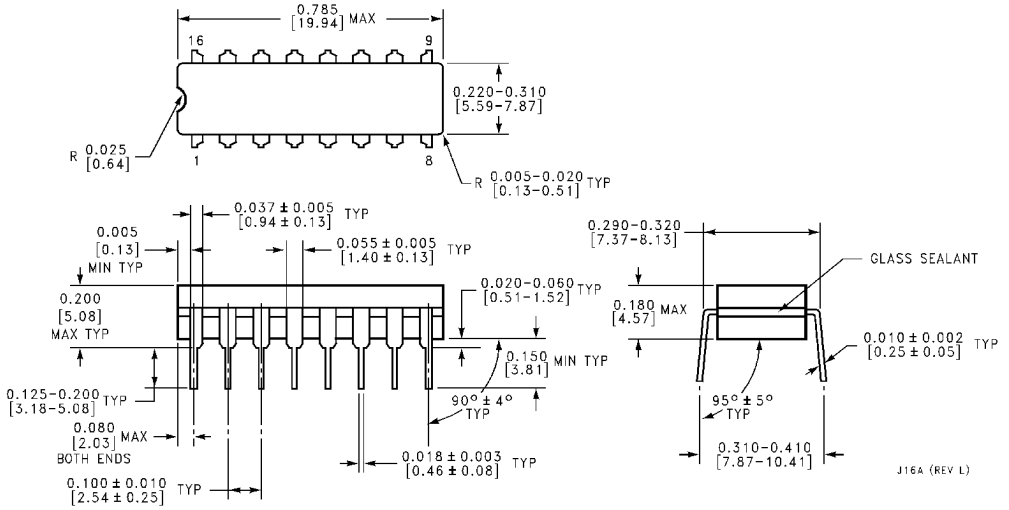
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	35.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

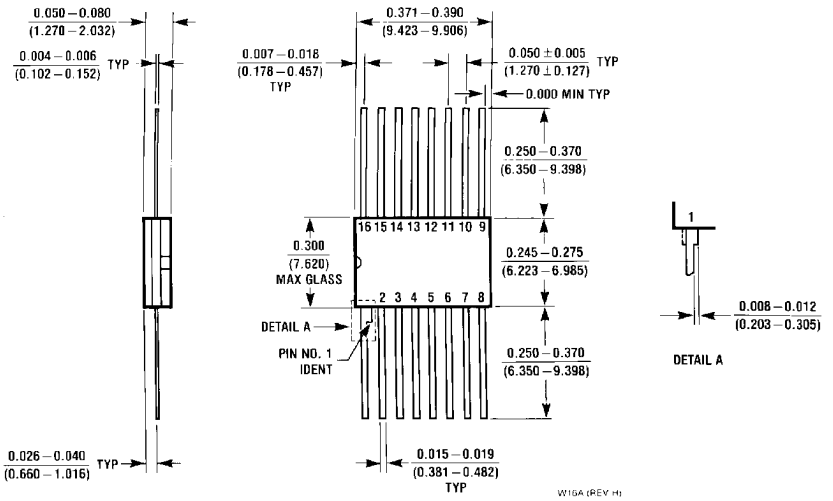


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179