FAIRCHILD

SEMICONDUCTOR ™

October 1995
Revised April 2001

74LCX16841
Low Voltage 20-Bit Transparent Latch
with 5V Tolerant Inputs and Outputs

General Description

The LCX16841 contains twenty non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The LCX16841 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16841 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 5.5 ns t_{PD} max (V_{CC} = 3.3V), 20 µA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX16841MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LCX16841MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
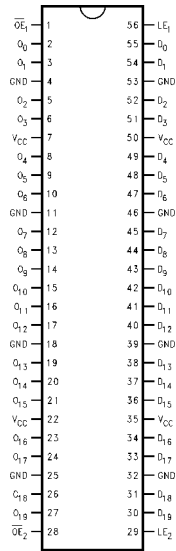
Logic Symbol
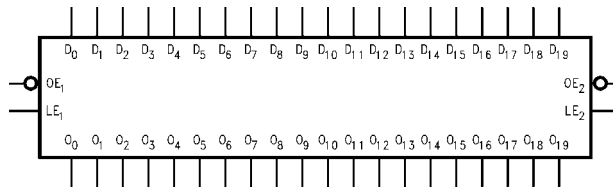
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
D_0–D_{19}	Inputs
O_0–O_{19}	Outputs

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Connection Diagram

$\overline{OE_1}$	1	56	LE_1
O_0	2	55	D_0
O_1	3	54	D_1
GND	4	53	GND
O_2	5	52	D_2
O_3	6	51	D_3
V_{CC}	7	50	V_{CC}
O_4	8	49	D_4
O_5	9	48	D_5
O_6	10	47	D_6
GND	11	46	GND
O_7	12	45	D_7
O_8	13	44	D_8
O_9	14	43	D_9
O_{10}	15	42	D_{10}
O_{11}	16	41	D_{11}
O_{12}	17	40	D_{12}
GND	18	39	GND
O_{13}	19	38	D_{13}
O_{14}	20	37	D_{14}
O_{15}	21	36	D_{15}
V_{CC}	22	35	V_{CC}
O_{16}	23	34	D_{16}
O_{17}	24	33	D_{17}
GND	25	32	GND
O_{18}	26	31	D_{18}
O_{19}	27	30	D_{19}
$\overline{OE_2}$	28	29	LE_2

Truth Tables

Inputs			Outputs
LE_1	$\overline{OE_1}$	D_0–D_9	O_0–O_9
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

| Inputs			Outputs
LE_2	$\overline{OE_2}$	D_{10}–D_{19}	O_{10}–O_{19}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Functional Description

The LCX16841 contains twenty D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE_n}$) input. When $\overline{OE_n}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE_n}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams
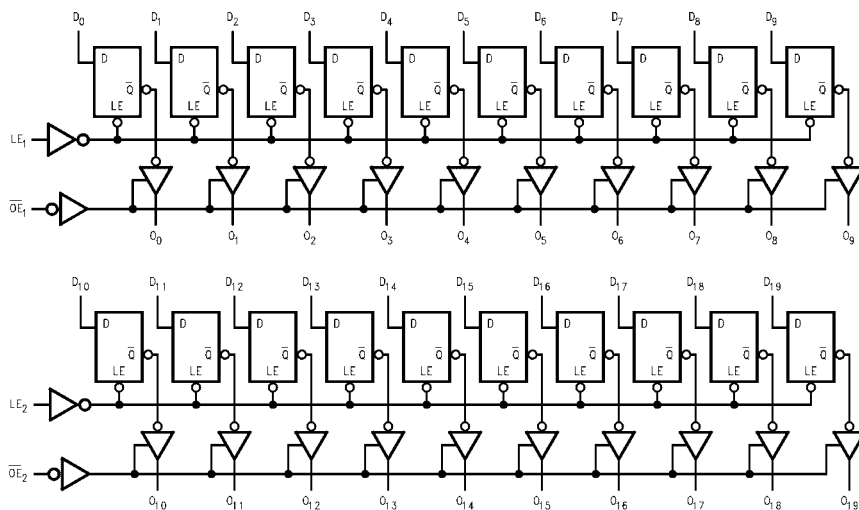
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V – 3.0V		±12	
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
Δt/ΔV	Input Edge Rate, V_{IN} = 0.8V – 2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.3 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 5.5V, V_I = V_{IH} or V_{IL}	2.3 – 3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	µA

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Sidebar: 74LCX16841

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μA
		$3.6V \leq V_I, V_O \leq 5.5V$ (Note 5)	2.3 – 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} -0.6V$	2.3 – 3.6		500	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$

Symbol	Parameter	$V_{CC} = 3.3V \pm 0.3V$ $C_L = 50$ pF Min	Max	$V_{CC} = 2.7V$ $C_L = 50$ pF Min	Max	$V_{CC} = 2.5V \pm 0.2V$ $C_L = 30$ pF Min	Max	Units
t_{PHL}	Propagation Delay	1.5	5.5	1.5	6.0	1.5	6.6	ns
t_{PLH}	D_n to O_n	1.5	5.5	1.5	6.0	1.5	6.6	
t_{PHL}	Propagation Delay	1.5	5.5	1.5	6.5	1.5	6.6	ns
t_{PLH}	LE to O_n	1.5	5.5	1.5	6.5	1.5	6.6	
t_{PZL}	Output Enable Time	1.5	6.5	1.5	7.0	1.5	8.5	ns
t_{PZH}		1.5	6.5	1.5	7.0	1.5	8.5	
t_{PLZ}	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
t_{PHZ}		1.5	6.5	1.5	7.0	1.5	7.8	
t_{OSHL}	Output to Output Skew (Note 6)		1.0					ns
t_{OSLH}			1.0					
t_S	Setup Time, D_n to LE	2.5		2.5		3.0		ns
t_H	Hold Time, D_n to LE	1.5		1.5		2.0		ns
t_W	LE Pulse Width	3.3		3.3		3.8		ns

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_CC (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

"74LCX16841MEAX"

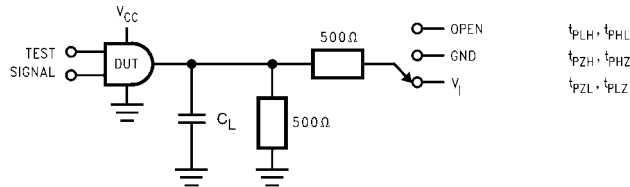## AC LOADING and WAVEFORMS Generic for LCX Family

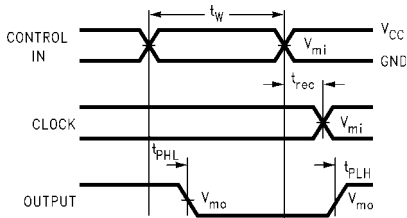**FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)**

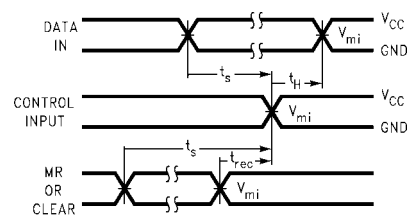| Test	Switch
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V
t$_{PZH}$, t$_{PHZ}$	GND
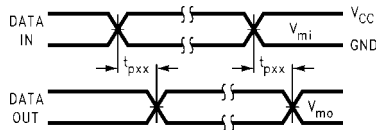
Waveform for Inverting and Non-Inverting Functions
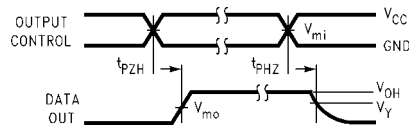
3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t$_{rec}$ Waveforms

Setup Time, Hold Time and Recovery Time for Logic
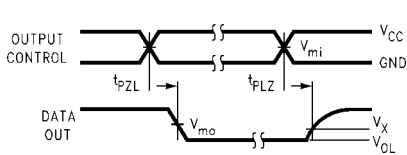
3-STATE Output Low Enable and Disable Times for Logic

t$_{rise}$ and t$_{fall}$
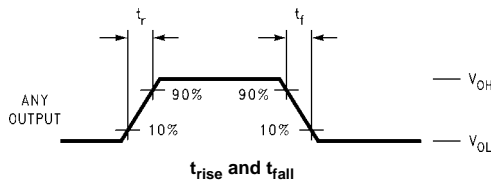
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_r$ = t$_f$ = 3ns)

Symbol	V$_{CC}$		
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

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Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

74LCX16841 Low Voltage 20-Bit Transparent Latch with 5V Tolerant Inputs and Outputs
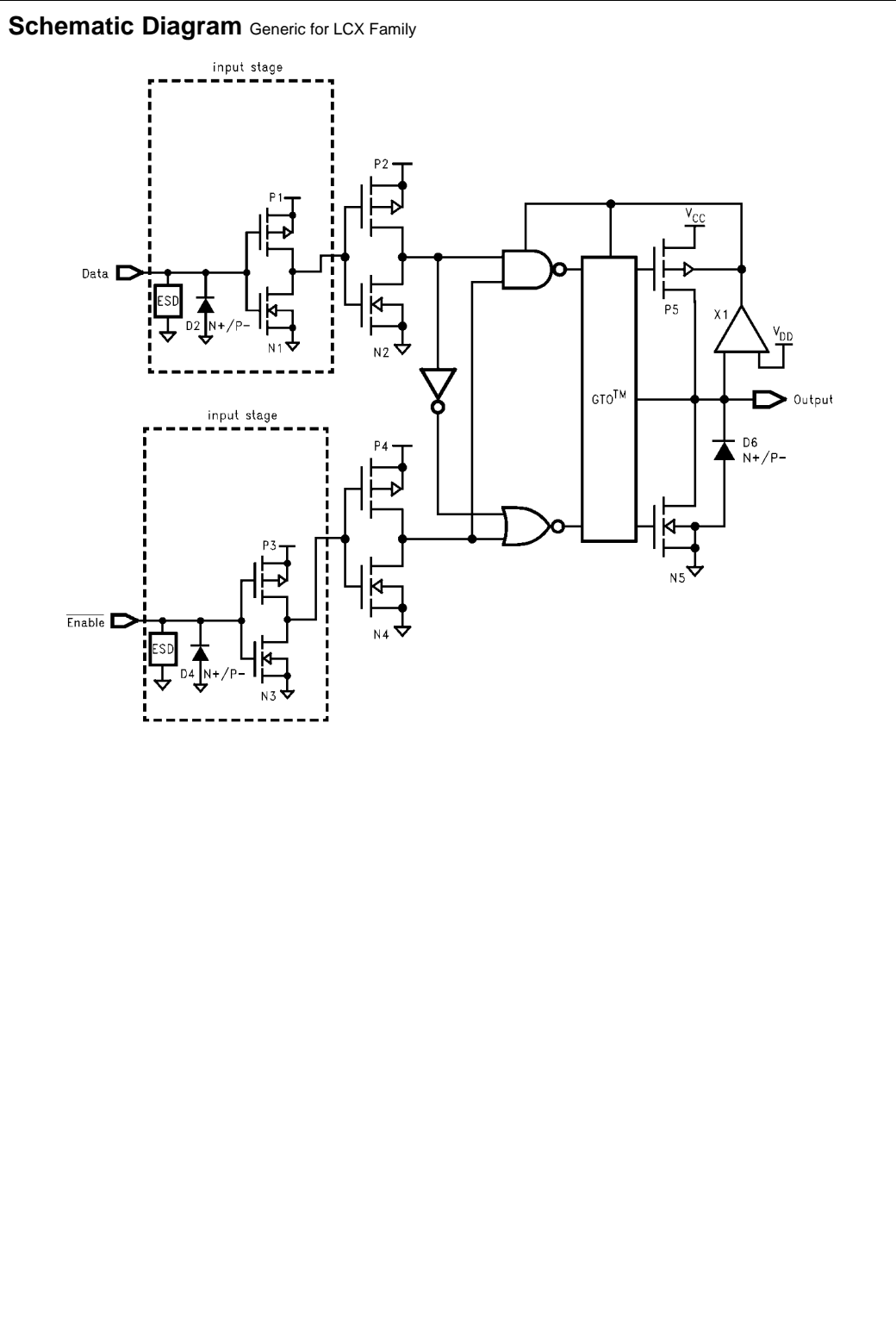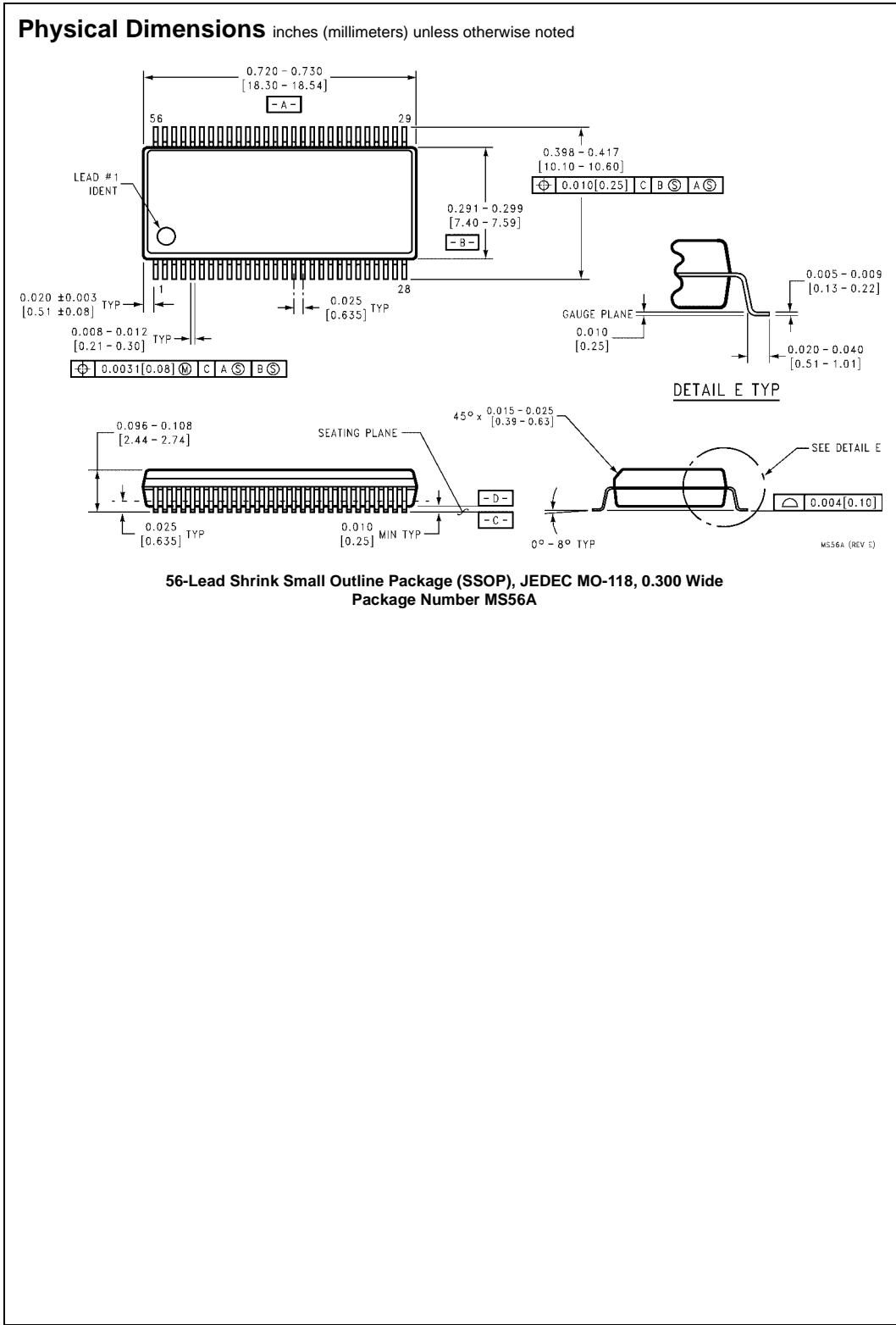
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

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