



May 1988
Revised August 1999

74F374

Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The 74F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

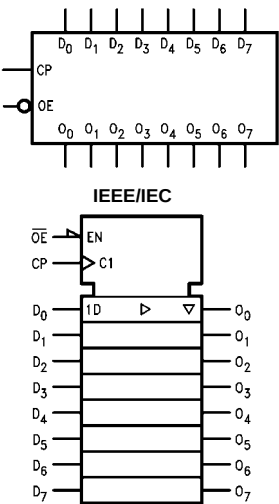
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Ordering Code:

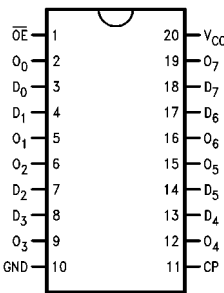
Order Number	Package Number	Package Description
74F374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F374MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F374PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



74F374 Octal D-Type Flip-Flop with 3-STATE Outputs

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Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D ₀ –D ₇	Data Inputs	1.0/1.0	20 μ A/–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/–0.6 mA
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
O ₀ –O ₇	3-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

Functional Description

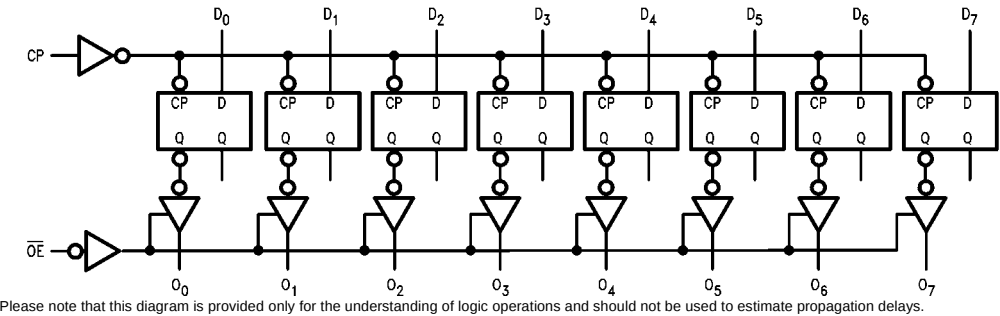
The 74F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affected the state of the flip-flops.

Truth Table

Inputs			Internal	Output
D _n	CP	$\overline{OE}$	Register	O _n
H		L	H	H
L		L	L	L
X	X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
 = LOW-to-HIGH Clock Transition

Logic Diagram



Absolute Maximum Ratings ^(Note 1)				Recommended Operating Conditions			
Storage Temperature		-65°C to +150°C		Free Air Ambient Temperature		0°C to +70°C	
Ambient Temperature under Bias		-55°C to +125°C		Supply Voltage		+4.5V to +5.5V	
Junction Temperature under Bias		-55°C to +150°C					
V _{CC} Pin Potential to Ground Pin		-0.5V to +7.0V					
Input Voltage (Note 2)		-0.5V to +7.0V					
Input Current (Note 2)		-30 mA to +5.0 mA					
Voltage Applied to Output							
in HIGH State (with V _{CC} = 0V)							
Standard Output		-0.5V to V _{CC}					
3-STATE Output		-0.5V to +5.5V					
Current Applied to Output							
in LOW State (Max)		twice the rated I _{OL} (mA)					
ESD Last Passing Voltage (Min)		4000V					
Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied. Note 2: Either voltage limit or current limit is sufficient to protect inputs.							
DC Electrical Characteristics							
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current		55	86	mA	Max	V _O = HIGH Z

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AC Electrical Characteristics									
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	140		60		70		MHz
t _{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns
t _{PHL}	CP to O _n	4.0	6.5	8.5	4.0	11.0	4.0	10.0	
t _{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	ns
t _{PZL}		2.0	5.8	7.5	2.0	10.0	2.0	8.5	
t _{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	
t _{PLZ}		1.5	4.3	5.5	1.5	7.5	1.5	6.5	
AC Operating Requirements									
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units	
		Min	Max	Min	Max	Min	Max		
t _S (H)	Setup Time, HIGH or LOW	2.0		2.5		2.0		ns	
t _S (L)	D _n to CP	2.0		2.0		2.0			
t _H (H)	Hold Time, HIGH or LOW	2.0		2.0		2.0			
t _H (L)	D _n to CP	2.0		2.5		2.0			
t _W (H)	CP Pulse Width	7.0		7.0		7.0		ns	
t _W (L)	HIGH or LOW	6.0		6.0		6.0			

Technical drawing of a rectangular component with dimensions and lead locations. The drawing shows a rectangular body with a semi-circular feature on the left side. Dimensions are provided for the overall width and height, and for the semi-circular feature. Lead locations are indicated by numbered circles (1 through 10) around the perimeter. A 30° angle is specified for the lead location on the right side. The drawing includes the following dimensions and labels:

- Overall width: $0.496 - 0.512$ (12.598 - 13.005)
- Overall height: $0.394 - 0.419$ (10.008 - 10.643)
- Lead NO. 1 IDENT (pointing to a lead location on the left side)
- Lead locations: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 (numbered circles around the perimeter)
- 30° TYP (angle specification for the lead location on the right side)
- 0.010 MAX (0.254) (dimension for the lead location on the right side)

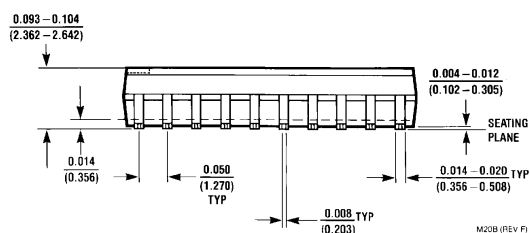
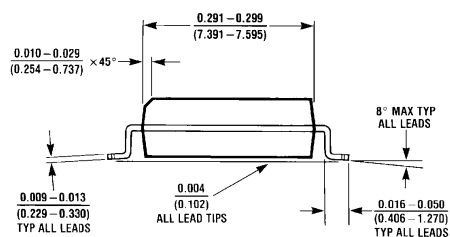
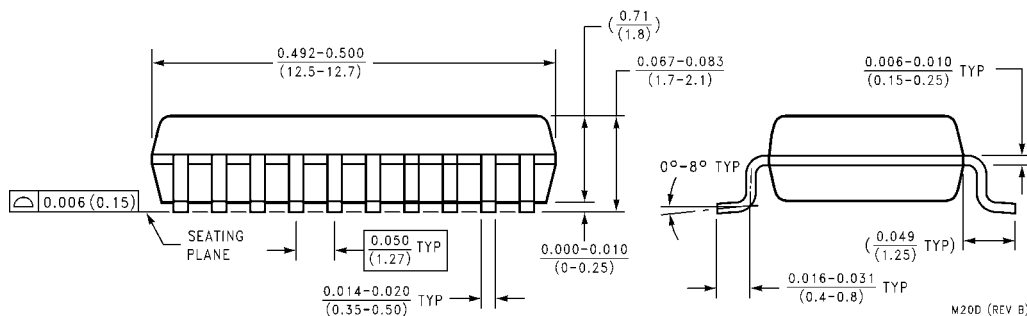


Diagram of a 20-pin DIP package. The package is shown with pins numbered 1 through 20. The dimensions are given in inches and millimeters:

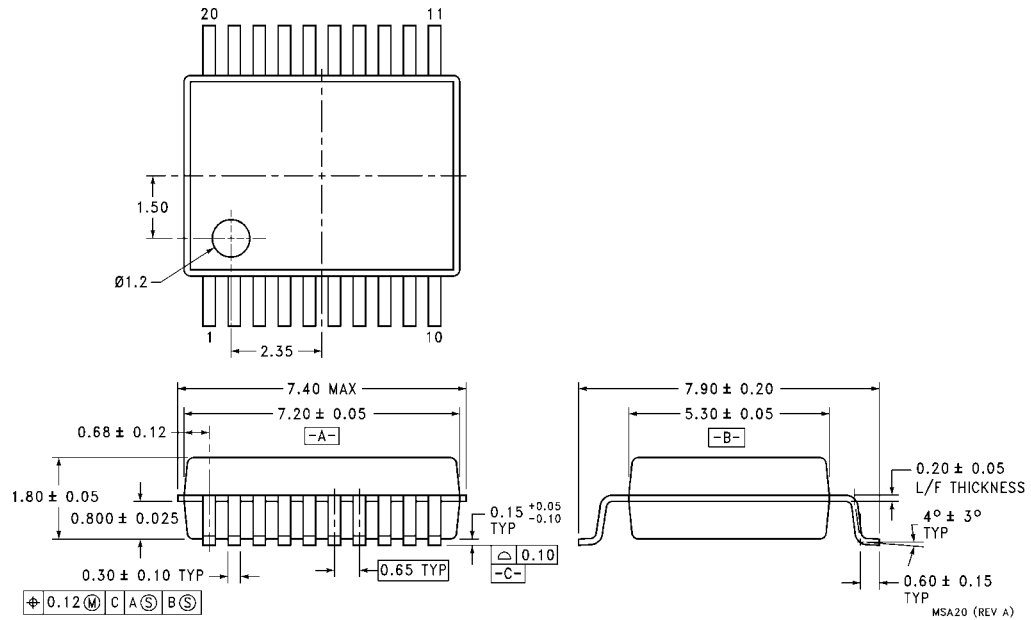
- Pin 1 to Pin 11: 0.295-0.319 (7.5-8.1)
- Pin 12 to Pin 20: 0.205-0.213 (5.2-5.4)



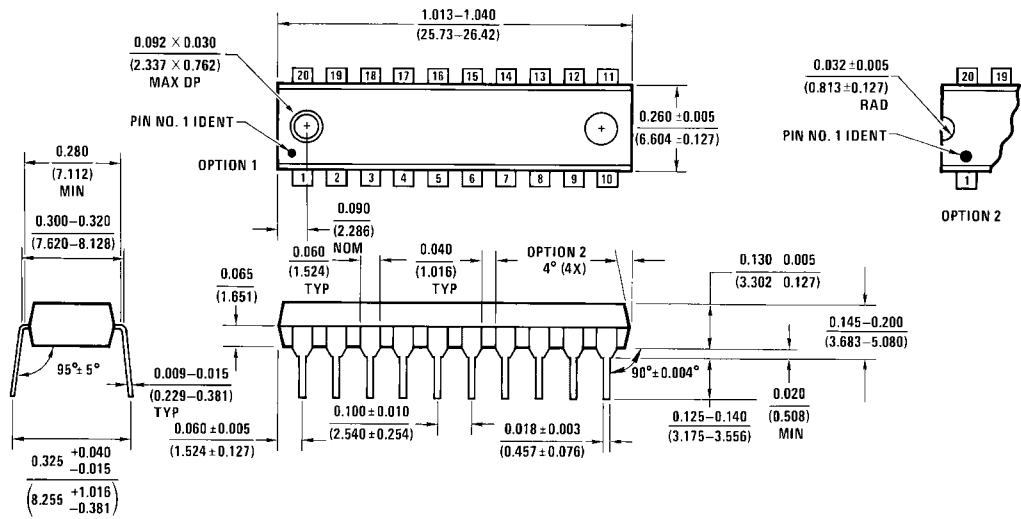
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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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