

## Low Side PWM FET Controller

The CS7054 is a monolithic integrated circuit designed primarily to control the rotor speed of permanent magnet, direct current (DC) brush motors. It drives the gate of an N channel power MOSFET or IGBT with a user-adjustable, fixed frequency, variable duty cycle, pulse width modulated (PWM) signal. The CS7054 can also be used to control other loads such as incandescent bulbs and solenoids. Inductive current from the motor or solenoid is recirculated through an external diode.

The CS7054 accepts a DC level input signal of 0 to 5.0 V to control the pulse width of the output signal. This signal can be generated by a potentiometer referenced to the on-chip 5.0 V linear regulator, or a filtered 0% to 100% PWM signal also referenced to the 5.0 V regulator.

The IC is placed in a sleep state by pulling the CTL lead below 0.5 V. In this mode everything on the chip is shut down except for the on-chip regulator and the overall current draw is less than 275  $\mu$ A. There are a number of on-chip diagnostics that look for potential failure modes and can disable the external power MOSFET.

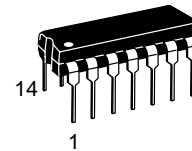
### Features

- 200 mA Peak PWM Gate Drive Output
- Patented Voltage Compensation Circuit
- 100% Duty Cycle Capability
- 5.0 V,  $\pm 3.0\%$  Linear Regulator
- Low Current Sleep Mode
- Overvoltage Protection
- Overcurrent Protection of External MOSFET/IGBT
- Output Inhibit

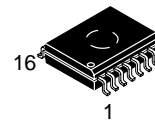


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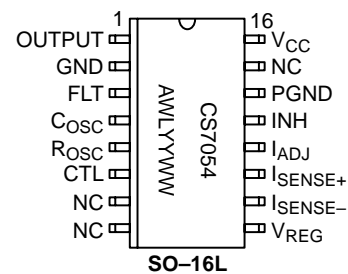
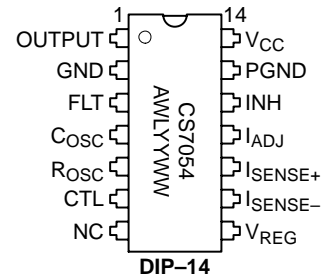


**DIP-14  
N SUFFIX  
CASE 646**



**SO-16L  
DW SUFFIX  
CASE 751G**

### PIN CONNECTIONS AND MARKING DIAGRAMS



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
CS7054YN14	DIP-14	25 Units/Rail
CS7054YDW16	SO-16L	46 Units/Rail
CS7054YDWR16	SO-16L	1000 Tape & Reel

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Rating	Value	Unit
Storage Temperature	−65 to 150	°C
V <sub>CC</sub>	−0.3 to 30	V
Supply Voltage Range (Load Dump = 26 V w/Series 51 Ω Resistor) V <sub>CC</sub> Peak Transient Voltage	40	V
Input Voltage Range (at any input)	−0.3 to 10	V
Maximum Junction Temperature	150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1. Reflow (SMD styles only) Note 2.	260 peak 230 peak °C

- \*The maximum package power dissipation must be observed.

# CS7054

## ELECTRICAL CHARACTERISTICS (8.0 V < V<sub>CC</sub> < 16 V; -40°C < T<sub>A</sub> < 125°C; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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### V<sub>CC</sub> Supply

Operating Current Supply	–	–	5.0	10	mA
Quiescent Current	V <sub>CC</sub> = 12 V	–	170	275	μA
Overvoltage Shutdown	–	18	19.5	21	V
Overvoltage Hysteresis	–	150	325	500	mV

### Control (CTL)

Control Input Current	CTL = 0 V to 5.0 V	–2.0	0.1	2.0	μA
Sleep Mode Threshold	–	8.0	10	12	% V <sub>REG</sub>
Sleep Mode Hysteresis	–	50	100	150	mV

### Current Sense

Differential Voltage Sense	I <sub>ADJ</sub> = 51.2% V <sub>REG</sub> and R <sub>CS1</sub> = 51 Ω	60.5	–	79.5	mV
I <sub>ADJ</sub> Input Current	I <sub>ADJ</sub> = 0 V to 5.0 V	–5.0	0.3	2.0	μA

### Linear Regulator

Output Voltage	V <sub>CC</sub> = 13.2 V	4.85	5.00	5.15	V
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### Inhibit

Inhibit Threshold	–	40	50	60	% V <sub>REG</sub>
Inhibit Hysteresis	–	150	325	575	mV

### External Drive (OUTPUT)

Output Frequency	R <sub>OSC</sub> = 105 kΩ, C <sub>OSC</sub> = 390 pF	17	20	23	kHz
Voltage to Duty Cycle Conversion	V <sub>CC</sub> = 13 V, CTL = 30% V <sub>REG</sub>	26.3	–	38.5	%
	V <sub>CC</sub> = 13 V, CTL = 70% V <sub>REG</sub>	69.5	–	81.5	%
Output Rise Time	V <sub>CC</sub> = 13 V, R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	–	0.25	1.0	μs
Output Fall Time	V <sub>CC</sub> = 13 V, R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	–	0.3	1.0	μs
Output Sink Current	V <sub>CC</sub> = 13 V, R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	–	400	–	mA
Output Source Current	V <sub>CC</sub> = 13 V, R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	–	400	–	mA
Output High Voltage	I <sub>OUT</sub> = 1.0 mA	V <sub>CC</sub> – 1.7	–	–	V
Output Low Voltage	I <sub>OUT</sub> = –1.0 mA	–	–	1.3	V

# CS7054

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## PACKAGE PIN DESCRIPTION

PACKAGE PIN #		PIN SYMBOL	FUNCTION
DIP-14	SO-16L		
1	1	OUTPUT	MOSFET Gate Drive.
2	2	GND	Ground.
3	3	FLT	Fault time out capacitor.
4	4	COSC	Oscillator capacitor.
5	5	ROSC	Oscillator resistor.
6	6	CTL	Pulse width control input.
7	7, 8, 15	NC	No connection.
8	9	VREG	5.0 V linear regulator.
9	10	I <sub>SENSE-</sub>	Current sense minus.
10	11	I <sub>SENSE+</sub>	Current sense plus.
11	12	I <sub>ADJ</sub>	Current limit adjust.
12	13	INH	Output Inhibit.
13	14	PGND	Power ground for on chip clamp.
14	16	V <sub>CC</sub>	Positive power supply input.

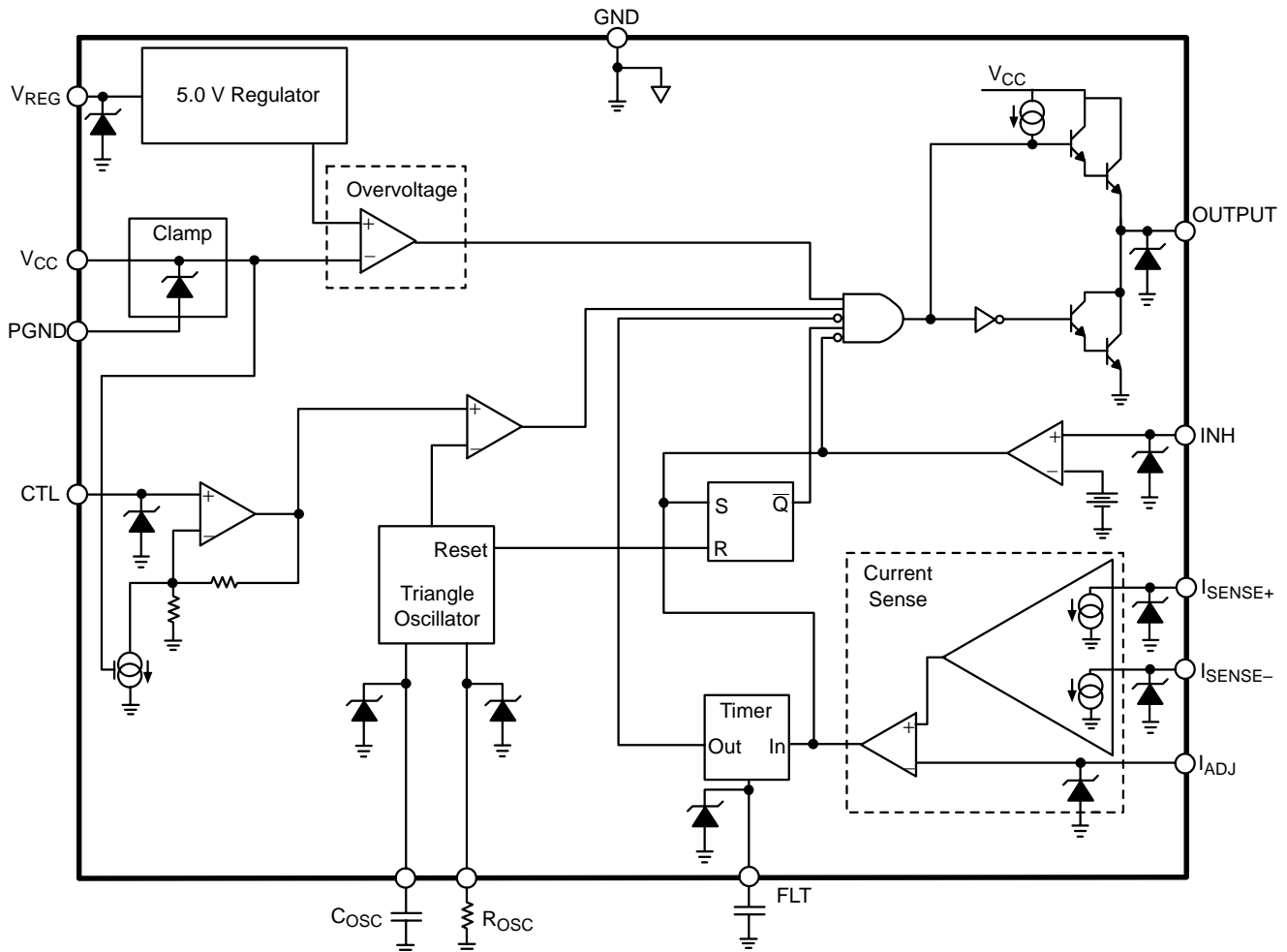


Figure 2. Block Diagram

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# TYPICAL PERFORMANCE CHARACTERISTICS

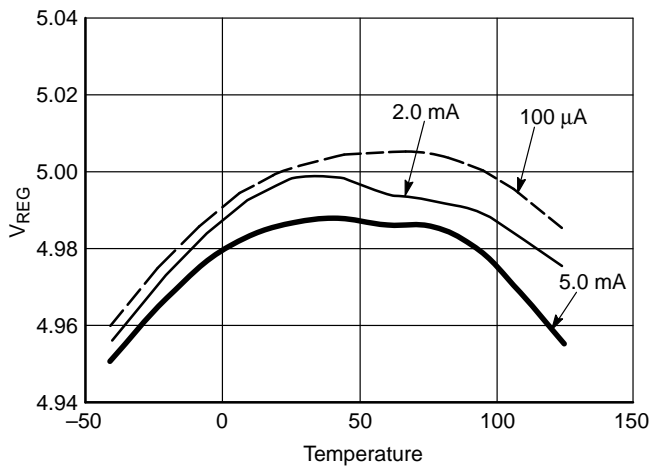


Figure 3.  $V_{REG}$  vs. Temperature @  $V_{CC} = 8.0\text{ V}$

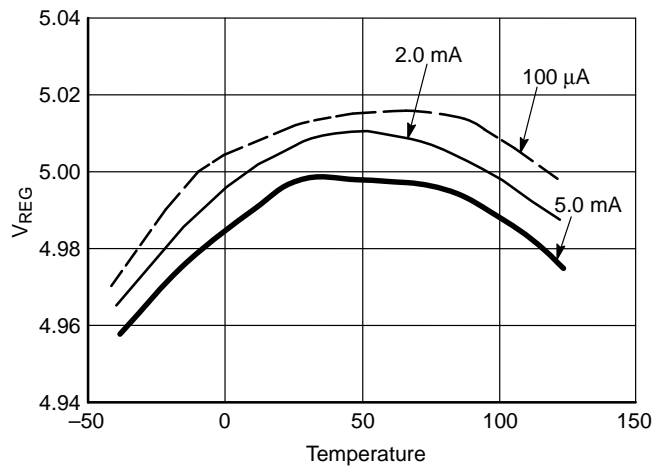


Figure 4.  $V_{REG}$  vs. Temperature @  $V_{CC} = 12\text{ V}$

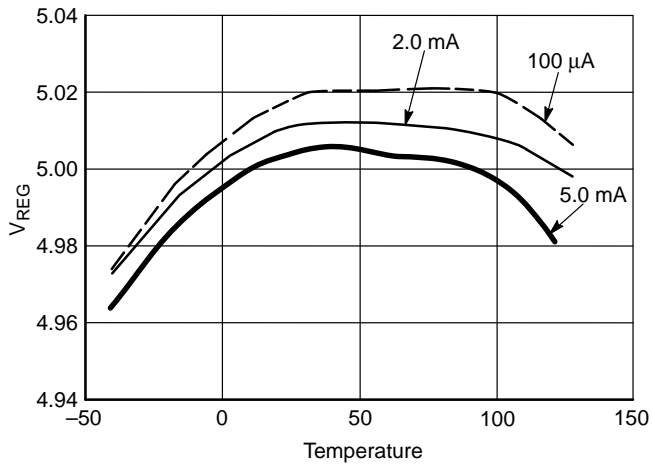


Figure 5.  $V_{REG}$  vs. Temperature @  $V_{CC} = 16\text{ V}$

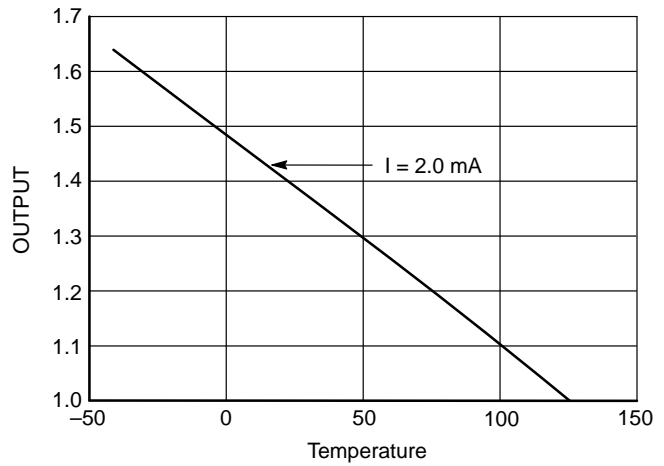


Figure 6. OUTPUT Saturation Voltage (Sourcing Current) vs Temperature

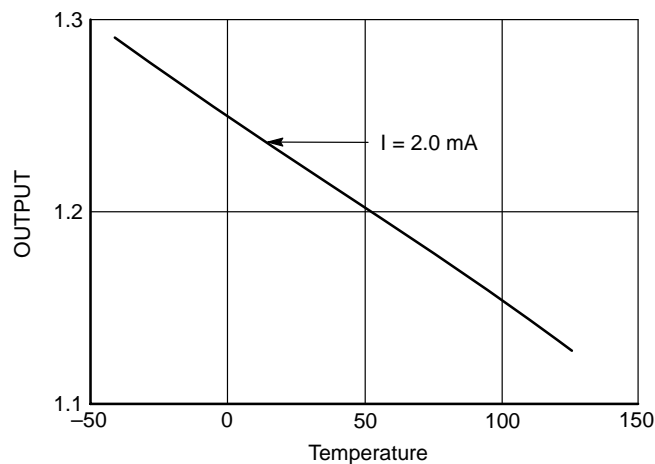


Figure 7. OUTPUT Voltage (Sinking Current) vs Temperature

## THEORY OF OPERATION

## Oscillator

The IC sets up a constant frequency triangle wave at the C<sub>OSC</sub> lead whose frequency is determined by the external components R<sub>OSC</sub> and C<sub>OSC</sub> by the following equation:

$$\text{Frequency} = \frac{0.83}{R_{OSC} \times C_{OSC}}$$

The peak and valley of the triangle wave are proportional to V<sub>CC</sub> by the following:

$$V_{VALLEY} = 0.2 \times V_{CC}$$

$$V_{PEAK} = 0.8 \times V_{CC}$$

This is required to make the voltage compensation function properly. In order to keep the frequency of the oscillator constant the current that charges C<sub>OSC</sub> must also vary with supply. R<sub>OSC</sub> sets up the current which charges C<sub>OSC</sub>. The voltage across R<sub>OSC</sub> is 50% of V<sub>CC</sub> and therefore:

$$I_{ROSC} = 0.5 \times \frac{V_{CC}}{R_{OSC}}$$

I<sub>ROSC</sub> is multiplied by two (2) internally and transferred to the C<sub>OSC</sub> lead. Therefore:

$$I_{COSC} = \pm \frac{V_{CC}}{R_{OSC}}$$

The period of the oscillator is:

$$T = 2C_{OSC} \times \frac{V_{PEAK} - V_{VALLEY}}{I_{COSC}}$$

The R<sub>OSC</sub> and C<sub>OSC</sub> components can be varied to create frequencies over the range of 15 Hz to 25 kHz. With the suggested values of 105 kΩ and 390 pF for R<sub>OSC</sub> and C<sub>OSC</sub> respectively, the nominal frequency will be approximately 20 kHz. I<sub>ROSC</sub>, at V<sub>CC</sub> = 14 V, will be 66.7 μA. I<sub>ROSC</sub> should not change over a more than 2:1 ratio and therefore C<sub>OSC</sub> should be changed to adjust the oscillator frequency.

## Voltage Duty Cycle Conversion

The IC translates an input voltage at the CTL lead into a duty cycle at the OUTPUT lead. The transfer function incorporates ON Semiconductor's patented Voltage Compensation method to keep the average voltage and current across the load constant regardless of fluctuations in the supply voltage. The duty cycle is varied based upon the input voltage and supply voltage by the following equation:

$$\text{Duty Cycle} = 100\% \times \frac{2.8 \times V_{CTL}}{V_{CC}}$$

An internal DC voltage equal to:

$$V_{DC} = (1.683 \times V_{CTL}) + V_{VALLEY}$$

is compared to the oscillator voltage to produce the compensated duty cycle. The transfer is set up so that at V<sub>CC</sub> = 14 V the duty will equal V<sub>CTL</sub> divided by V<sub>REG</sub>. For example at V<sub>CC</sub> = 14 V, V<sub>REG</sub> = 5.0 V and V<sub>CTL</sub> = 2.5 V, the duty cycle would be 50% at the output. This would place a 7.0 V average voltage across the load. If V<sub>CC</sub> then drops to 10 V, the IC would change the duty cycle to 70% and hence keep the average load voltage at 7.0 V.

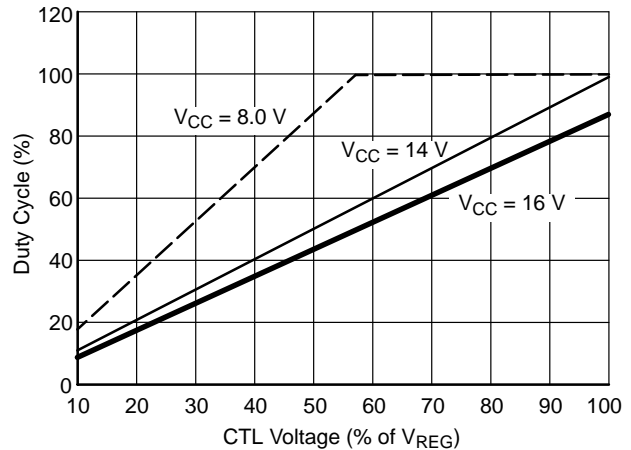


Figure 8. Voltage Compensation

## 5.0 V Linear Regulator

There is a 5.0 V, 5.0 mA linear regulator available at the V<sub>REG</sub> lead for external use. This voltage acts as a reference for many internal and external functions. It has a drop out of approximately 1.5 V at room temperature and does not require an external capacitor for stability.

## Current Sense and Timer

The IC differentially monitors the load current on a cycle by cycle basis at the I<sub>SENSE+</sub> and I<sub>SENSE-</sub> leads. The differential voltage across these two leads is amplified internally and compared to the voltage at the I<sub>ADJ</sub> lead. The gain, A<sub>V</sub>, is set internally and externally by the following equation:

$$A_V = \frac{V_{I(ADJ)}}{I_{SENSE+} - I_{SENSE-}} = \frac{37000}{1000 + R_{CS}}$$

The current limit (I<sub>LIM</sub>) is set by the external current sense resistor (R<sub>SENSE</sub>) placed across the I<sub>SENSE+</sub> and I<sub>SENSE-</sub> terminals and the voltage at the I<sub>ADJ</sub> lead.

$$I_{LIM} = \frac{1000 + R_{CS}}{37000} \times \frac{V_{I(ADJ)}}{R_{SENSE}}$$

The R<sub>CS</sub> resistors and C<sub>CS</sub> components form a differential low pass filter which filters out high frequency noise generated by the switching of the external MOSFET and the associated lead noise. R<sub>CS</sub> also forms an error term in the gain of the I<sub>LIM</sub> equation because the I<sub>SENSE+</sub> and I<sub>SENSE-</sub>

leads are low impedance inputs thereby creating a good current sensing amplifier. Both leads source 50  $\mu\text{A}$  while the chip is in run mode.  $R_{CS}$  should be much less than 1000  $\Omega$  to minimize error in the  $I_{LIM}$  equation.  $I_{ADJ}$  should be biased between 1.0 V and 4.0 V.

When the current through the external MOSFET exceeds  $I_{LIM}$ , an internal latch is set and the output pulls the gate of the MOSFET low for the remainder of the oscillator cycle (fault mode). At the start of the next cycle, the latch is reset and the IC reverts back to run mode until another fault occurs. If a number of faults occur in a given period of time, the IC “times out” and disables the MOSFET for a long period of time to let it cool off. This is accomplished by charging the  $C_{FLT}$  capacitor each time an over current condition occurs. If a cycle goes by with no overcurrent fault occurring, an even smaller amount of charge will be removed from  $C_{FLT}$ . If enough faults occur together, eventually  $C_{FLT}$  will charge up to 2.4 V and the fault latch will be set. The fault latch will not be reset until the  $C_{FLT}$  discharges to 0.6 V. This action will continue indefinitely if the fault persists.

The off time and on time are set by the following:

$$\text{Off Time} = C_{FLT} \times \frac{2.4 \text{ V} - 0.6 \text{ V}}{4.5 \mu\text{A}}$$

$$\text{On Time} = C_{FLT} \times \frac{2.4 \text{ V} - 0.6 \text{ V}}{I_{AVG}}$$

where:

$$I_{AVG} = (295.5 \mu\text{A} \times \text{DC}) - [4.5 \mu\text{A} \times (1 - \text{DC})]$$

$$I_{AVG} = (300 \mu\text{A} \times \text{DC}) - 4.5 \mu\text{A}$$

$$\text{DC} = \text{PWM Duty Cycle}$$

### Sleep State

This device will enter into a low current mode ( $< 275 \mu\text{A}$ ) when CTL lead is brought to less than 0.5 V. All functions are disabled in this mode, except for the regulator.

### Inhibit

When the inhibit voltage is greater than 2.5 V the internal latch is set and the external MOSFET will be turned off for the remainder of the oscillator cycle. The latch is then reset at the start of the next cycle.

### Overvoltage Shutdown

The IC will disable the output during an overvoltage event. This is a real time fault event and does not set the internal latch and therefore is independent of the oscillator timing (i.e. asynchronous). There is no undervoltage lockout. The device will shutdown gracefully once it runs out of headroom. This happens at the point when VREG falls out of regulation.

### Reverse Battery

The CS7054 will not survive a reverse battery condition. Therefore, a series diode is required between the battery and the  $V_{CC}$  lead.

### Load Dump

$V_{CC}$  is internally clamped to 30 V. It is recommended that a 51  $\Omega$  resistor, ( $R_S$ ) is placed in series with  $V_{CC}$  to limit the current flow into the IC in the event of a 40 V peak transient condition.

### Using the CS7054 as a Frequency Converter

Figure 9 shows the CS7054 configured for use as a frequency converter. In the setup shown, a 150 Hz square wave from a microprocessor is converted to a 10 kHz square wave. The duty cycle of each waveform is identical. The amplitude of the input waveform is 5.0 V, but does not need to be. The input amplitude requirement just needs to be high enough to switch the external bipolar transistor. The 10 kHz oscillator frequency is setup per the oscillator section of this data sheet.

The external resistor divider composed of the 3.6 k and 6.2 k resistors supplies 5.0 V to the CTL pin when the input duty cycle is at 100%. This also makes the output waveform 100%.

The RC filter (1.0 M $\Omega$  and 0.1  $\mu\text{F}$ ) sets up a pole at 1.6 Hz:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \left[ 1 \text{ M}\Omega + \left( \frac{(6.2 \text{ k})(3.6 \text{ k})}{6.2 \text{ k} + 3.6 \text{ k}} \right) \right] (0.1 \mu\text{F})}$$

$$= 1.6 \text{ Hz}$$

In this case, the pole is 2 orders of magnitude below the input waveform. Care must be taken to provide the appropriate DC level on the control pin in addition to providing the required response time.

\*Note the current limit feature of the CS7054 has been defeated by grounding the  $I_{SENSE+}$  and the  $I_{SENSE-}$  pins and connecting the  $I_{ADJ}$  lead to  $V_{REG}$ .

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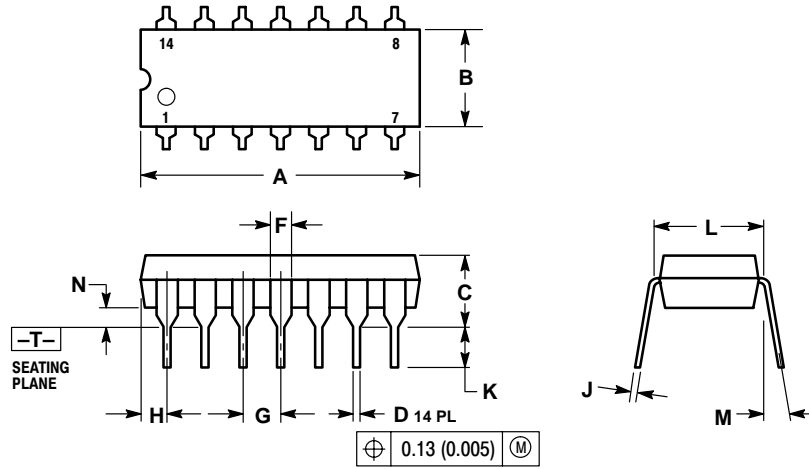


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## PACKAGE DIMENSIONS

**DIP-14**  
**N SUFFIX**  
CASE 646-04  
ISSUE M

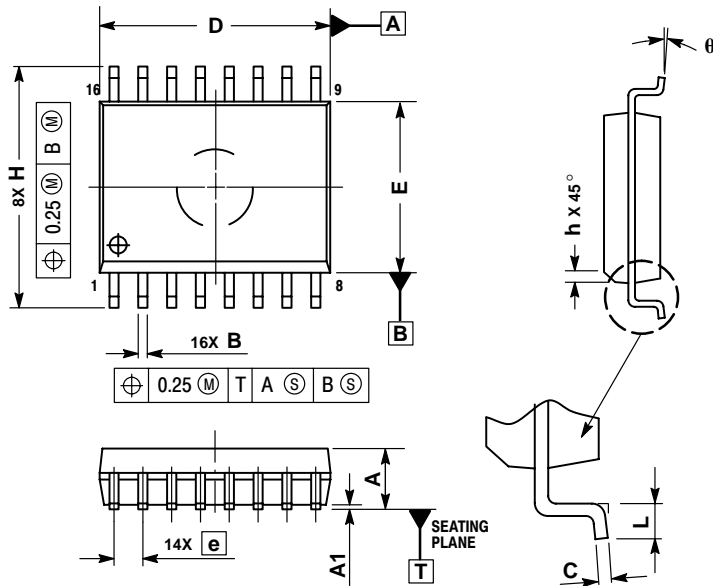


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.740	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.160	0.180	4.06	4.57
D	0.015	0.020	0.38	0.51
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.052	0.072	1.32	1.83
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.020	0.040	0.51	1.02

**SO-16L**  
**DW SUFFIX**  
CASE 751G-03  
ISSUE B



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °


## PACKAGE THERMAL DATA

Parameter		DIP-14	SO-16L	Unit
R <sub>θJC</sub>	Typical	48	23	°C/W
R <sub>θJA</sub>	Typical	85	105	°C/W

**Notes**  
[http://www.onsemi.com/pdf/datasheet/cs7054.pdf](#)

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