

查询"74HC243D"供应商 QUAD BUS TRANSCEIVER, 3-STATE

FEATURES

- Non-inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT243 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT243 are quad bus transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ($\overline{OE}_A$ and $\overline{OE}_B$) can be used to isolate the buses.

The "243" is similar to the "242" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n ; B_n to A_n	$C_L = 15$ pF $V_{CC} = 5$ V	6	11	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	26	34	pF

$GND = 0$ V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz
 f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in V
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

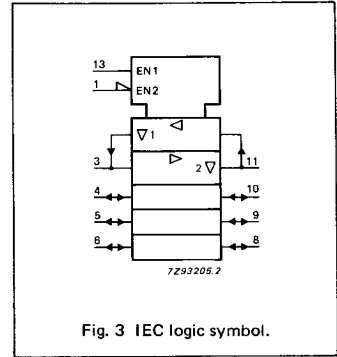
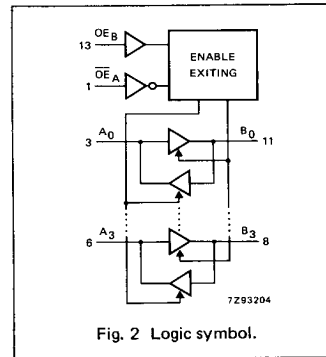
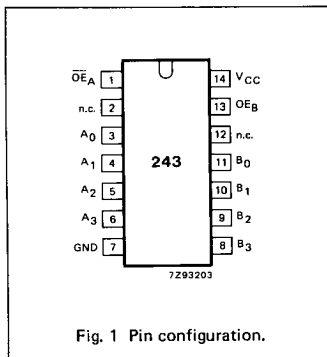
PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).

14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	A_0 to A_3	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	B_0 to B_3	data inputs/outputs
13	$\overline{OE}_B$	output enable input
14	V_{CC}	positive supply voltage



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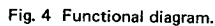


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	inputs	$B = A$
H	L	Z	Z
L	H	Z	Z
H	H	$A = B$	inputs

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t _{PZH} / t _{PZL}	3-state output enable time OE _A to A _n or B _n ; OE _B to A _n or B _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t _{PHZ} / t _{PLZ}	3-state output disable time OE _A to A _n or B _n ; OE _B to A _n or B _n		61 22 18	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Figs 6 and 7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.10
B _n	1.10
OE _A	1.00
OE _B	1.00

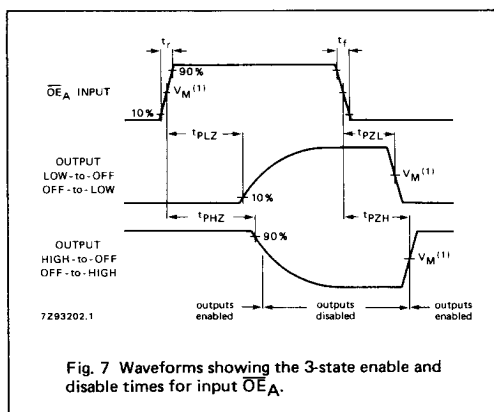
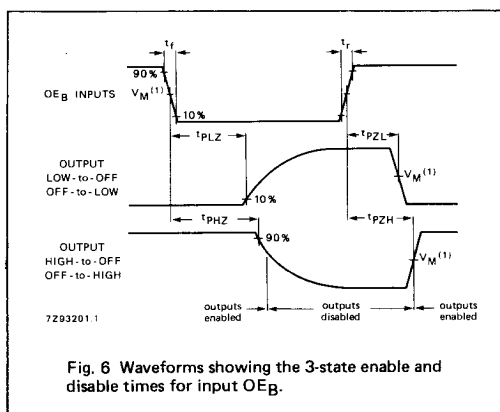
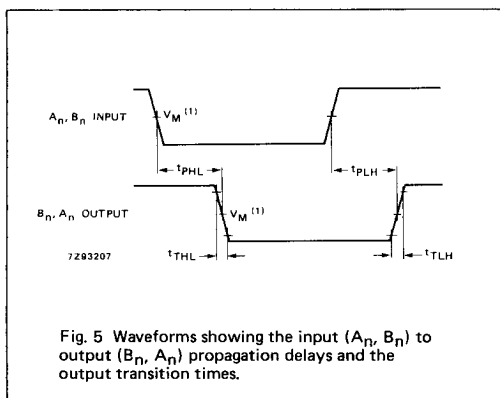
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		13	22		28		33	ns	4.5	Fig. 5
t _{PZH} / t _{PZL}	3-state output enable time OE _A to A _n or B _n ; OE _B to A _n or B _n		18	34		43		51	ns	4.5	Figs 6 and 7
t _{PHZ} / t _{PLZ}	3-state output disable time OE _A to A _n or B _n ; OE _B to A _n or B _n		23	35		44		53	ns	4.5	Figs 6 and 7
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 5

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AC WAVEFORMS



Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.