REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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REV STATUS OF SHEETS			REV																	
			SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13			

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-09-04

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUITS, DIGITAL, BIPOLAR, TTL, HEX BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS WITH 2 INDEPENDENT OR 2 DEPENDENT INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-96878**

SHEET 1 OF 13

DESC FORM 193
JUL 94

5962-E492-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

■ 9004708 0024467 42T ■

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 *PIN*. *The PIN is as shown in the following example:*

5962	-	96878	01	Q	E	A
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

\ V /
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54365A	Hex bus driver, non-inverted, 3-state outputs
02	54366A	Hex bus driver, inverted, 3-state outputs
03	54367A	Hex bus driver, non-inverted, 3-state outputs, w/2 independent enable inputs
04	54368A	Hex bus driver, inverted, 3-state outputs, w/2 independent enable inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-Line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	-0.5 V dc to +7.0 V dc
Input current range (I_{IN})	-30 mA to 5.0 mA
ndard output	-0.5 V to V_{CC}
-STATE output	-0.5 V to 5.5 V
rage temperature range	-65°C to +150°C
ad temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D): 2/	500 mW 2/
Thermal resistance, junction-to-case (Θ_{JC}):	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V
Low level input voltage (V_{IL})	-0.8 V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) . . . . XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883	Test Methods and Procedures for Microelectronics.
MIL-STD-973	Configuration Management.
MIL-STD-1835	Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Maximum power dissipation is defined as $V_{CC} \times I_{CC}$ and must withstand the added P_D due to the short circuit output test (e.g., I_{OS}).

3/ Values will be added when they become available.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test		Symbol	Conditions -55°C ≤ T_C ≤+125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
							Min	Max	
High level output voltage		V_{OH}	V_{CC} = 4.5 V V_{IL} = 0.8 V I_{OH} = -2 mA V_{IH} = 2.0 V		1, 2, 3	All	2.4		V
Low level output voltage		V_{OL}	V_{CC} = 4.5 V V_{IH} = 2.0 V I_{OL} =32 mA V_{IL} = 0.8 V		1, 2, 3	All		0.4	V
Input clamp voltage		V_{IK}	V_{CC} = 4.5 V I_I = -12 mA		1, 2, 3	All		-1.5	V
High level input current		I_{IH}	V_{CC} = 5.5 V V_{IN} = 2.4 V		1, 2, 3	All		40	µA
Low level input current	A inputs	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V Either $\overline{G}$ input at 2.0 V		1, 2, 3	All		-40	µA
			V_{CC} = 5.5 V V_{IN} = 0.4 V Both $\overline{G}$ inputs at 0.4 V			All		-1.6	mA
	$\overline{G}$ inputs		V_{CC} = 5.5 V V_{IN} = 0.4 V		1, 2, 3	All		-1.6	mA
Short circuit output current		I_{OS}	V_{CC} = 5.5 V 1/		1, 2, 3	All	-40	-130	mA
Supply current		I_{CC}	V_{CC} = 5.5 V Data inputs = 0 V Output Controls = 4.5 V		1, 2, 3	1, 3		85	mA
						2, 4		77	
Output leakage current		I_{OZH}	V_{CC} = 5.5 V V_{IH} = 2 V V_{IL} = 0.8 V	V_{OUT} = 2.4 V	1, 2, 3	All		40	µA
		I_{OZL}		V_{OUT} = 0.4 V		All		-40	
Functional test			See 4.4.1b		7, 8	All			
Propagation delay time, I_n to 0_n		t_{PLH}	R_L = 400Ω C_L = 50 pF		9, 10, 11	1, 3		16	ns
						2, 4		17	
		t_{PHL}				1, 3		22	ns
						2, 4		16	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output enable time	t_{PZH}	R_L = 400Ω C_L = 50 pF	9, 10, 11	All		35	ns
	t_{PZL}					37	ns
Output disable time	t_{PHZ}	R_L = 400Ω C_L = 5 pF	9, 10, 11	All		11	ns
	t_{PLZ}					27	ns

1/ Not more than one output should be shorted at a time. For testing I_{OS}, the use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above mormal and cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Device type	01, 02	03, 04
Case outline	E	E
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{G}1$	$1\overline{G}$
2	A1	1A1
3	Y1	1Y1
4	A2	1A2
5	Y2	1Y2
6	A3	1A3
7	Y3	1Y3
8	GND	GND
9	Y4	1Y4
10	A4	1A4
11	Y5	2Y1
12	A5	2A1
13	Y6	2Y2
14	A6	2A2
15	$\overline{G}2$	$2\overline{G}$
16	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Device 01			
$\overline{G}$1	$\overline{G}$2	An	Yn
L	L	H	H
L	L	L	L
L	H	X	Z
H	L	X	Z
H	H	X	Z

Device 02			
$\overline{G}$1	$\overline{G}$2	An	Yn
L	L	H	L
L	L	L	H
L	H	X	Z
H	L	X	Z
H	H	X	Z

Device 03					
1$\overline{G}$	1An	1Yn	2$\overline{G}$	2An	2Yn
L	L	L	L	L	L
L	H	H	L	H	H
H	X	Z	H	X	Z

Device 04					
1$\overline{G}$	1An	1Yn	2$\overline{G}$	2An	2Yn
L	L	H	L	L	H
L	H	L	L	H	L
H	X	Z	H	X	Z

FIGURE 2. Truth tables.

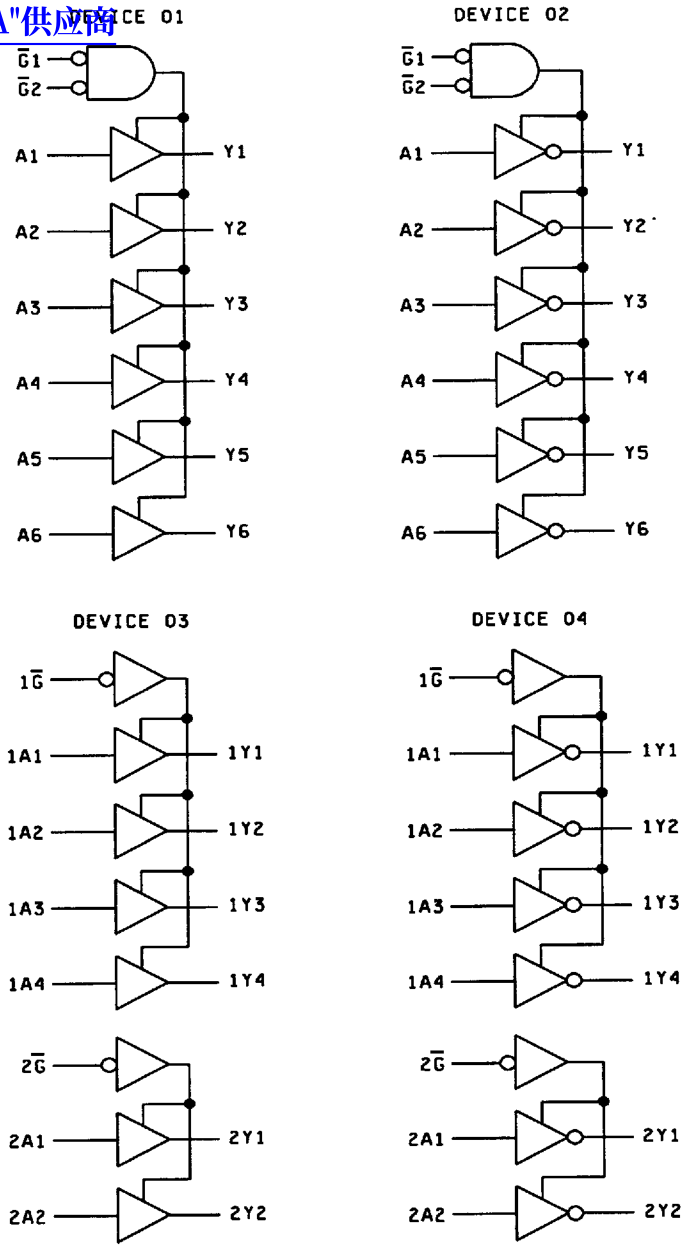
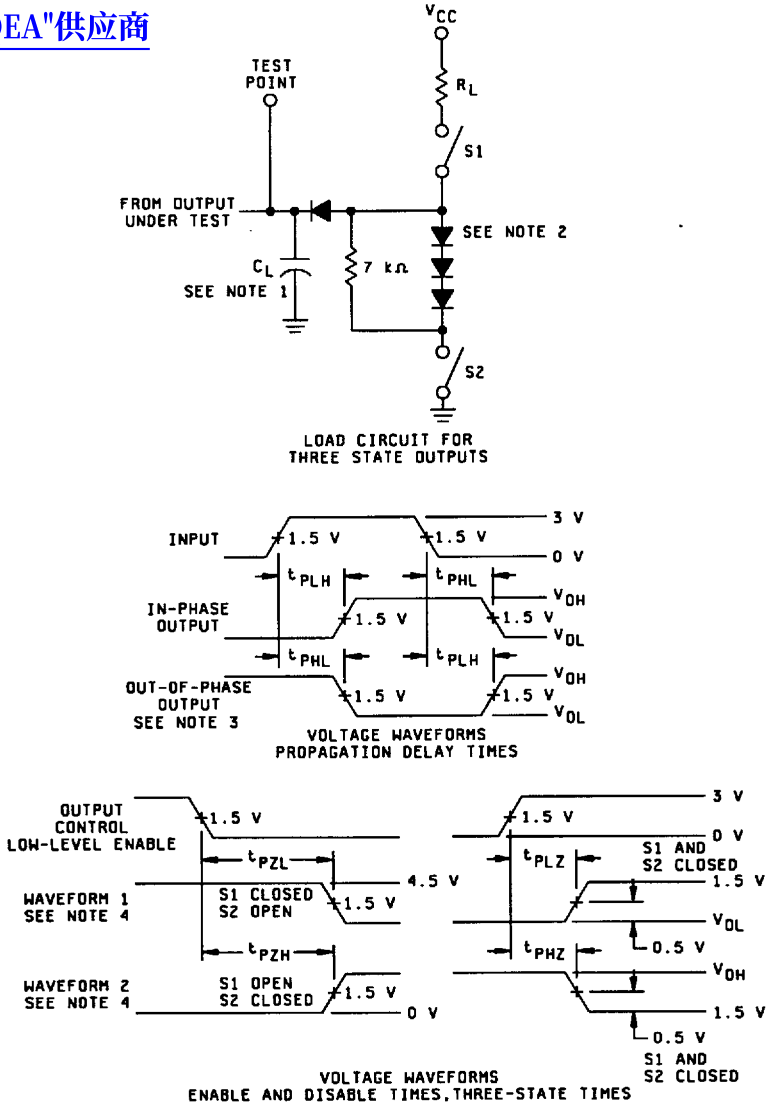


FIGURE 3. Logic diagram.



1/ C_L includes probe and jig capacitance.
2/ All diodes are 1N3064 or equivalent.
3/ When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
4/ Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 4. Test circuit and switching waveforms.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 2 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

  (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

  (2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, and D inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,7 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VAC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 96-09-04

Approved sources of supply for SMD 5962-96878 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9687801QEA	01295	SNJ54365AJ
5962-9687802QEA	01295	SNJ54366AJ
5962-9687803QEA	01295	SNJ54367AJ
5962-9687804QEA	01295	SNJ54368AJ

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated PO Box 60448 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.