

## 3.3 V Clock Synthesizer for DLP™ Systems

### FEATURES

- High-Performance Clock Synthesizer
- Uses a 20 MHz Crystal Input to Generate Multiple Output Frequencies
- Integrated Load Capacitance for 20 MHz Oscillator Reducing System Cost
- All PLL Loop Filter Components are Integrated
- Generates the Following Clocks:
  - REF CLK 20 MHz (Buffered)
  - XCG CLK 100 MHz With SSC
  - DMD CLK 200-400 MHz With Selectable SSC
- Very Low Period Jitter Characteristic:
  - $\pm 100$  ps at 20 MHz Output
  - $\pm 75$  ps at 100 MHz and 200–400 MHz Outputs
- Includes Spread-Spectrum Clocking (SSC), With Down Spread for 100 MHz and Center Spread for 200–400 MHz
- HCLK Differential Outputs for the 100 MHz and the 200–400 MHz Clock
- Operates From Single 3.3-V Supply
- Packaged in TSSOP20
- Characterized for the Industrial Temperature Range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- ESD Protection Exceeds JESD22
- 2000-V Human-Body Model (A114-C) – MIL-STD-883, Method 3015

### TYPICAL APPLICATIONS

- Central Clock Generator for DLP™ Systems

### DESCRIPTION

The CDCDLP223 is a PLL-based high performance clock synthesizer that is optimized for use in DLP™ systems. It uses a 20 MHz crystal to generate the fundamental frequency and derives the frequencies for the 100 MHz HCLK and the 300 MHz HCLK output. Further, the CDCDLP223 generates a buffered copy of the 20 MHz Crystal Oscillator Frequency at the 20 MHz output terminal.

CDCDLP223 PIN ASSIGNMENTS

XIN	1	TSSOP 20	20	IREF
XOUT	2		19	VDD
VSS	3		18	100MHZ
VDD	4		17	100MHZ
20MHZ	5		16	VSS
VSS	6		15	VSS
EN	7		14	300MHZ
IDO	8		13	300MHZ
SDATA	9		12	VSS
SCLK	10		11	VDD

The 100 MHz HCLK output provides the reference clock for the XDR Clock Generator (CDCD5704). Spread-spectrum clocking with 0.5% down spread, which reduces Electro Magnetic Interference (EMI), is applied in the default configuration. The spread-spectrum clocking (SSC) is turned on and off via the serial control interface.

The 300 MHz HCLK output provides a 200-400 MHz clock signal for the DMD Control Logic of the DLP™ Control ASIC. Frequency selection in 20 MHz steps is possible via the serial control interface. Spread-spectrum clocking with  $\pm 1.0\%$  or  $\pm 1.5\%$  center spread is applied, which can be disabled via the serial control interface.

The CDCDLP223 features a fail safe start-up circuit, which enables the PLLs only if a sufficient supply voltage is applied and a stable oscillation is delivered from the crystal oscillator. After the crystal start-up time and the PLL stabilization time, all outputs are ready for use.

The CDCDLP223 works from a single 3.3-V supply and is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



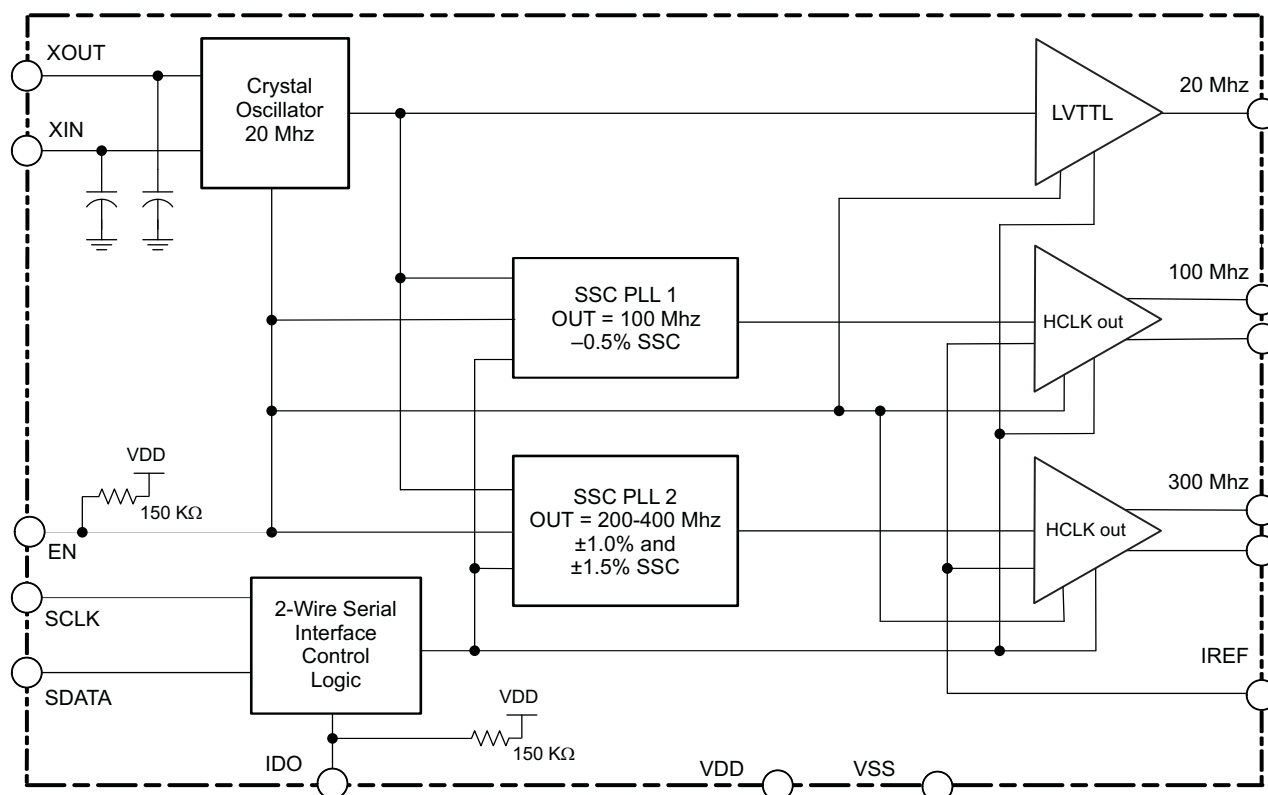
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## FUNCTIONAL BLOCK DIAGRAM



## TERMINAL FUNCTIONS

TERMINAL	PIN	TYPE	DESCRIPTION
XIN	1	I	Crystal oscillator input for 20-MHz crystal in parallel resonance
XOUT	2	O	Crystal oscillator output for 20-MHz crystal in parallel resonance
SDATA	9	I/O Open drain	Data I/O, 2-wire serial interface controller, internal 1-M $\Omega$ pullup
SCLK	10	I Interface Clock	Clock input, 2-wire serial interface controller, internal 1-M $\Omega$ pullup
20 MHz	5	O LVTTTL	Clock output, 20 MHz (buffered output from crystal oscillator)
100 MHz	18	O HCLK	Clock output for XDR clock generator
$\overline{100\text{ MHz}}$	17	O $\overline{\text{HCLK}}$	Clock output for XDR clock generator
300 MHz	14	O HCLK	Clock output for DMD system
$\overline{300\text{ MHz}}$	13	O $\overline{\text{HCLK}}$	Clock output for DMD system
VDD	4,11,19	Power	3.3 V Power supply
VSS	3,6,12,15,16	Ground	Ground
IREF	20	O R <sub>REF</sub> to GND	IREF pin for HCLK output drive-current biasing
EN	7	I LVTTTL	Output enable, 20 MHz, 100 MHz and 200–400 MHz outputs, 150 k $\Omega$ pullup, default = logic high
IDO	8	I LVTTTL	Sets 2-wire serial interface ID address bit A0, 150 k $\Omega$ pull-up resistor, default = logic high

Table 1. EN Pin (20 MHz, 100 MHz and 300 MHz Clocks)

EN PIN	DESCRIPTION
1	All HCLK outputs, and 20-MHz outputs enabled, detailed device configurations are determined by 2-wire serial interface settings.
0	All HCLK = true Hi-Z, both PLLs are powered down and 20-MHz output in Hi-Z and Crystal Oscillator disabled, EN overrides 2-wire serial interface settings.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE	UNIT
V <sub>DD</sub>	Supply voltage range	–0.5 to 4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5 to V <sub>DD</sub> + 0.5	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	–0.5 to V <sub>DD</sub> + 0.5	V
	Input current (V <sub>I</sub> < 0, V <sub>I</sub> > V <sub>DD</sub> )	±20	mA
I <sub>O</sub>	Continuous output current	±17.5	mA
T <sub>stg</sub>	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## PACKAGE THERMAL IMPEDANCE FOR TSSOP20 PACKAGE <sup>(1)</sup>

Airflow (lfm)	θ <sub>JA</sub> (°C/W)	θ <sub>JC</sub> (°C/W)	θ <sub>JB</sub> (°C/W)	Ψ <sub>JT</sub> (°C/W)
0	83.0	32	54	0.25
150	77.9	–	–	
250	75.4	–	–	
500	71.4	–	–	

- (1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature	-40		85	°C
V <sub>DD</sub>	Supply voltage	3.0	3.3	3.6	V
V <sub>IH</sub>	High level input voltage SDATA and SCLK	0.7 × V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IL</sub>	Low level input voltage SDATA and SCLK	−0.15		0.3 × V <sub>DD</sub>	V
V <sub>IL</sub>	Low level input voltage LVTTL			0.8	V
V <sub>I</sub>	thresh Input Voltage threshold LVTTL	1.40			V
V <sub>IH</sub>	High level input voltage LVTTL	2.0			V
I <sub>OH</sub>	High-level output current LVTTL			−8	mA
I <sub>OL</sub>	Low-level output current LVTTL			8	mA
I <sub>OH</sub>	High-level output current HCLK/ <del>HCLK</del>			−20	mA
I <sub>OL</sub>	Low-level output current HCLK/ <del>HCLK</del>			0	mA
t <sub>PU</sub>	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

## RECOMMENDED CRYSTAL SPECIFICATION <sup>(1)</sup>

	MIN	NOM	MAX	UNIT
f <sub>xtal</sub>	Crystal input frequency (fundamental)	20		MHz
ESR	Effective series resistance		100	Ω
P <sub>drive</sub>	Maximum power handling (drive level)	100		μW
C <sub>L</sub>	Load capacitance	20		pF

- (1) See DLP™ Control ASIC DDP2230 datasheet for additional requirements.

**TIMING REQUIREMENTS<sup>(1)</sup>**

over recommended ranges of supply voltage, load and operating free air temperature

PARAMETER		MIN	TYP	MAX	UNIT
<b>XIN, XOUT REQUIREMENTS</b>					
$f_{XIN}$	Frequency of crystal attached to XIN, XOUT, with $C_L = 20$ pF ( $2 \times 40$ pF) on-die capacitance		20		MHz
<b>2 WIRE SERIAL INTERFACE REQUIREMENTS STANDARD MODE</b>					
$f_{SCLK}$	SCLK frequency	0		100	kHz
$t_{H(START)}$	START hold time (see <a href="#">Figure 1</a> )	4.0			$\mu$ s
$t_{W(SCLL)}$	SCLK low-pulse duration (see <a href="#">Figure 1</a> )	4.7			$\mu$ s
$t_{W(SCLH)}$	SCLK high-pulse duration (see <a href="#">Figure 1</a> )	4.0			$\mu$ s
$t_{SU(START)}$	START setup time (see <a href="#">Figure 1</a> )	4.7			$\mu$ s
$t_{H(SDATA)}$	SDATA hold time (see <a href="#">Figure 1</a> )	0		3.45	$\mu$ s
$t_{SU(SDATA)}$	SDATA setup time (see <a href="#">Figure 1</a> )	250			ns
$t_{R(SDATA)}$	SCLK / SDATA input rise time (see <a href="#">Figure 1</a> )			1000	ns
$t_{F(SDATA)}$	SCLK / SDATA input fall time (see <a href="#">Figure 1</a> )			300	ns
$t_{SU(STOP)}$	STOP setup time (see <a href="#">Figure 1</a> )	4.0			$\mu$ s
$t_{BUS}$	Bus free time	4.7			$\mu$ s
<b>2 WIRE SERIAL INTERFACE REQUIREMENTS FAST MODE</b>					
$f_{SCLK}$	SCLK frequency	0		400	kHz
$t_{H(START)}$	START hold time (see <a href="#">Figure 1</a> )	0.6			$\mu$ s
$t_{W(SCLL)}$	SCLK low-pulse duration (see <a href="#">Figure 1</a> )	1.3			$\mu$ s
$t_{W(SCLH)}$	SCLK high-pulse duration (see <a href="#">Figure 1</a> )	0.6			$\mu$ s
$t_{SU(START)}$	START setup time (see <a href="#">Figure 1</a> )	0.6			$\mu$ s
$t_{H(SDATA)}$	SDATA hold time (see <a href="#">Figure 1</a> )	0		0.9	$\mu$ s
$t_{SU(SDATA)}$	SDATA setup time (see <a href="#">Figure 1</a> )	100			ns
$t_{R(SDATA)}$	SCLK / SDATA input rise time (see <a href="#">Figure 1</a> )	20		300	ns
$t_{F(SDATA)}$	SCLK / SDATA input fall time (see <a href="#">Figure 1</a> )	20		300	ns
$t_{SU(STOP)}$	STOP setup time (see <a href="#">Figure 1</a> )	0.6			$\mu$ s
$t_{BUS}$	Bus free time	1.3			$\mu$ s

(1) The CDCDLP223 2-wire serial interface in Send-Mode meets both I<sup>2</sup>C and SMBus *set up time*  $t_{su}$  and *hold time*  $t_h$  requirements.

## APPLICATION INFORMATION

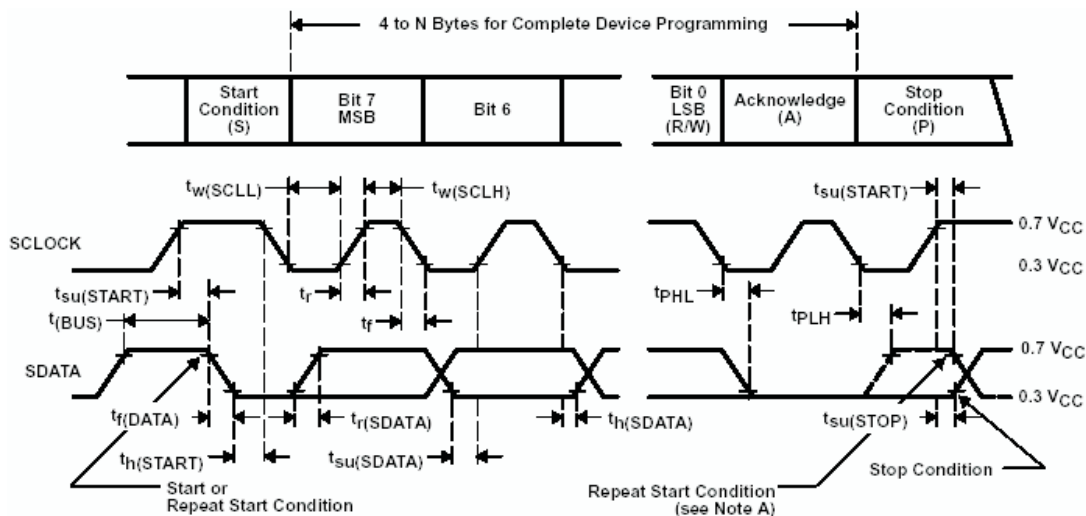


Figure 1. Timing Diagram, Serial Control Interface

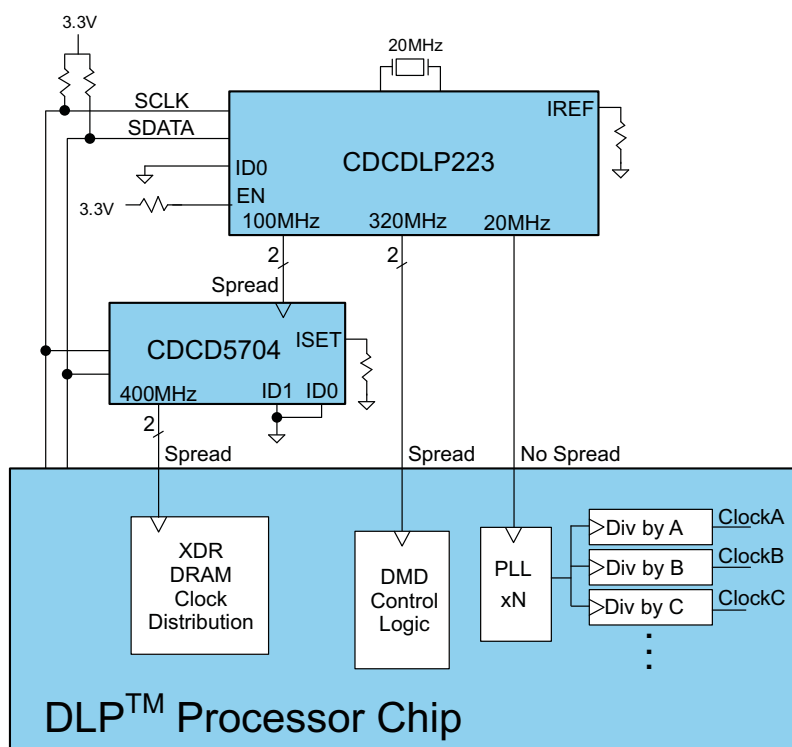
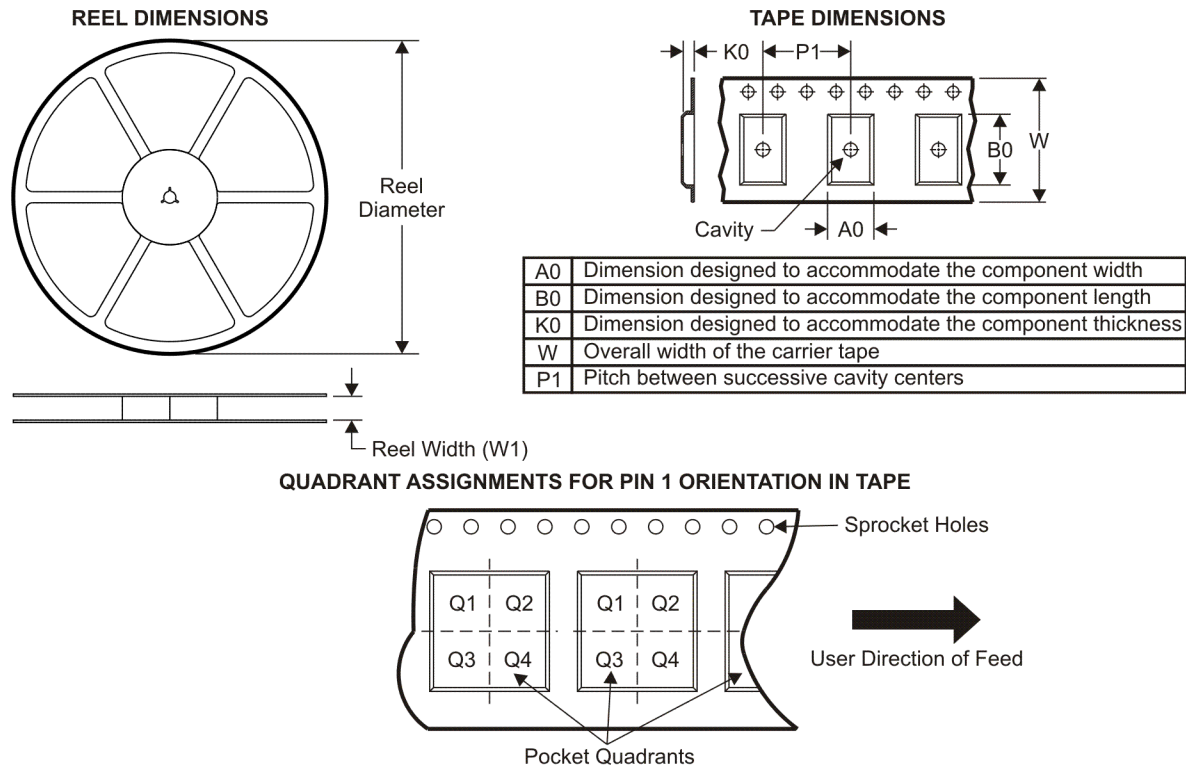


Figure 2. Typical CDCDLP223 Application

**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCDLP223PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



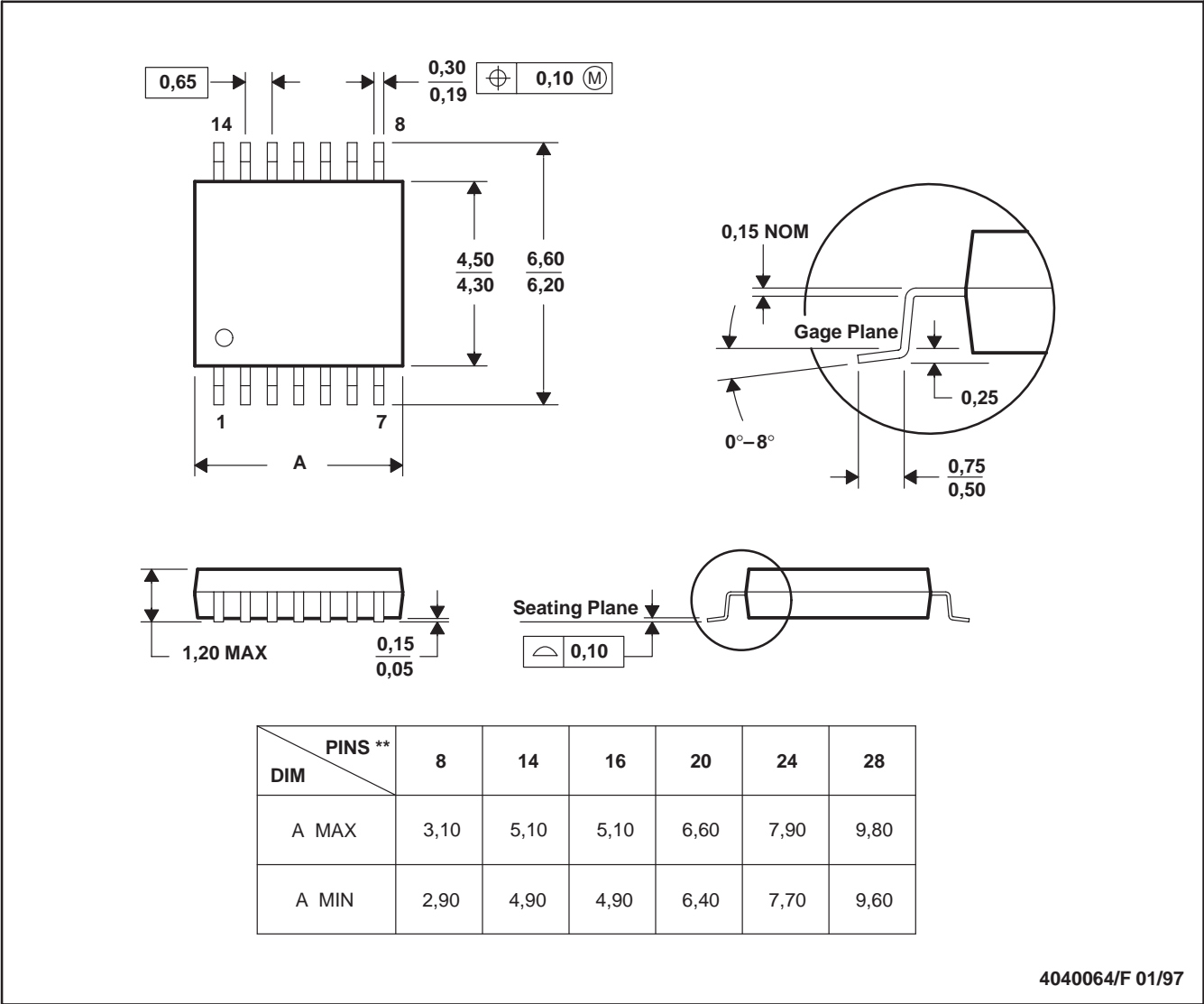
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCDLP223PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-153



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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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