REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R043-92	91-11-25	M. L. Poelking
B	Changes in accordance with NOR 5962-R070-93	93-01-22	M. L. Poelking
C	Change to class level V. Update boilerplate. - LTG	97-07-11	T. M. Hess
D	Changes in accordance with NOR 5962-R001-98	97-10-17	M. L. Poelking
E	Made Rad Hard changes in Table I. Added appendix A. - LTG	99-09-08	M. L. Poelking
F	Update boilerplate to MIL-PRF-38535 requirements. – LTG	01-04-25	Thomas M. Hess
G	Added tests V_{OL2} and V_{OH2} to table I sheet 6. – LTG	01-12-21	Thomas M. Hess
H	Correct the unit of measure from microseconds to nanoseconds for the DMAG(L) to STDINTL(L) test on sheet 10 in Table I. - CFS	02-07-23	Thomas M. Hess

REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G						
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48						
REV	C	C	C	C	C	C	E	E	C	C	E	C	F	E	E	F	C	G	G	G
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	H	C	E	F	F	G	E	E	E	H	E	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Christopher A. Rauch

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
90-02-08

MICROCIRCUIT, DIGITAL, CMOS, BUS CONTROLLER, REMOTE TERMINAL AND MONITOR, MONOLITIHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
H	A	**67268**	**5962-89577**

SHEET 1 OF 48

DSCC FORM 2233
APR 97

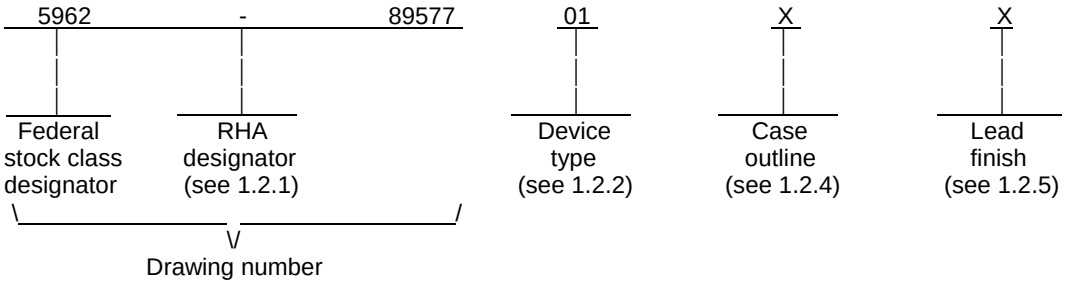
5962-E504-02

1. SCOPE

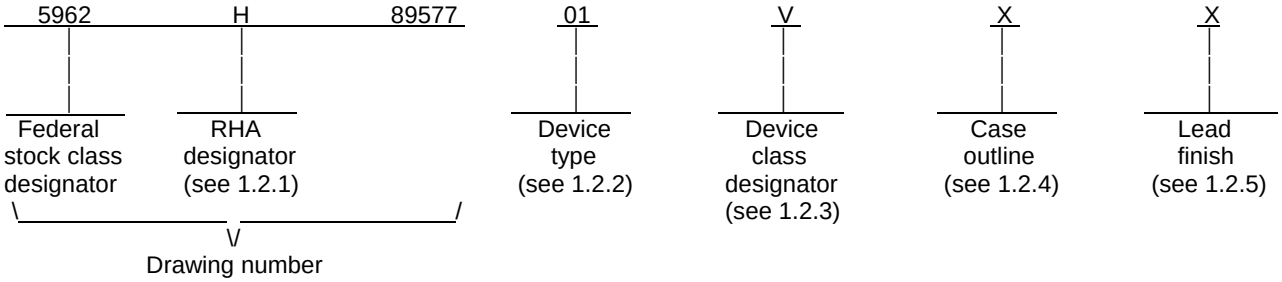
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT1553BCRTM	Bus controller, remote terminal and monitor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-P84	84	Pin grid array
Y	CQCC2-J84	84	Leaded chip carrier w/unformed leads
Z	CQCC1-N84	84	Square chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range	0.3 V to +7.0 V
DC input/dc output voltage range ($V_{I/O}$)	-0.3 V to (V_{DD} +0.3 V)
DC input current (I_I)	±10 mA
Storage temperature range	-65°C to +150°C
Lead tempreature (soldering 10 seconds)	+300°C
Maximum power dissipation, (P_D) 2/	300 mW
Maximum junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Latchup immunity (I_{LU})	±150 mA
Duty cycle	50 ±10 percent

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	4.5 V to 5.5 V
Case operating temperature range (T_C)	-55°C to +125°C
Operating frequency (F_o)	12 MHz ± .01 percent
Radiation features:	
Total dose	≥ 1 x 10^6 Rads (Si)
Single event phenomenon (SEP) effective linear energy threshold, no upsets or latchup (see 4.4.4.4)	≥ 27 MEV- cm^2 /mg
Dose rate upset (20 ns pulse)	3/
Dose rate latchup	3/
Dose rate survivability	3/
Neutron irradiated	> 1 x 10^{14}

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	86.5 percent

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

3/ When characterized as a result of the procuring activities request, the condition will be specified.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.4 Switching test circuit and waveforms. The switching test circuit and waveforms shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V ≤ V_{DD} ≤ 5.5 V 1/ -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input voltage TTL inputs	V_{IL}		1, 2, 3	All		0.8	V
High level input voltage TTL inputs 2/	V_{IH}		1, 2, 3	All	2.0		V
Input leakage current TTL inputs	I_{IN}	V_{IN} = V_{DD} or V_{SS}	1, 2, 3	All	-1	1	µA
		M, D, P,L, R, F, G, H	1	All	-10	10	
With pull-up resistors		V_{IN} = V_{DD}	1, 2, 3	All	-1	1	
		M, D, P,L, R, F, G, H	1	All	-10	10	
With pull-up resistors		V_{IN} = V_{SS}	1, 2, 3	All	-550	-80	
		M, D, P,L, R, F, G, H	1	All	-900	-150	
Low level output voltage TTL outputs	V_{OL}	I_{OL} = 3.2 mA	1, 2, 3	All		0.4	V
Low level output voltage CMOS outputs	V_{OL2}	I_{OL} = 50 µA	1, 2, 3	All		V_{SS} +0.1	V
High level output voltage TTL outputs	V_{OH}	I_{OH} = -400 µA	1, 2, 3	All	2.4		V
High level output voltage CMOS outputs	V_{OH2}	I_{OH} = -50 µA	1, 2, 3	All	V_{DD} -0.1		V
Three-state output leakage Current TTL outputs	I_{OZ}	V_{OUT} = V_{DD} or V_{SS}	1, 2, 3	All	-10	10	µA
Short-circuit output current 3/ 4/	I_{OS}	V_{DD} = 5.5 V, V_{OUT} = V_{DD}	1, 2, 3	All		110	mA
		V_{DD} = 5.5 V, V_{OUT} = 0 V	1, 2, 3	All	-110		mA
Quiescent current 5/ 14/	Q_{IDD}		1, 3	All		35	µA
			2			1	mA
Average operating current 3/ 6/	I_{DD}	f = 12 MHz, C_L = 50 pF	1, 2, 3	All		50	mA
Input capacitance	C_{IN}	See 4.4.1c	4	All		10	pF
Output capacitance	C_{OUT}		4	All		15	pF
Bidirect I/O capacitance	C_{IO}		4	All		20	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics. - Continued

Test	Symbol	Conditions 4.5 V ≤ V_{DD} ≤ 5.5 V -55°C ≤ T_C ≤+125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional tests		See 4.4.1d	7, 8				
$\overline{DMACK}$ (L) to $\overline{DMAR}$ high impedance	T_{SHL1}	See figure 3 BURST DMA timing	9, 10, 11	All	0	10	ns
		M,D,P,L,R,F,G,H			-5	5	
$\overline{DMAG}$ (L) to $\overline{DMACK}$ (L) 7/	T_{PZL2}	See figure 3 BURST DMA timing	9, 10, 11	All	0	45	ns
$\overline{DMAG}$ (L) to $\overline{TSCTL}$ (L) 15/	T_{PHL2}		9, 10, 11	All	2x MCLK	4x MCLK	ns
$\overline{TSCTL}$ (L) to ADDRESS valid 3/	T_{PzL1}		9, 10, 11	All	0	40	ns
		M,D,P,L,R,F,G,H			-2	40	
$\overline{RWR}$ / $\overline{RRD}$ (H) to $\overline{DMACK}$ (H)	t_{HLH2}	See figure 3 BURST DMA timing	9, 10, 11	All	THMC1 -10	THMC1 +10	ns
$\overline{TSCTL}$ (L) to $\overline{RWR}$ / $\overline{RRD}$ (L)	t_{PHL3}		9, 10, 11	All	MCLK -20	MCLK +20	ns
$\overline{DMAG}$ (L) to $\overline{DMAG}$ (H) 15/	t_{PW2}		9, 10, 11	All	MCLK	6xMCLK	ns
$\overline{DMAR}$ (L) to BURST(H)	t_{OOZL1}		9, 10, 11	All	-10	10	ns
$\overline{DMAR}$ (L) to $\overline{DMAG}$ (L) 8/ 15/	t_{PHL4}	MCLK = 12 MHz MCLK = 6 MHz See figure 3 BURST DMA timing	9, 10, 11	All	0 0	1.9 (0.8) 3.5 (1.9)	µs
ADDRESS valid to $\overline{RRD}$ (L) (Address setup)	t_{SHL1}	See figure 3 DMA read timing	9, 10, 11	All	THMC2 -10	THMC2 +5	ns
		M,D,P,L,R,F,G,H			THMC2 -10	THMC2 +10	
$\overline{RRD}$ (L) to $\overline{RRD}$ (H)	T_{PW1}	See figure 3 DMA read timing	9, 10, 11	All	MCLK -10	MCLK +5	ns
$\overline{RRD}$ (H) to ADDRESS high impedance (ADDRESS hold)	t_{HLZ2}		9, 10, 11	All	THMC1 -10	THMC1 +10	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics. - Continued

Test	Symbol	Conditions 4.5 V ≤ V_{DD} ≤ 5.5 V -55°C ≤ T_C ≤+125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RRD}$ (H) to DATA high impedance (DATA hold)	t_{HLZ1}	See figure 3 DMA read timing	9, 10, 11	All	5		ns
DATA valid to $\overline{RRD}$ (H) (DATA setup)	t_{SLH1}		9, 10, 11	All	40		ns
MCLK(H) to MCLKD2(H)	t_{PLH1}		9, 10, 11	All	0	40	ns
MCLK(H) to $\overline{TSCTL}$ / $\overline{MEMCSO}$ (L)	t_{PLH2}		9, 10, 11	All	0	40	ns
MCLK(H) to $\overline{RRD}$ (L)	T_{IOHL1}		9, 10, 11	All	0	60	ns
ADDRESS valid to $\overline{RWR}$ (L) (ADDRESS setup)	t_{SHL1}	See figure 3 DMA write timing	9, 10, 11	All	THMC2 -10	THMC2 +5	ns
		M,D,P,L,R,F,G,H			THMC2 -10	THMC2 +10	
$\overline{RWR}$ (L) to DATA valid 13/	t_{OOZL1}	See figure 3 DMA write timing	9, 10, 11	All	0	30	ns
		M,D,P,L,R,F,G,H			-5	30	
$\overline{RWR}$ (H) to DATA high impedance DATA hold)	t_{HLZ1}	See figure 3 DMA write timing	9, 10, 11	All	THMC1 -10	THMC1 +10	ns
$\overline{RWR}$ (H) to ADDRESS high impedance (ADDRESS hold)	t_{HLZ2}		9, 10, 11	All	THMC1 -10	THMC1 +10	ns
$\overline{RWR}$ (L) to $\overline{RWR}$ (H)	t_{PW1}		9, 10, 11	All	MCLK -10	MCLK +5	ns
MCLK(H) to MCLKD2(H)	t_{PLH1}		9, 10, 11	All	0	40	ns
MCLK(H) to $\overline{TSCTL}$ / $\overline{MEMCSO}$ (L)	t_{PLH2}		9, 10, 11	All	0	40	ns
MCLK(H) to $\overline{RWR}$ (L)	t_{IOHL1}		9, 10, 11	All	0	60	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics. - Continued

Test	Symbol	Conditions 4.5 V ≤ V_{DD} ≤ 5.5 V -55°C ≤ T_C ≤+125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ADDRESS valid to DATA Valid 9/	t_{OOZH2}	See figure 3 Register read timing	9, 10, 11	All		80	ns
$\overline{RD}$ + $\overline{CS}$ (H) to DATA high impedance (DATA hold)	t_{HLH2}		9, 10, 11	All	5	50	ns
$\overline{RD}$ + $\overline{CS}$ (L) to DATA valid (DATA access) 9/	t_{OOZH1}		9, 10, 11	All		60	ns
$\overline{RD}$ + $\overline{CS}$ (H) to ADDRESS high impedance (ADDRESS hold)	t_{HLH1}		9, 10, 11	All	5		ns
$\overline{RD}$ + $\overline{CS}$ (L) to $\overline{RD}$ + $\overline{CS}$ (H)	t_{PW1}		9, 10, 11	All	60		ns
$\overline{RD}$ + $\overline{CS}$ (H) to $\overline{RD}$ + $\overline{CS}$ (L) 15/	t_{PW2}		9, 10, 11	All	80		ns
ADDRESS valid to $\overline{WR}$ + $\overline{CS}$ (L) (ADDRESS setup)	t_{SHL1}	See figure 3 Register write timing	9, 10, 11	All	60		ns
DATA valid to $\overline{WR}$ + $\overline{CS}$ (L) (DATA setup)	t_{SHL2}		9, 10, 11	All	5		ns
$\overline{WR}$ + $\overline{CS}$ (L) to $\overline{WR}$ + $\overline{CS}$ (H)	t_{PW1}		9, 10, 11	All	60		ns
$\overline{WR}$ + $\overline{CS}$ (H) to DATA high impedance (DATA hold)	t_{HLH1}		9, 10, 11	All	10		ns
$\overline{WR}$ + $\overline{CS}$ (H) to ADDRESS high impedance (ADDRESS hold)	t_{HLH2}		9, 10, 11	All	10		ns
$\overline{WR}$ + $\overline{CS}$ (H) to $\overline{WR}$ + $\overline{CS}$ (L) 15/	t_{PW2}		9, 10, 11	All	80		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics. - Continued

Test	Symbol	Conditions 4.5 V ≤ V_{DD} ≤ 5.5 V -55°C ≤ T_C ≤+125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RD}$ (L) to $\overline{RRD}$ (L)	t_{PHL1}	See figure 3 Dual port interface timing	9, 10, 11	All	0	30	ns
$\overline{WR}$ (L) to $\overline{RWR}$ (L)	t_{PHL2}		9, 10, 11	All	0	30	ns
$\overline{MEMCSI}$ (L) to $\overline{MEMCSO}$ (L)	t_{PHL3}		9, 10, 11	All	0	30	ns
$\overline{MEMWIN}$ (H) to DMA activity 10/	t_{OOLH1}	See figure 3 Memory window (RT) mode	9, 10, 11	All	9		µs
$\overline{MEMWIN}$ (L) to $\overline{MEMWIN}$ (H) 10/	t_{PW1}		9, 10, 11	All	0	10/	µs
Data word to DMA Activity 15/	t_{PZL1}		9, 10, 11	All	0	4	µs
$\overline{DMAG}$ (L) to $\overline{DMAGO}$ (L) 12/	t_{PHL1}	See figure 3 Arbitration when $\overline{DMAG}$ is asserted before arbitration	9, 10, 11	All	0	30	ns
$\overline{DMACK}$ (L) to $\overline{DMAR}$ high impedance	t_{SHL1}		9, 10, 11	All	0	10	ns
		M,D,P,L,R,F,G,H			-5	5	
MCLK(H) to MCLKD2(H)	t_{PLH2}		9, 10, 11	All	0	40	ns
$\overline{MEMWIN}$ (H) to $\overline{DMAR}$ (L) 10/	t_{OOLH2}	See figure 3 Interrupt log list entry operation timing	9, 10, 11	All	9		µs
$\overline{TSCTL}$ (H) to $\overline{STDINTP}$ / $\overline{STDINTL}$ (L)	t_{OOLH1}		9, 10, 11	All		1	µs
$\overline{STDINTP}$ (L) to $\overline{STDINTP}$ (H)	t_{PW1}		9, 10, 11	All	320	340	ns
$\overline{DMACK}$ (L) to $\overline{RWR}$ (L)	t_{OOHL1}		9, 10, 11	All	3xMCLK -10	5xMCLK	ns
$\overline{DMAG}$ (L) to $\overline{STDINTL}$ (L)	t_{OOHL2}		9, 10, 11	All	8xMCLK	10x MCLK +40	ns

See footnotes on next page.

TABLE IA. Electrical performance characteristics. - Continued

1/ Devices supplied to this drawing are characterized at all levels M, D, P, L, R, F, G, and H of irradiation. However, this device is only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Radiation hardened technology shall have a V_{IH} pre-irradiation limit of 2.2 V.

3/ Guaranteed to the limit specified in table IA. Tested only at initial qualification, and after any design or process changes which may affect this characteristic.

4/ Not more than one output may be shorted at a time for a maximum duration of one second.

5/ All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

6/ Includes current through input pull-up. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.

7/ $\overline{\text{DMAG}}$ must be asserted at least 45 ns prior to the rising edge of MCLKD2 in order to be recognized for the next MCLKD2 cycle. If $\overline{\text{DMAG}}$ is not asserted at least 45 ns prior to the rising edge of MCLKD2, $\overline{\text{DMAG}}$ is not recognized until the following MCLKD2 cycle.

8/ Number in parentheses indicates the longest $\overline{\text{DMAR}}$ (L) to $\overline{\text{DMAG}}$(L) allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT response time. The number not in parentheses applies to all other circumstances.

9/ User must adhere to both T_{OOZH1} and T_{OOZH2} timing constraints to ensure valid data.

10/ $\overline{\text{MEMWIN}}$ is an internal test pin only and should be considered a floating pin and not for use.

11/ The pulse width = (11 µs - t_{DMA} - t_{PZL1}) where t_{DMA} is the time to complete DMA activity.

12/ When $\overline{\text{DMAG}}$ is asserted before $\overline{\text{DMAR}}$, the $\overline{\text{DMAG}}$ signal passes through device 01 as $\overline{\text{DMAGO}}$.

13/ Timing is not valid for RT timer field of message status word. The timer value may update during a DMA memory write.
14/ Guaranteed to pre-and post-irradiation limits.
15/ Guaranteed by functional test.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	T_A = Temperature ±10°C 4/	Memory pattern	V_{CC} = 4.5 V T_A = +25°C		Bias for latch-up test V_{CC} =5.5 V no latch-up LET 4/ T_A = +125°C
			Effective LET no upsets	Maximum device cross section cm^2/bit (LET = 128)	
All	+25°C	5/	≥ 27	≤ 8.5×10^{-7}	≤ 80

NOTE: Devices that contain cross coupled resistance must be tested at the maximum rated T_A
1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Values will be added when they become available. Rad hard devices have not yet been tested for SEP.
4/ Worst case temperature T_A = +125°C.
5/ For memories only.

Device type	01		
Case outlines	X	Y, Z	Description
Terminal symbol	Terminal Numbers		
V_{SS}	F3	1	Ground
D7	F1	2	Bit 7 of the data bus, TTB
D6	G1	3	Bit 6 of the data bus, TTB
D5	G2	4	Bit 5 of the data bus, TTB
D4	G3	5	Bit 4 of the data bus, TTB
D3	H1	6	Bit 3 of the data bus, TTB
D2	H2	7	Bit 2 of the data bus, TTB
D1	J1	8	Bit 1 of the data bus, TTB
D0	K1	9	Bit 0, LSB of the data bus, TTB
$\overline{MRST}$	J2	10	Master Reset, Active low, TTL input
BCRTSEL	L1	11	BC/$\overline{RT}$ Select, TUI
LOCK	K2	12	Lock, Active high, TUI
TAZ	K3	13	Transmit (Channel) A Z, TO
TAO	L2	14	Transmit (Channel) A O, TO
RAZ	L3	15	Receive (Channel) A Z, TI
RAO	K4	16	Receive (Channel) A O, TI
TBZ	L4	17	Transmit (Channel) B Z, TO
TBO	K6	18	Transmit (Channel) B O, TO
RBZ	K5	19	Receive (Channel) B Z, TI
RBO	L5	20	Receive (Channel) B O, TI
CLK	J5	21	Clock, TI
V_{SS}	J6	22	Ground
V_{DD}	L6	23	+5.0 V

FIGURE 1. Terminal connections.

Device Type	01		
Case Outlines	X	Y, Z	Description
Terminal Symbol	Terminal Numbers		
$\overline{\text{EXTOVR}}$	L7	24	External Override, Active low, TUI
$\overline{\text{TIMERON}}$	K7	25	(RT) Timer On, Active low, TO
CHA/$\overline{\text{B}}$	J7	26	Channel A/$\overline{\text{B}}$, TO
$\overline{\text{COMSTR}}$	L8	27	(RT) Command Strobe, Active low, TO
RTAO	K8	28	Remote Terminal Address Bit 0, LSB, TUI
RTA1	L9	29	Remote Terminal Address Bit 1, TUI
RTA2	L10	30	Remote Terminal Address Bit 2, TUI
RTA3	K9	31	Remote Terminal Address Bit 3, TUI
RTA4	L11	32	Remote Terminal Address Bit 4, TUI
RTPTY	K10	33	Remote Terminal Address, Parity, TUI
A0	J10	34	Bit 0 (LSB) of the address bus, TTB
A1	K11	35	Bit 1 of the address bus, TTB
A2	J11	36	Bit 2 of the address bus, TTB
A3	H10	37	Bit 3 of the address bus, TTB
A4	H11	38	Bit 4 of the address bus, TTB
A5	G9	39	Bit 5 of the address bus, TTB
A6	G10	40	Bit 6 of the address bus, TTB
A7	G11	41	Bit 7 of the address bus, TTB
V_{SS}	F10	42	Ground
V_{DD}	F9	43	+5.0 V
A8	E9	44	Bit 8 of the address bus, TTO

FIGURE 1. Terminal connections. - Continued

Device Type	01		
Case outlines	X	Y, Z	Description
Terminal Symbol	Terminal Number		
A9	E11	45	Bit 9 of the address bus, TTO
A10	E10	46	Bit 10 of the address bus, TTO
A11	F11	47	Bit 11 of the address bus, TTO
A12	D11	48	Bit 12 of the address bus, TTO
A13	D10	49	Bit 13 of the address bus, TTO
A14	C11	50	Bit 14 of the address bus, TTO
A15	B11	51	Bit 15 of the address bus, TTO
$\overline{RWR}$	C10	52	RAM Write, Active low, TO
$\overline{RRD}$	A11	53	RAM Read (Active low)
$\overline{MEMCSO}$	B10	54	Memory Chip Select Out, Active low, TO
$\overline{TSCTL}$	B9	55	Three-State Control, Active low, TO
$\overline{DMAR}$	A10	56	DMA Request, Active low, inactive state is high impedance, TTO
$\overline{DMAG}$	A9	57	DMA Grant, Active low, TI
$\overline{DMACK}$	B8	58	DMA Acknowledge, Active low, inactive state is high impedance, TTO
$\overline{MEMCSI}$	A8	59	Memory Chip Select In, Active low, TI
$\overline{WR}$	C7	60	Write, Active low, TI
$\overline{RD}$	B7	61	Read, Active low, TI
$\overline{CS}$	A7	62	Chip Select, Active low, TI
V_{SS}	B6	63	Ground
V_{DD}	C6	64	+5.0 V
MCLK	C5	65	Memory Clock, TI
AEN	A5	66	Address Enable, Active high, TI

FIGURE 1. Terminal connections. - Continued

Device Type	01		
Case Outlines	X	Y, Z	
Terminal symbol	Terminal Numbers		Description
$\overline{\text{DMAGO}}$	B5	67	DMA grant out, low, TO
$\overline{\text{STDINTL}}$	A6	68	Standard interrupt level, active low, inactive state is high impedance, TTO
$\overline{\text{STDINTP}}$	A4	69	Standard interrupt pulse, active low, TO
$\overline{\text{HPINT}}$	B4	70	High-priority interrupt active low, inactive state is high impedance, TTO
MCLKD2	A3	71	Memory clock divided by two, TO
SSYSF	A2	72	Subsystem fail, active high, TI
$\overline{\text{MEMWIN}}$	B3	73	Memory access window, active low, TO
BURST	A1	74	BURST, DMA cycle, multiple word DMA access, active high, TO
BCRTF	B2	75	BCRT fail, active high, TO
D15	C2	76	Bit 15 MSB of the data bus, TTB
D14	B1	77	Bit 14 of the data bus, TTB
D13	C1	78	Bit 13 of the data bus, TTB
D12	D2	79	Bit 12 of the data bus, TTB
D11	D1	80	Bit 11 of the data bus, TTB
D10	F2	81	Bit 10 of the data bus, TTB
D9	E2	82	Bit 9 of the data bus, TTB
D8	E1	83	Bit 8 of the data bus, TTB
V_{DD}	E3	84	+5.0 V

NOTES: Address and data busses are in the high-impedance state when idle.
TI = TTL input
TO = TTL output
TTB = bidirectional
TTO = three state TTL output
TUI = TTL input (pull-up)
$\overline{\text{MEMWIN}}$ is an internal test pin only and should be considered a floating pin and not for use.

FIGURE 1. Terminal connections. - Continued

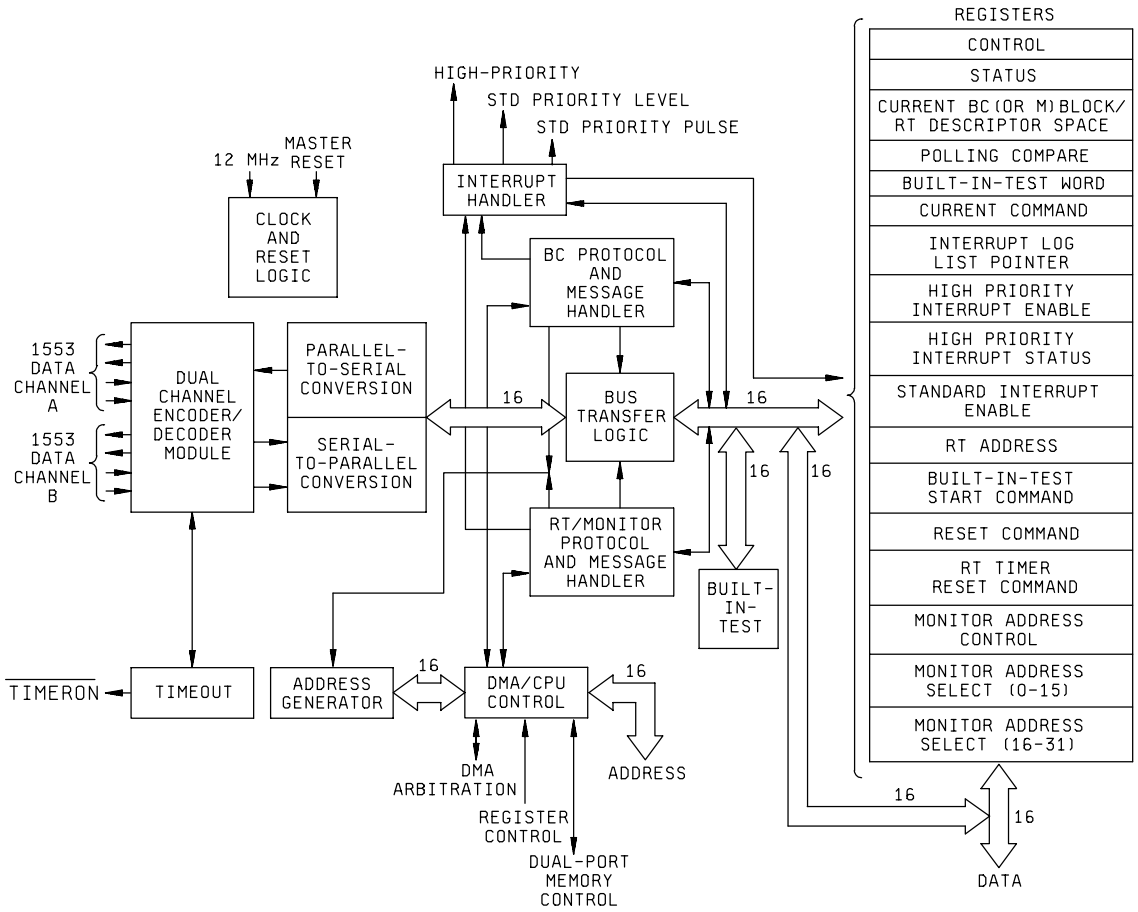
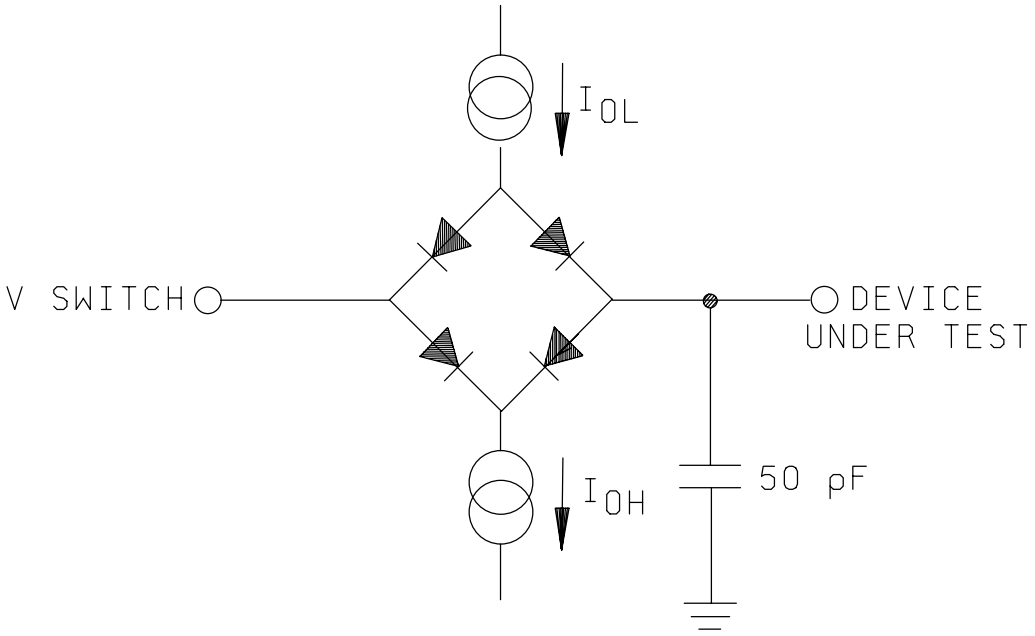
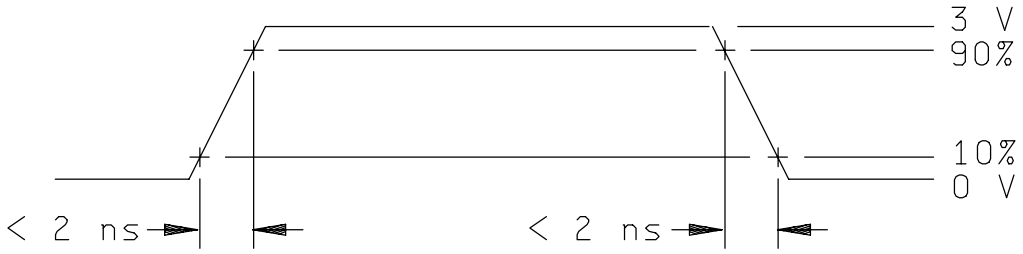


FIGURE 2. Functional block diagram.



TEST CIRCUIT



INPUT PULSES

FIGURE 3. Switching test circuit and waveforms.

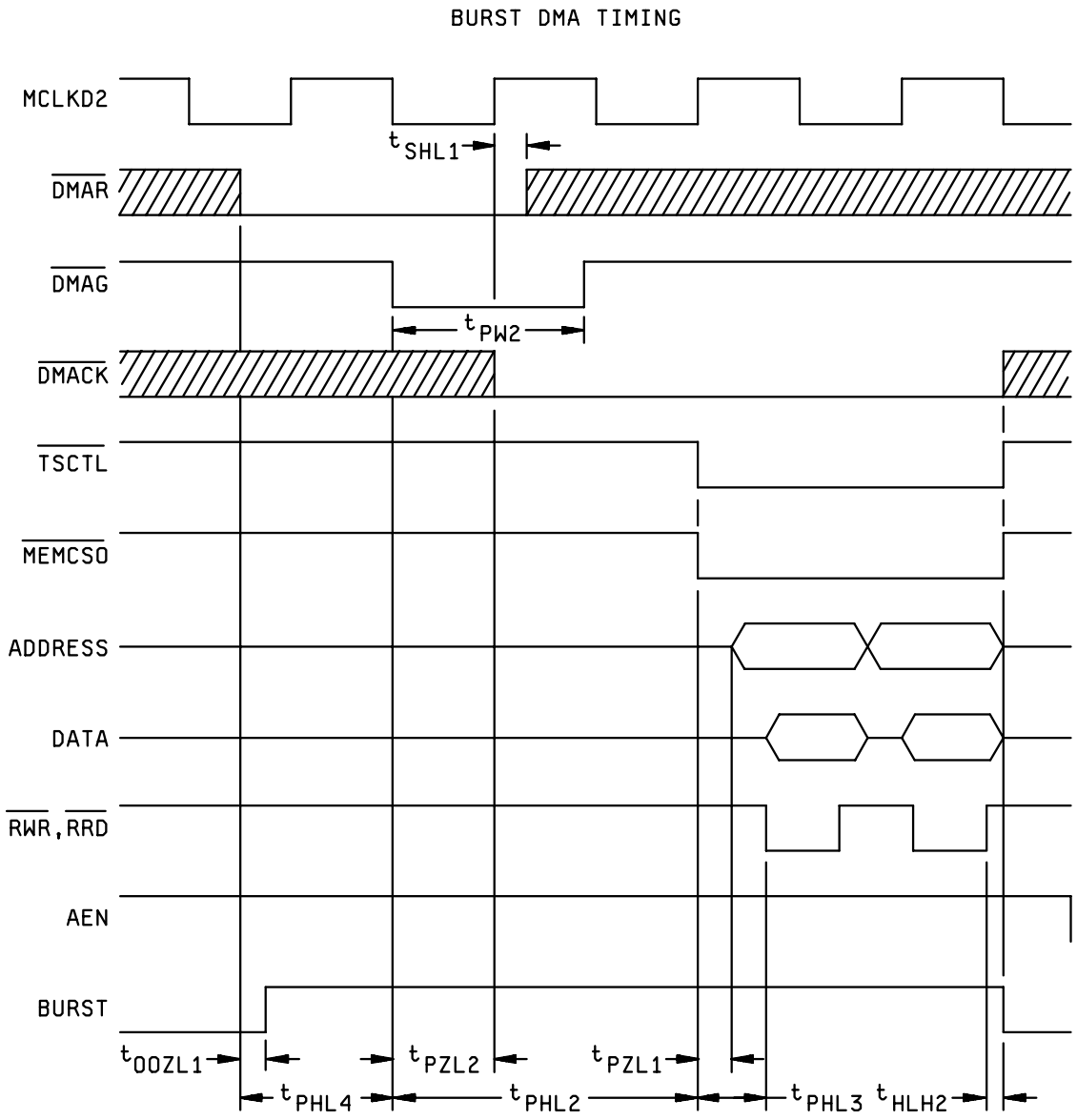


FIGURE 3. Switching test circuit and waveforms. - Continued

DMA READ TIMING

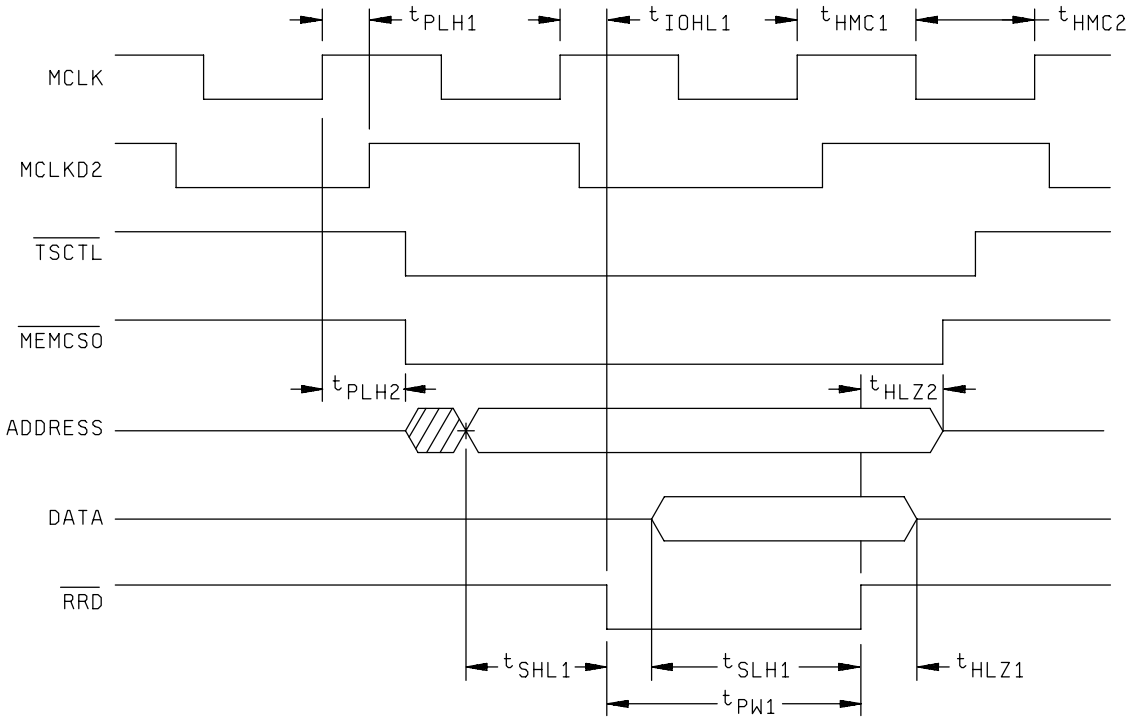


FIGURE 3. Switching test circuit and waveforms. - Continued

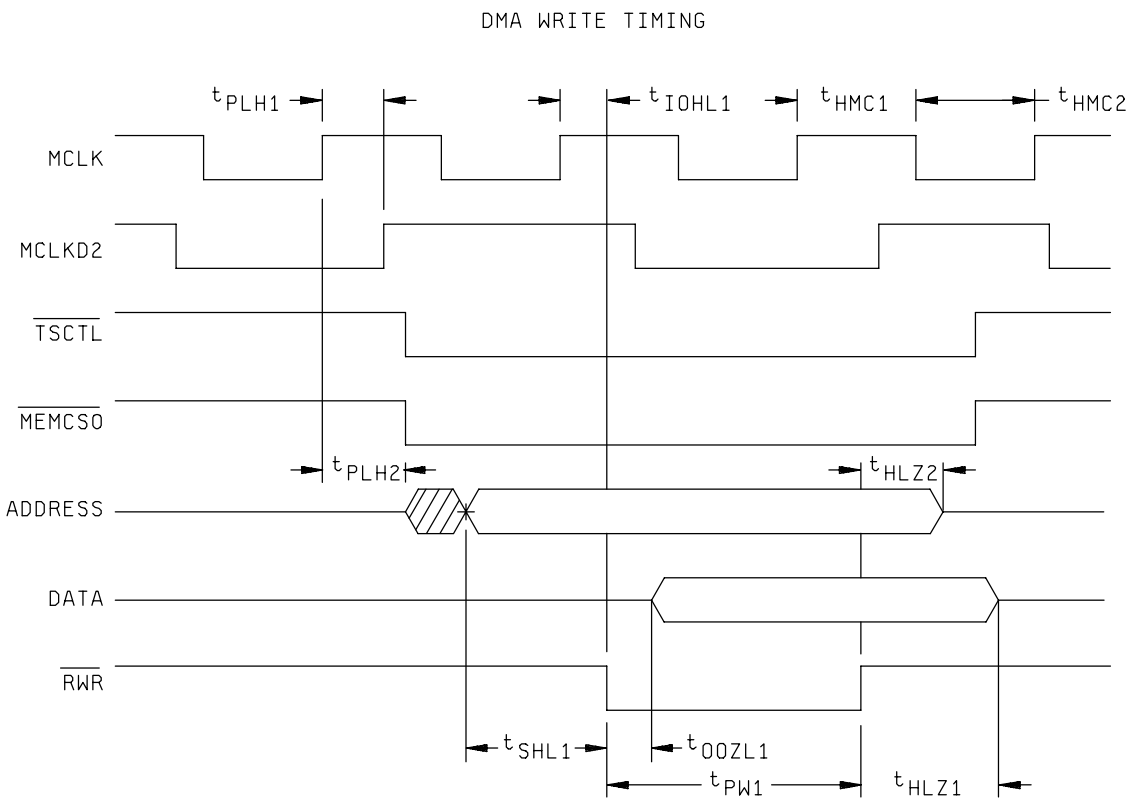
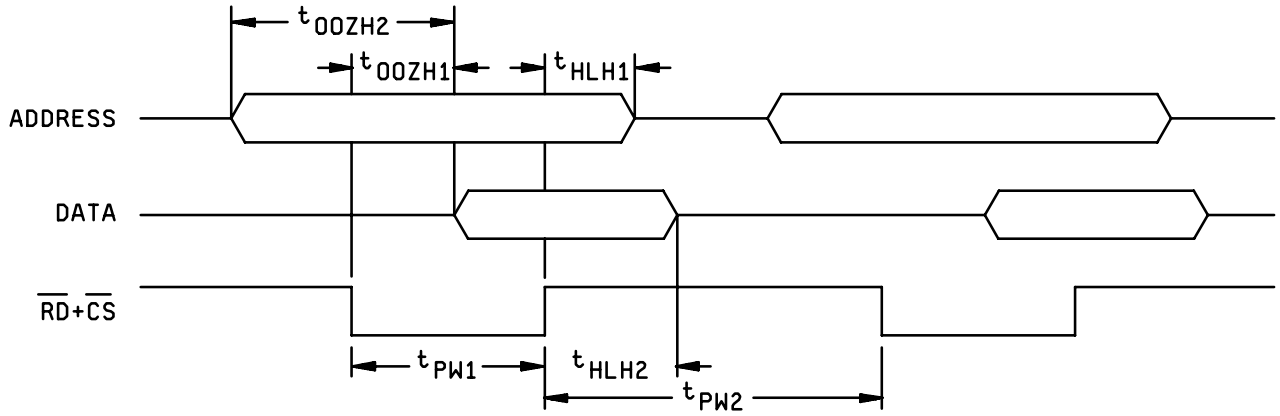


FIGURE 3. Switching test circuit and waveforms. - Continued

REGISTER READ TIMING



REGISTER WRITE TIMING

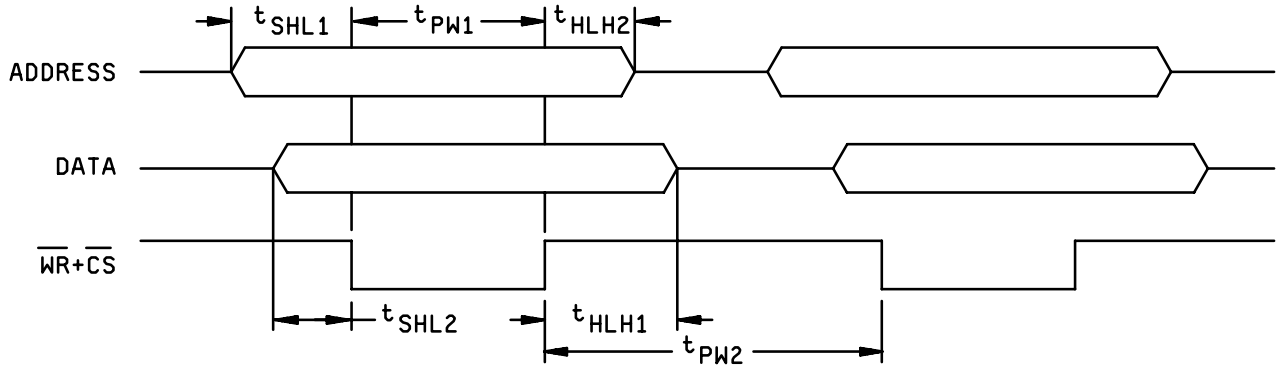


FIGURE 3. Switching test circuit and waveforms. - Continued

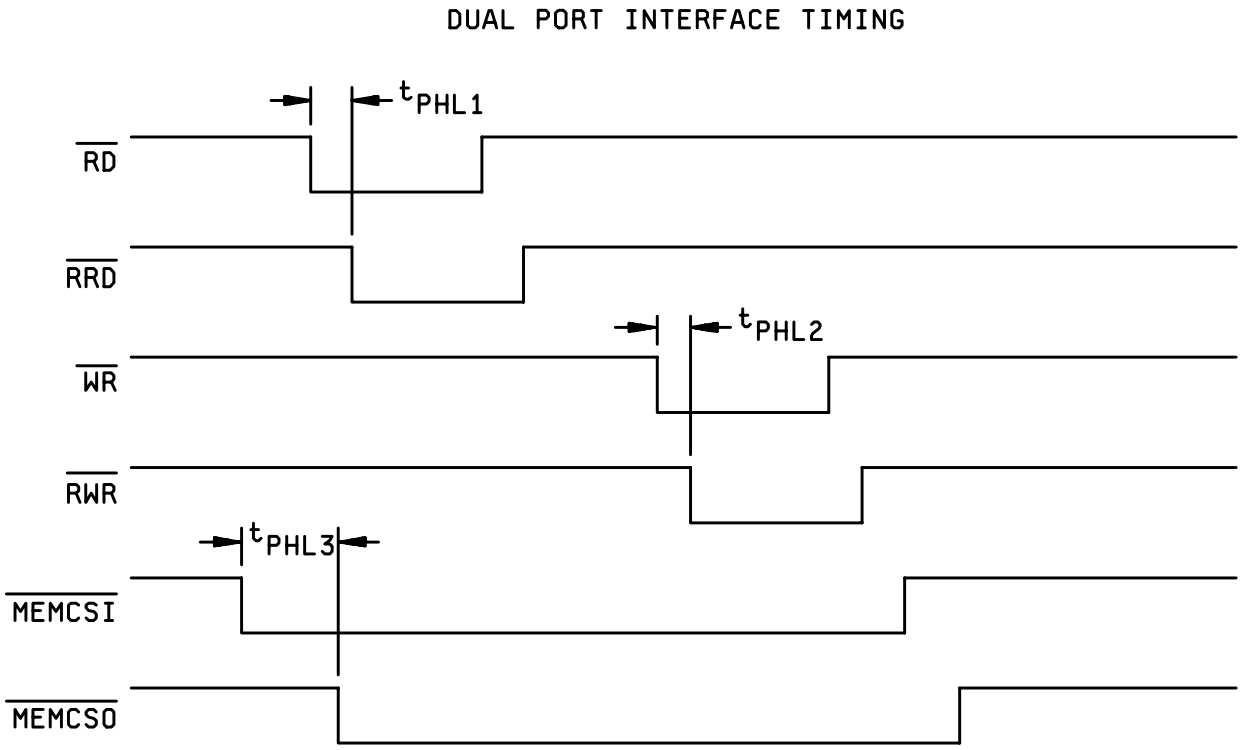


FIGURE 3. Switching test circuit and waveforms. - Continued

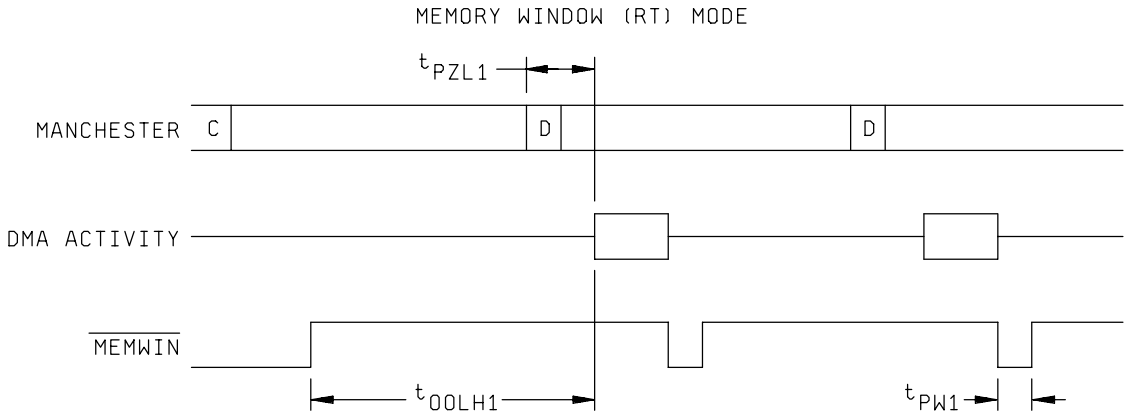


FIGURE 3. Switching test circuit and waveforms. - Continued

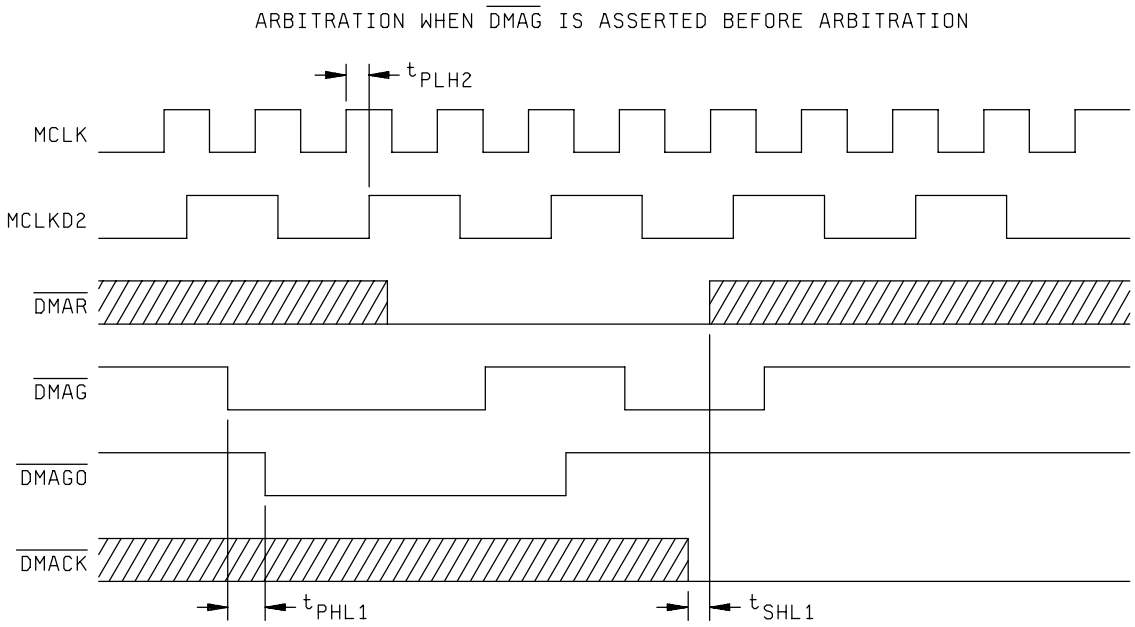


FIGURE 3. Switching test circuit and waveforms. - Continued

INTERRUPT LOG LIST ENTRY OPERATION TIMING

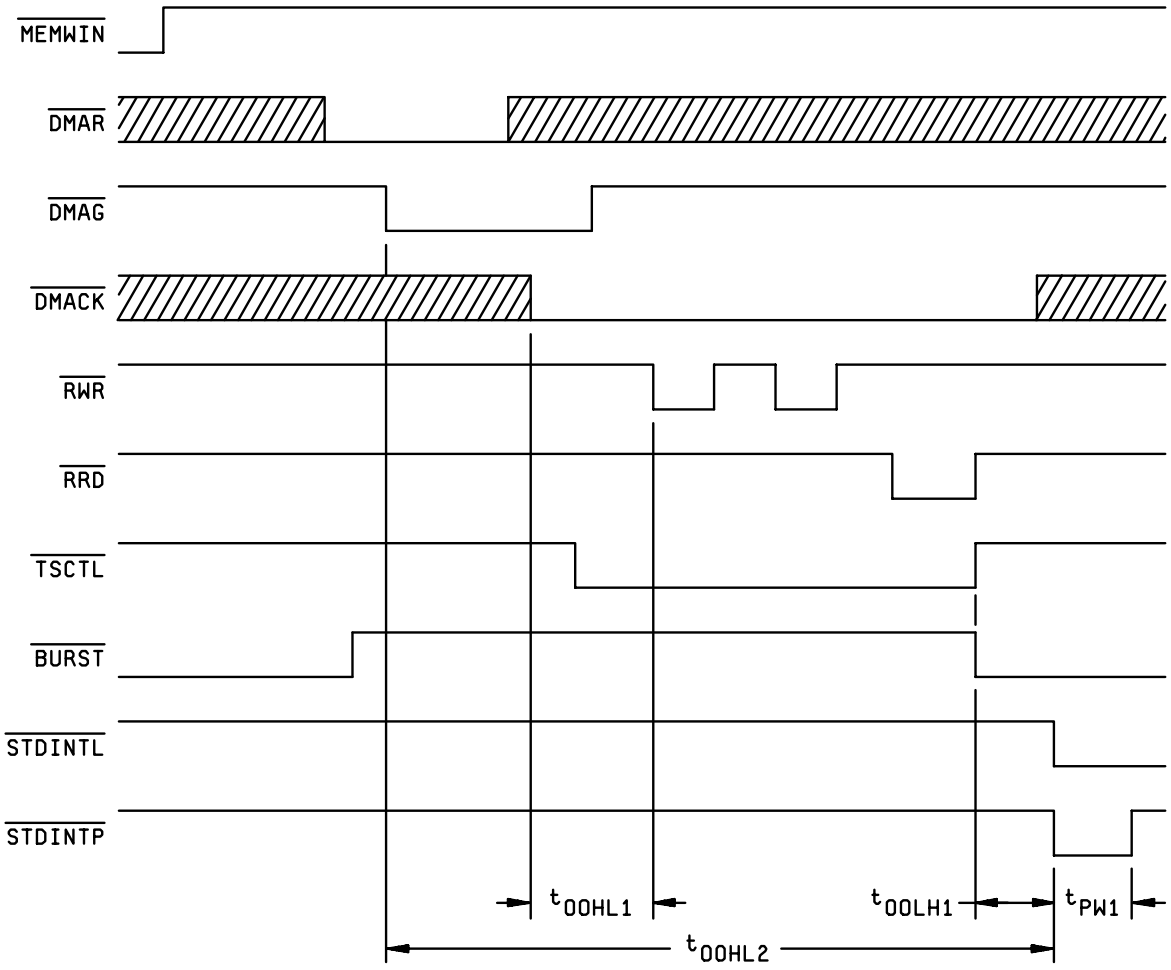


FIGURE 3. Switching test circuit and waveforms. - Continued

Open	V_{DD} = 5 V ±0.5 V	Ground
13 (K3), 14 (L2), 17 (L4), 18 (K6), 25 (K7), 26 (J7), 27 (L8), 38 (H11), 39 (G9), 40 (G10), 41 (G11), 44 (E9), 45 (E11), 46 (E10), 47 (F11), 48 (D11), 49 (D10), 50 (C11), 51 (B11), 52 (C10), 53 (A11), 54 (B10), 55 (B9), 56 (A10), 58 (B8), 67 (B5), 68 (A6), 69 (A4), 70 (B4), 71 (A3), 73 (B3), 74 (A1), 75 (B2), 76 (C2), 77 (B1), 78 (C1), 79 (D2), 80 (D1), 81 (F2), 82 (E2), 83 (E1)	10 (J2), 11 (L1), 12 (K2), 23 (L6), 24 (L7), 28 (K8), 43 (F9), 57 (A9), 59 (A8), 61 (B7), 64 (C6), 84 (E3)	1 (F3), 2 (F1), 3 (G1), 4 (G2) 5 (G3), 6 (H1), 7 (H2), 8 (J1), 9 (K1), 15 (L3), 16 (K4), 19 (K5), 20 (L5), 21 (J5), 22 (J6), 29 (L9), 30 (L10), 31 (K9), 32 (L11), 33 (K10), 34 (J10), 35 (K11), 36 (J11), 37 (H10), 42 (F10), 60 (C7), 62 (A7), 63 (B6), 65 (C5), 66 (A5), 72 (A2)

Pin grid array pin identification is in parenthesis. Flat pack pin numbers is not in parenthesis.

FIGURE 4. Radiation exposure circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of table IV method 5010 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT} and C_{IO}) shall be measured only for the initial test and after process or design changes which may affect input/output capacitance. A minimum sample size of 10 devices with zero rejects shall be required.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - - -	- - - -	- - - -
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 7, 8A	1, 2, 7, 8A 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 7 ,8A	1, 2, 7, 8A	1, 2, 7, 8A
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in Table IIB herein shall be required when specified and the Delta values shall be completed with reference to the zero hour electrical parameter.

Table IIB. Delta limits

Parameter	Condition	Limits
Q_{IDD}	T_A = 25°C	±10% of measured value or 35 µA whichever is greater

NOTE: If device is tested at or below 35 µA no deltas are required. Deltas are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q, and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelarated aging test. Accelaerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accoradance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accoradance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upse or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

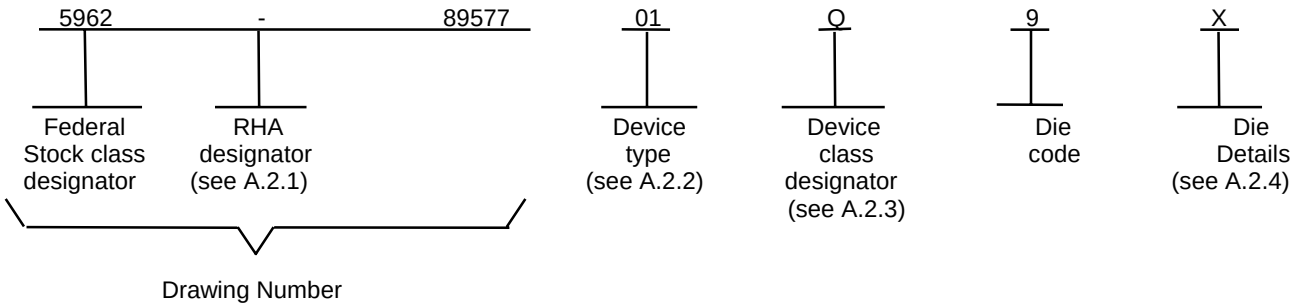
e. Occurrence of latchup (SEP).

APPENDIX A FORMS A PART OF SMD 5962-89577

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN shall be as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT1553BCRTM	Bus controller, remote terminal and monitor

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die Physical dimensions.

Die Types	Die detail designator	Figure number
01	A	A-1
	B	B-1

A.1.2.4.2 Die Bonding pad locations and Electrical functions.

Die Types	Die detail designator	Figure number
01	A	A-1
	B	B-1

A.1.2.4.3 Interface Materials.

Die Types	Die detail designator	Figure number
01	A	A-1
	B	B-1

A.1.2.4.4 Assembly related information.

Die Types	Die detail designator	Figure number	Substrate potential
01	A	A-1	Tied to V_{DD}
	B	B-1	Tied to V_{SS}

A.1.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

A.2 APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item Requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die Physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1 and B-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1and B-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A-1 and B-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figures A-1 and B-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.5 of the body of this document.

A.3.3 Electrical performance characteristics and post- irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 QUALITY ASSURANCE PROVISIONS

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer Lot acceptance for Class V product using the criteria defined within MIL-STD-883 TM 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 TM2010 or the alternate procedures allowed within MIL-STD-883 TM5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined with MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of Supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS

o DIE PHYSICAL DIMENSIONS

Die Size:	394 mils. x 394 mils.
Die Thickness:	17.5 +/- 1 mils.

o INTERFACE MATERIALS

Top Metallization:	Si Al Cu 9 kÅ-12.5kÅ
Backside Metallization	None: Backgrind
Glassivation	
Type:	PSG
Thickness	10 KÅ +/- 2.kÅ
Substrate:	EPI on single crystal silicon

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Tied to V_{DD}
Special assembly instructions:	None

FIGURE A-1

DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS

o DIE PHYSICAL DIMENSIONS

Die Size:	394 mils. x 394 mils.
Die Thickness:	17.5 +/- 1 mils.

o INTERFACE MATERIALS

Top Metallization:	Si Al Cu 9 kÅ-12.5kÅ
Backside Metallization	None: Backgrind
Glassivation	
Type:	PSG
Thickness	10 KÅ +/- 2.kÅ
Substrate:	EPI on single crystal silicon

o ASSEMBLY RELATED INFORMATION

Substrate Potential:	Tied to V_{SS}
Special assembly instructions:	None

FIGURE B-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
1	-0.0035	0.1840	V_{SS}
2	-0.0099	0.1840	No connect
3	-0.0163	0.1840	D7
4	-0.0226	0.1840	No connect
5	-0.0290	0.1840	No connect
6	-0.0354	0.1840	D6
7	-0.0418	0.1840	No connect
8	-0.0482	0.1840	D5
9	-0.0545	0.1840	No connect
10	-0.0609	0.1840	D4
11	-0.0673	0.1840	No connect
12	-0.0737	0.1840	No connect
13	-0.0800	0.1840	No connect
14	-0.0864	0.1840	D3
15	-0.0928	0.1840	No connect
16	-0.0992	0.1840	D2
17	-0.1056	0.1840	No connect
18	-0.1119	0.1840	D1
19	-0.1183	0.1840	No connect
20	-0.1247	0.1840	No connect
21	-0.1311	0.1840	No connect
22	-0.1374	0.1840	D0
23	-0.1438	0.1840	No connect
24	-0.1502	0.1840	MRST
25	-0.1566	0.1840	No connect
26	-0.1630	0.1840	BCRTSEL
27	-0.1743	0.1840	No connect
28	-0.1904	0.1676	No connect
29	-0.1904	0.1564	LOCK
30	-0.1904	0.1500	No connect
31	-0.1904	0.1436	TAZ
32	-0.1904	0.1372	No connect
33	-0.1904	0.1308	TA0
34	-0.1904	0.1245	No connect
35	-0.1904	0.1181	No connect
36	-0.1904	0.1117	No connect
37	-0.1904	0.1053	RAZ
38	-0.1904	0.0990	No connect
39	-0.1904	0.0926	RA0
40	-0.1904	0.0862	No connect
41	-0.1904	0.0798	TBZ
42	-0.1904	0.0734	No connect
43	-0.1904	0.0671	TB0
44	-0.1904	0.0607	No connect
45	-0.1904	0.0543	RBZ
46	-0.1904	0.0479	No connect
47	-0.1904	0.0416	No connect
48	-0.1904	0.0352	RB0
49	-0.1904	0.0288	No connect
50	-0.1904	0.0224	MHX12

NOTE: The die center is the coordinate origin (0,0).

Figure A-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
51	-0.1904	0.0160	No connect
52	-0.1904	0.0097	No connect
53	-0.1904	0.0033	V_{SS}
54	-0.1904	-0.0031	V_{DD}
55	-0.1904	-0.0095	No connect
56	-0.1904	-0.0158	No connect
57	-0.1904	-0.0222	No connect
58	-0.1904	-0.0286	EXTOVR
59	-0.1904	-0.0350	No connect
60	-0.1904	-0.0414	No connect
61	-0.1904	-0.0477	TIMERON
62	-0.1904	-0.0541	No connect
63	-0.1904	-0.0605	CHA/B
64	-0.1904	-0.0669	No connect
65	-0.1904	-0.0732	No connect
66	-0.1904	-0.0796	No connect
67	-0.1904	-0.0860	COMSTR
68	-0.1904	-0.0924	No connect
69	-0.1904	-0.0988	RTA0
70	-0.1904	-0.1051	No connect
71	-0.1904	-0.1115	RTA1
72	-0.1904	-0.1179	No connect
73	-0.1904	-0.1243	RTA2
74	-0.1904	-0.1307	No connect
75	-0.1904	-0.1370	No connect
76	-0.1904	-0.1434	No connect
77	-0.1904	-0.1498	RTA3
78	-0.1904	-0.1562	No connect
79	-0.1905	-0.1625	RTA4
80	-0.1904	-0.1743	No connect
81	-0.1743	-0.1905	No connect
82	-0.1629	-0.1905	RTPTY
83	-0.1566	-0.1905	No connect
84	-0.1502	-0.1905	A0
85	-0.1438	-0.1905	No connect
86	-0.1374	-0.1905	No connect
87	-0.1311	-0.1905	No connect
88	-0.1247	-0.1905	A1
89	-0.1183	-0.1905	No connect
90	-0.1119	-0.1905	A2
91	-0.1056	-0.1905	No connect
92	-0.0992	-0.1905	A3
93	-0.0928	-0.1905	No connect
94	-0.0864	-0.1905	A4
95	-0.0800	-0.1905	No connect

NOTE: The die center is the coordinate origin (0,0).

Figure A-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
96	-0.0737	-0.1905	No connect
97	-0.0673	-0.1905	No connect
98	-0.0609	-0.1905	A5
99	-0.0545	-0.1905	No connect
100	-0.0482	-0.1905	A6
101	-0.0418	-0.1905	No connect
102	-0.0354	-0.1905	A7
103	-0.0290	-0.1905	No connect
104	-0.0226	-0.1905	BCRTMSEL
105	-0.0163	-0.1905	No connect
106	-0.0099	-0.1905	V_{SS}
107	-0.0035	-0.1905	V_{DD}
108	0.0029	-0.1905	No connect
109	0.0093	-0.1905	No connect
110	0.0156	-0.1905	A8
111	0.0220	-0.1905	No connect
112	0.0284	-0.1905	A9
113	0.0348	-0.1905	No connect
114	0.0411	-0.1905	A10
115	0.0475	-0.1905	No connect
116	0.0539	-0.1905	A11
117	0.0603	-0.1905	No connect
118	0.0667	-0.1905	No connect
119	0.0730	-0.1905	No connect
120	0.0794	-0.1905	A12
121	0.0858	-0.1905	No connect
122	0.0922	-0.1905	A13
123	0.0985	-0.1905	No connect
124	0.1049	-0.1905	A14
125	0.1113	-0.1905	No connect
126	0.1177	-0.1905	No connect
127	0.1241	-0.1905	No connect
128	0.1305	-0.1905	A15
129	0.1369	-0.1904	No connect
130	0.1433	-0.1904	RWR
131	0.1497	-0.1904	No connect
132	0.1560	-0.1905	RRD
133	0.1676	-0.1905	No connect
134	0.1840	-0.1743	No connect
135	0.1840	-0.1624	MEMSCO
136	0.1840	-0.1562	No connect
137	0.1840	-0.1498	TSCTL
138	0.1840	-0.1434	No connect
139	0.1840	-0.1370	No connect
140	0.1840	-0.1307	No connect
141	0.1840	-0.1243	DMAR
142	0.1840	-0.1179	No connect

NOTE: The die center is the coordinate origin (0,0).

Figure A-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
143	0.1840	-0.1115	DMAG
144	0.1840	-0.1051	No connect
145	0.1840	-0.0988	No connect
146	0.1840	-0.0924	No connect
147	0.1840	-0.0860	DMACK
148	0.1840	-0.0796	No connect
149	0.1840	-0.0732	MEMCSI
150	0.1840	-0,0669	No connect
151	0.1840	-0.0605	$\overline{WR}$
152	0.1840	-0.0541	No connect
153	0.1840	-0.0477	No connect
154	0.1840	-0.0414	$\overline{RD}$
155	0.1840	-0.0350	No connect
156	0.1840	-0.0286	$\overline{CS}$
157	0.1840	-0.0222	No connect
158	0.1840	-0.0158	No connect
159	0.1840	-0.0095	V_{SS}
160	0.1840	-0.0031	V_{DD}
161	0.1840	0.0033	No connect
162	0.1840	0.0097	No connect
163	0.1840	0.0160	No connect
164	0.1840	0.0224	MCLK
165	0.1840	0.0288	No connect
166	0.1840	0.0352	AEN
167	0.1840	0.0416	No connect
168	0.1840	0.0479	No connect
169	0.1840	0.0543	DMAGO
170	0.1840	0.0607	No connect
171	0.1840	0.0671	STDINTL
172	0.1840	0.0734	No connect
173	0.1840	0.0798	STDINTP
174	0.1840	0.0862	No connect
175	0.1840	0.0926	HPINT
176	0.1840	0.0990	No connect
177	0.1840	0.1053	No connect
178	0.1840	0.1117	No connect
179	0.1840	0.1181	MCLKD2
180	0.1840	0.1245	No connect
181	0.1840	0.1308	SSYSF
182	0.1840	0.1372	No connect
183	0.1840	0.1436	TEST
184	0.1840	0.1500	No connect
185	0.1840	0.1564	BURST
186	0.1840	0.1676	No connect
187	0.1676	0.1840	No connect

NOTE: The die center is the coordinate origin (0,0).

Figure A-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
188	0.1559	0.1840	BCRTF
189	0.1496	0.1840	No connect
190	0.1432	0.1840	D15
191	0.1368	0.1840	No connect
192	0.1304	0.1840	D14
193	0.1241	0.1840	No connect
194	0.1177	0.1840	No connect
195	0.1113	0.1840	No connect
196	0.1049	0.1840	D13
197	0.0985	0.1840	No connect
198	0.0922	0.1840	D12
199	0.0858	0.1840	No connect
200	0.0794	0.1840	D11
201	0.0730	0.1840	No connect
202	0.0667	0.1840	No connect
203	0.0603	0.1840	No connect
204	0.0539	0.1840	D10
205	0.0475	0.1840	No connect
206	0.0411	0.1840	D9
207	0.0348	0.1840	No connect
208	0.0284	0.1840	No connect
209	0.0220	0.1840	D8
210	0.0156	0.1840	No connect
211	0.0093	0.1840	No connect
212	0.0029	0.1840	V_{DD}

NOTE: The die center is the coordinate origin (0,0).

Figure A-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
1	165	185.9	V_{SS}
2	158.7	185.9	V_{DQ}
3	152.4	185.9	No Connect
4	146.1	185.9	BF
5	139.8	185.9	No Connect
6	133.5	185.9	D15
7	127.2	185.9	D14
8	120.9	185.9	No Connect
9	114.6	185.9	No Connect
10	108.3	185.9	No Connect
11	102	185.9	D13
12	95.7	185.9	No Connect
13	89.4	185.9	D12
14	83.1	185.9	D11
15	76.8	185.9	V_{SQ}
16	70.5	185.9	No Connect
17	64.2	185.9	No Connect
18	57.9	185.9	No Connect
19	51.6	185.9	D10
20	45.3	185.9	No Connect
21	39	185.9	D9
22	32.7	185.9	No Connect
23	26.4	185.9	D8
24	20.1	185.9	No Connect
25	13.8	185.9	V_{DQ}
26	7.5	185.9	V_{SS}
27	1.2	185.9	V_{DD}
28	-5.1	185.9	V_{SQ}
29	-11.4	185.9	No Connect
30	-17.7	185.9	No Connect
31	-24	185.9	No Connect
32	-30.3	185.9	D7
33	-36.6	185.9	No Connect
34	-42.9	185.9	D6
35	-49.2	185.9	No Connect
36	-55.5	185.9	D5
37	-61.8	185.9	No Connect
38	-68.1	185.9	No Connect
39	-74.4	185.9	V_{SQ}
40	-80.7	185.9	D4
41	-87	185.9	No Connect
42	-93.3	185.9	D3
43	-99.6	185.9	No Connect
44	105.9	185.9	D2
45	112.2	185.9	No Connect
46	118.5	185.9	No Connect
47	124.8	185.9	D0
48	131.1	185.9	MRST
49	137.4	185.9	BCRTSEL
50	143.7	185.9	No Connect

NOTE: The die center is the coordinate origin (0,0).

Figure B-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
51	150	185.9	No Connect
52	156.3	185.9	No Connect
53	162.6	185.9	V_{SQ}
54	168.9	185.9	V_{SS}
55	184.6	170.2	V_{DD}
56	184.6	163.9	V_{DQ}
57	184.6	157.4	No Connect
58	184.6	151.1	No Connect
59	184.6	144.8	LOCK
60	184.6	138.5	No Connect
61	184.6	132.2	TAZ
62	184.6	125.9	TAO
63	184.6	119.6	No Connect
64	184.6	113.3	RAZ
65	184.6	107.1	No Connect
66	184.6	100.8	No Connect
67	184.6	94.5	RAO
68	184.6	88.2	No Connect
69	184.6	81.9	V_{SQ}
70	184.6	75.6	TBZ
71	184.6	69.3	TBO
72	184.6	63	No Connect
73	184.6	56.7	No Connect
74	184.6	50.4	RBZ
75	184.6	44.1	RBO
76	184.6	37.8	No Connect
77	184.6	31.5	MHz12
78	184.6	25.2	No Connect
79	184.6	18.9	V_{DQ}
80	184.6	12.6	V_{DD}
81	184.6	6.3	V_{SS}
82	184.6	0	V_{SQ}
83	184.6	-6.3	No Connect
84	184.6	-12.6	No Connect
85	184.6	-18.9	No Connect
86	184.6	-25.2	No Connect
87	184.6	-31.5	EXTOVR
88	184.6	-37.8	No Connect
89	184.6	-44.1	TIMERON
90	184.6	-50.4	No Connect
91	184.6	-56.7	$\overline{CHAB}$
92	184.6	-63	No Connect
93	184.6	-69.3	V_{SQ}
94	184.6	-75.6	CMDST
95	184.6	-81.9	$\overline{V_{DD}}$
96	184.6	-88.2	No Connect
97	184.6	-94.5	RTA0
98	184.6	-100.8	RTA1
99	184.6	-107.1	No Connect
100	184.6	-113.4	No Connect

NOTE: The die center is the coordinate origin (0,0).

Figure B-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
101	184.6	-119.7	RTA2
102	184.6	-126	RTA3
103	184.6	-132.3	RTA4
104	184.6	-138.6	No Connect
105	184.6	-144.9	No Connect
106	184.6	-151.2	No Connect
107	184.6	-157.5	No Connect
108	184.6	-164	V_{SQ}
109	184.6	-170.3	V_{DD}
110	168.9	-186	V_{SS}
111	162.6	-186	V_{DQ}
112	156.3	-186	No Connect
113	150	-186	RTPTY
114	143.7	-186	No Connect
115	137.4	-186	A0
116	131.1	-186	No Connect
117	124.8	-186	A1
118	118.5	-186	No Connect
119	112.2	-186	No Connect
120	105.9	-186	No Connect
121	-99.6	-186	A2
122	-93.3	-186	No Connect
123	-87	-186	No Connect
124	-80.7	-186	V_{SQ}
125	-74.4	-186	A4
126	-68.1	-186	No Connect
127	-61.8	-186	No Connect
128	-55.5	-186	A5
129	-49.2	-186	No Connect
130	-42.9	-186	No Connect
131	-36.6	-186	A6
132	-30.3	-186	A7
133	-24	-186	No Connect
134	-17.7	-186	V_{DQ}
135	-11.4	-186	V_{SS}
136	-5.1	-186	V_{DD}
137	1.2	-186	V_{SQ}
138	7.5	-186	No Connect
139	13.8	-186	No Connect
140	20.1	-186	No Connect
141	26.4	-186	A8
142	32.7	-186	No Connect
143	39	-186	A9
144	45.3	-186	No Connect
145	51.6	-186	A10
146	57.9	-186	No Connect
147	64.2	-186	No Connect
148	70.5	-186	V_{SQ}
149	76.8	-186	A11
150	83.1	-186	No Connect

NOTE: The die center is the coordinate origin (0,0).

Figure B-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
151	89.4	-186	A12
152	95.7	-186	No Connect
153	102	-186	A13
154	108.3	-186	A14
155	114.6	-186	No Connect
156	120.9	-186	A15
157	127.2	-186	No Connect
158	133.5	-186	$\overline{RWR}$
159	139.8	-186	No Connect
160	146.1	-186	$\overline{RRD}$
161	152.4	-186	No Connect
162	158.7	-186	V_{SQ}
163	165	-186	V_{SS}
164	180.7	-170.3	V_{DD}
165	180.7	-163.8	V_{DQ}
166	180.7	-157.5	No Connect
167	180.7	-151.2	MEMCSO
168	180.7	-144.9	No Connect
169	180.7	-138.6	TSCTL
170	180.7	-132.3	No Connect
171	180.7	-126	DMAR
172	180.7	-119.7	No Connect
173	180.7	-113.4	No Connect
174	180.7	-107.1	DMAG
175	180.7	-100.8	No Connect
176	180.7	-94.5	DMAAK
177	180.7	-88.2	MEMCSI
178	180.7	-81.9	V_{SQ}
179	180.7	-75.6	No Connect
180	180.7	-69.3	No Connect
181	180.7	-63	No Connect
182	180.7	-56.7	$\overline{WR}$
183	180.7	-50.4	No Connect
184	180.7	-44.1	$\overline{RD}$
185	180.7	-37.8	No Connect
186	180.7	-31.5	$\overline{CS}$
187	180.7	-25.2	No Connect
188	180.7	-18.9	V_{DQ}
189	180.7	-12.6	V_{SS}
190	180.7	-6.3	V_{DD}
191	180.7	0	V_{SQ}
192	180.7	6.3	No Connect
193	180.7	12.6	No Connect
194	180.7	18.9	No Connect
195	180.7	25.2	MCLK
196	180.7	31.5	No Connect
197	180.7	37.8	AEN
198	180.7	44.1	No Connect
199	180.7	50.4	DMAGO
200	180.7	56.7	No Connect

NOTE: The die center is the coordinate origin (0,0).

Figure B-1

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
201	180.7	63	No Connect
202	180.7	69.3	V_{SQ}
203	180.7	75.6	STDINT
204	180.7	81.9	STDPUL
205	180.7	88.2	No Connect
206	180.7	94.5	HPINT
207	180.7	100.8	MCKD2
208	180.7	107.1	No Connect
209	180.7	113.4	SSYSF
210	180.7	119.7	No Connect
211	180.7	126	TEST
212	180.7	132.3	No Connect
213	180.7	138.6	BURST
214	180.7	144.9	No Connect
215	180.7	151.2	No Connect
216	180.7	157.6	No Connect
217	180.7	163.9	V_{SQ}
218	180.7	170.2	V_{DD}

NOTE: The die center is the coordinate origin (0,0).

Figure B-1

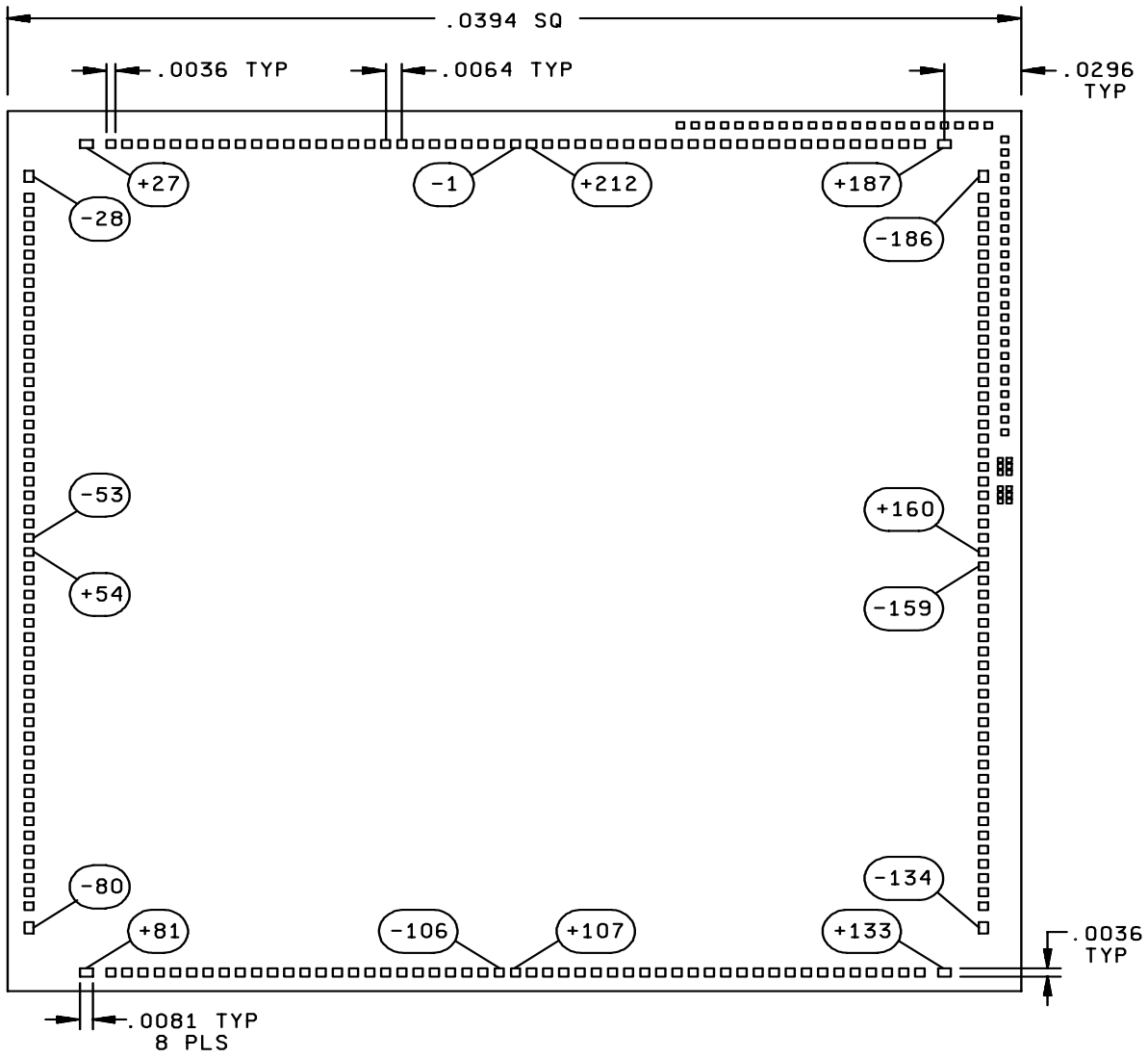


Figure A-1

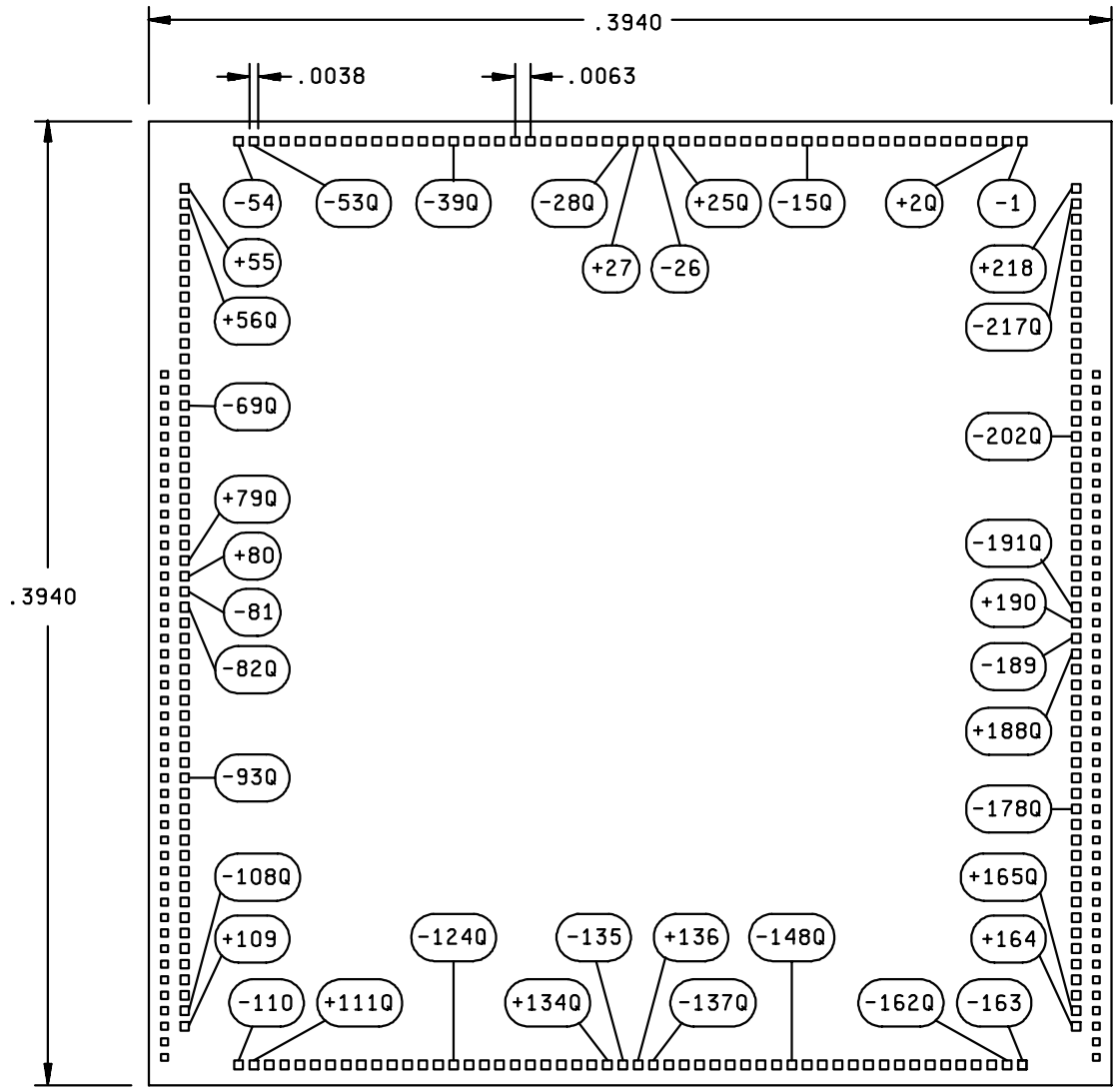


Figure B-1

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 02-07-23

Approved sources of supply for SMD 5962-89577 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard Microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8957701XA	65342	UT1553BCRTMGA
5962-8957701XC	65342	UT1553BCRTMGC
5962-8957701YA	65342	UT1553BCRTMWA
5962-8957701YC	65342	UT1553BCRTMWC
5962-8957701ZA	65342	UT1553BCRTMAA
5962-8957701ZC	65342	UT1553BCRTMAC
5962H8957701XA	65342	UT1553BCRTMGAH
5962H8957701XC	65342	UT1553BCRTMGCH
5962H8957701YA	65342	UT1553BCRTMWAH
5962H8957701YC	65342	UT1553BCRTMWCH
5962H8957701ZA	65342	UT1553BCRTMAAH
5962H8957701ZC	65342	UT1553BCRTMACH
5962H8957701VXA	65342	UT1553BCRTMVGAH
5962H8957701VXC	65342	UT1553BCRTMVGCH
5962H8957701VYA	65342	UT1553BCRTMVWAH
5962H8957701VYC	65342	UT1553BCRTMVWCH
5962H8957701VZA	65342	UT1553BCRTMVAAH
5962H8957701VZC	65342	UT1553BCRTMVACH

Standard Microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/
5962-8957701Q9A	65342	UT1553BCRTM-Q DIE
5962-8957701V9A	65342	UT1553BCRTM-V DIE
5962H8957701Q9A	3/	
5962H8957701V9A	3/	
5962H8957701Q9B	65342	UT1553BCRTM-Q DIE
5962H8957701V9B	65342	UT1553BCRTM-V DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	UTMC Aeroflex Microelectronics Systems Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486