Dual-Channel Digital Isolators, Enhanced System-Level ESD Reliability

ADuM3210/ADuM3211

FEATURES

- Enhanced system-level ESD performance per IEC 61000-4-x
- High temperature operation: 125°C
- Default low output
- Narrow body, RoHS-compliant, 8-lead SOIC
- Low power operation
  - 5 V operation
    - 1.6 mA per channel maximum @ 0 Mbps to 2 Mbps
    - 3.7 mA per channel maximum @ 10 Mbps
  - 3 V operation
    - 1.4 mA per channel maximum @ 0 Mbps to 2 Mbps
    - 2.4 mA per channel maximum @ 10 Mbps
- 3 V/5 V level translation
- High data rate: dc to 10 Mbps (NRZ)
- Precise timing characteristics
  - 3 ns maximum pulse-width distortion at 5 V operation
  - 3 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/μs
- Safety and regulatory approvals
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE Certificate of Conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
    - V_{IORM} = 560 V peak

APPLICATIONS

- Size-critical multichannel isolation
- SPI interface/data converter isolation
- RS-232/RS-422/RS-485 transceiver isolation
- Digital field bus isolation
- Gate drive interfaces

GENERAL DESCRIPTION

The ADuM321x[1] are dual-channel, digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The two channels of the ADuM321x are independent isolation channels and are available in two channel configurations with two different data rates up to 10 Mbps (see the Ordering Guide). They operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The ADuM321x isolators have a default output low characteristic in comparison to the ADuM3200/ADuM3201 models that have a default output high characteristic. The ADuM321x are also available in 125°C temperature grade.

In comparison to the ADuM120x isolator, the ADuM321x isolators contain various circuit and layout changes providing increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM120x or ADuM321x products is strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

FUNCTIONAL BLOCK DIAGRAMS

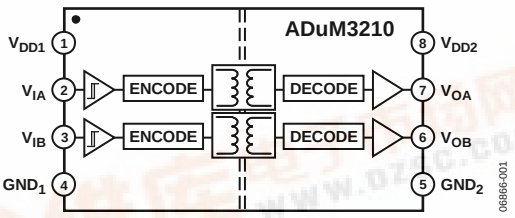

Figure 1. ADuM3210 Functional Block Diagram

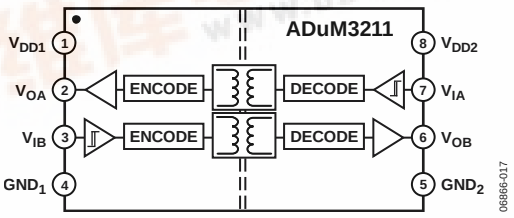

Figure 2. ADuM3211 Functional Block Diagram

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. C

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REVISION HISTORY

9/09 –Rev. B to Rev. C

Added ADuM3210A and ADuM3211A ... Throughout
Changes to General Description Section ... 1
Reformatted Electrical Characteristics Tables ... 3
Moved Truth Tables Section ... 14
Changes to Ordering Guide ... 20

7/09—Rev. A to Rev. B

Added ADuM3211 ... Throughout
Changes to Specifications Section ... 3
Added Table 16 ... 19
Added Figure 5 and Table 18 ... 20
Added Figure 11 ... 21
Changes to Power Consumption Section ... 23
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9/08—Rev. Sp0 to Rev. A

Changes to Features and General Description Sections ... 1
Changes to Specifications Section ... 3
Changes to Recommended Operating Conditions Section ... 11
Changes to Ordering Guide ... 18

7/07—Revision Sp0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105° OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		50	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			20			15	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			5			3	ns	
Opposing-Direction	t_{PSKOD}			20			15	ns	
Output Rise/Fall Time	t_R/t_F		2.5			2.5		ns	10% to 90%

Table 2.

Parameter	Symbol	1 Mbps—A Grade, B Grade			10 Mbps–B Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
ADuM3210	I_{DD1}		1.3	1.7		3.5	4.6	mA	
	I_{DD2}		1.0	1.6		1.7	2.8	mA	
ADuM3211	I_{DD1}		1.1	1.5		2.6	3.4	mA	
	I_{DD2}		1.3	1.8		3.1	4.0	mA	

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3 V, 105°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: ADuM3210 supply voltages 2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; ADuM3211 supply voltages 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		60	20		60	ns	50% input to 50% output
Pulse Width Distortion	PWD								$\lvert t_{PLH} - t_{PHL} \rvert$
ADuM3210				5			3	ns	
ADuM3211				6			4	ns	
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			29			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			5			3	ns	
Opposing-Direction	t_{PSKOD}			29			22	ns	
Output Rise/Fall Time	t_R/t_F		3.0			3.0		ns	10% to 90%

Table 5.

		1 Mbps—A Grade, B Grade			10 Mbps—B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
SUPPLY CURRENT									
ADuM3210	I_{DD1}		0.8	1.3		2.0	3.2	mA	
	I_{DD2}		0.7	1.0		1.1	1.7	mA	
ADuM3211	I_{DD1}		0.7	1.3		1.5	2.1	mA	
	I_{DD2}		0.8	1.6		1.9	2.4	mA	

Table 6. For All Models

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0.1	3.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V, 105°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: ADuM3210 supply voltages 4.5 V ≤ V_{DD1} ≤ 5.5V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; ADuM3211 supply voltages 4.5 V ≤ V_{DD1} ≤ 5.5V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

Table 7.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			29			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			5			3	ns	
Opposing-Direction	t_{PSKOD}			29			22	ns	
Output Rise/Fall Time	t_R/t_F		3.0			3.0		ns	10% to 90%

Table 8.

		1 Mbps—A Grade, B Grade			10 Mbps—B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
SUPPLY CURRENT									
ADuM3210	I_{DD1}		1.3	1.7		3.5	4.6	mA	
	I_{DD2}		0.7	1.0		1.1	1.7	mA	
ADuM3211	I_{DD1}		1.1	1.5		2.6	3.4	mA	
	I_{DD2}		0.8	1.6		1.9	2.4	mA	

Table 9. For All Models

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}	0.8		0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0.1	V_{DDX}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	V_{DDX} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V, 105°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3 V, V_{DD2} = 5.0 V. Minimum/maximum specifications apply over the entire recommended operation range: ADuM3210 supply voltages 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; ADuM3211 supply voltages 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD								$\lvert t_{PLH} - t_{PHL} \rvert$
ADuM3210				5			3	ns	
ADuM3211				6			4	ns	
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			29			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			15			3	ns	
Opposing-Direction	t_{PSKOD}			29			22	ns	
Output Rise/Fall Time	t_R/t_F		2.5			2.5		ns	10% to 90%

Table 11.

		1 Mbps—A Grade, B Grade			10 Mbps—B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
SUPPLY CURRENT									
ADuM3210	I_{DD1}		0.8	1.3		2.0	3.2	mA	
	I_{DD2}		1.0	1.6		1.7	2.8	mA	
ADuM3211	I_{DD1}		0.7	1.3		1.5	2.1	mA	
	I_{DD2}		1.3	1.8		3.1	4.0	mA	

Table 12. For All Models

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}	0.4		0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0. 1	V_{DDX}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	V_{DDX} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 13.

Parameter		Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			15	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing-Direction	t_{PSKOD}			15	ns	
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%

Table 14.

		1 Mbps			10 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT									
ADuM3210	I_{DD1}		1.3	1.7		3.5	4.6	mA	
	I_{DD2}		1.0	1.6		1.7	2.8	mA	
ADuM3211	I_{DD1}		1.1	1.5		2.6	3.4	mA	
	I_{DD2}		1.3	1.8		3.1	4.0	mA	

Table 15. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 16.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
Data Rate				10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		60	ns	50% input to 50% output
Pulse Width Distortion	PWD					$\lvert t_{PLH} - t_{PHL} \rvert$
ADuM3210				3	ns	
ADuM3211				4	ns	
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			22	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing-Direction	t_{PSKOD}			22	ns	
Output Rise/Fall Time	t_R/t_F		3.0		ns	10% to 90%

Table 17.

		1 Mbps			10 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT									
ADuM3210	I_{DD1}		0.8	1.3		2.0	3.2	mA	
	I_{DD2}		0.7	1.0		1.1	1.7	mA	
ADuM3211	I_{DD1}		0.7	1.3		1.5	2.1	mA	
	I_{DD2}		0.8	1.6		1.9	2.4	mA	

Table 18. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0.1	3.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 19.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
Data Rate				10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			22	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing-Direction	t_{PSKOD}			22	ns	
Output Rise/Fall Time	t_R/t_F		3.0		ns	10% to 90%

Table 20.

		1 Mbps			10 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT									
ADuM3210	I_{DD1}		1.3	1.7		3.5	4.6	mA	
	I_{DD2}		0.7	1.0		1.1	1.7	mA	
ADuM3211	I_{DD1}		1.1	1.5		2.6	3.4	mA	
	I_{DD2}		0.8	1.6		1.9	2.4	mA	

Table 21. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}	0.8		0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0.1	V_{DDX}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	V_{DDX} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3 V, V_{DD2} = 5.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 22.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
Data Rate				10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD					$\lvert t_{PLH} - t_{PHL} \rvert$
ADuM3210				3	ns	
ADuM3211				4	ns	
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			22	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing-Direction	t_{PSKOD}			22	ns	
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%

Table 23.

		1 Mbps			10 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT									
ADuM3210	I_{DD1}		0.8	1.3		2.0	3.2	mA	
	I_{DD2}		1.0	1.6		1.7	2.8	mA	
ADuM3211	I_{DD1}		0.7	1.3		1.5	2.1	mA	
	I_{DD2}		1.3	1.8		3.1	4.0	mA	

Table 24. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDX}			V	
Logic Low Input Threshold	V_{IL}	0.4		0.3 V_{DDX}	V	
Logic High Output Voltages	V_{OH}	V_{DDX} − 0.1	V_{DDX}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDX} − 0.5	V_{DDX} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM}= 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 25.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		41		°C/W	

[1] The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM321x are approved by the organizations listed in Table 26.

Table 26.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single/basic 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms(1131 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM321x is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM321x is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 27.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 28.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	150	mA
Side 2 Current		I_{S2}	160	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

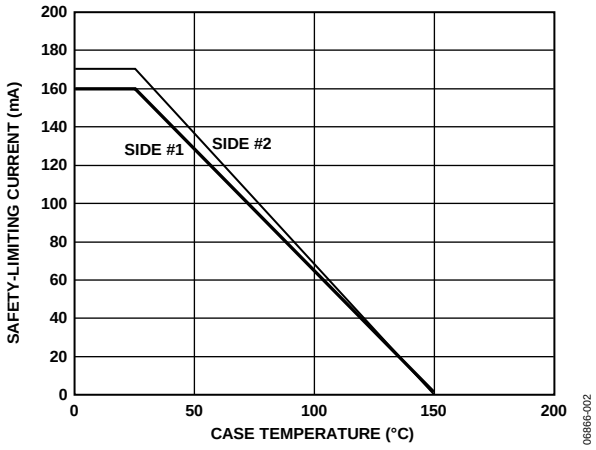


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 29.

Parameter	Symbol	Rating
Operating Temperature	T_A	
ADuM3210AR/ADuM3210BR		−40°C to +105°C
ADuM3211AR/ADuM3211BR		−40°C to +105°C
ADuM3210TR/ADuM3211TR		−40°C to +105°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	
ADuM3210AR/ADuM3210BR		2.7 V to 5.5 V
ADuM3210TR/ADuM3211AR ADuM3211BR/ADuM3211TR		3 V to 5.5 V
Input Signal Rise and Fall Times		1 ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 30.

Parameter	Symbol	Rating
Storage Temperature	T_{ST}	−55°C to +150°C
Ambient Operating Temperature	T_A	−40°C to +105°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	−0.5 V to +7.0 V
Input Voltage[1, 2]	V_{IA}, V_{IB}	−0.5 V to V_{DDI} + 0.5 V
Output Voltage[1, 2]	V_{OA}, V_{OB}	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	I_O	−35 mA to +35 mA
Common-Mode Transients[4]	CM_H, CM_L	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 3 for information on maximum allowable current for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 31. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

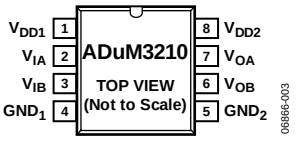


Figure 4. ADuM3210 Pin Configuration

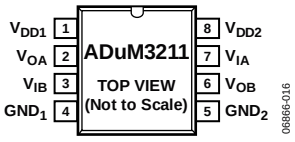


Figure 5. ADuM3211 Pin Configuration

Table 32. ADuM3210 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

Table 33. ADuM3211 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

TRUTH TABLES

Table 34. ADuM3210 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 µs of V_{DDI} power restoration
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration

Table 35. ADuM3211 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	L	Outputs return to the input state within 1 µs of V_{DDI} power restoration
X	X	Powered	Unpowered	L	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration

TYPICAL PERFORMANCE CHARACTERISTICS

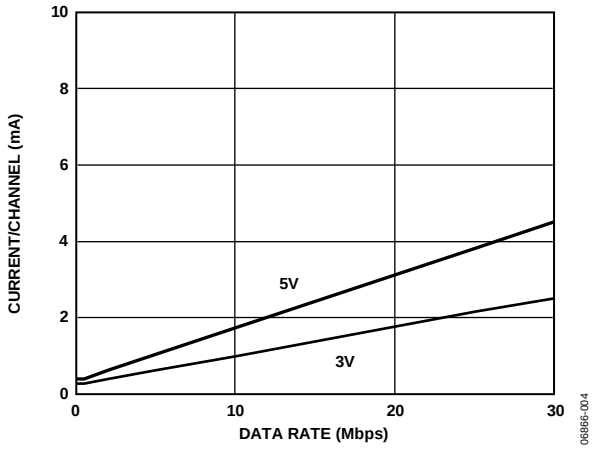


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

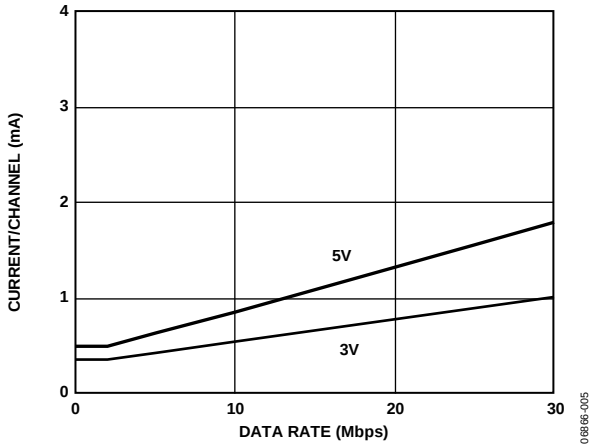


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

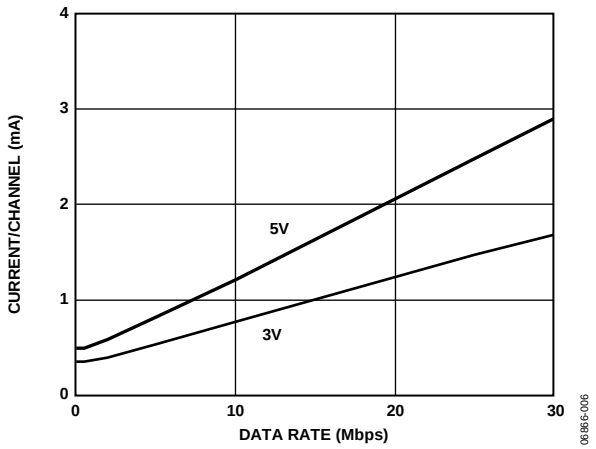


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

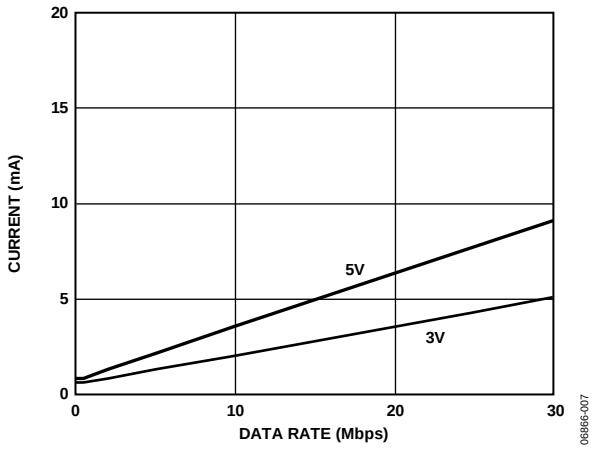


Figure 9. Typical ADuM3210 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

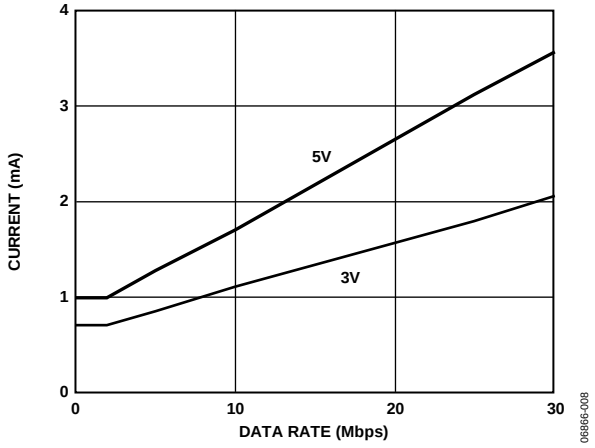


Figure 10. ADuM3210 Typical V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

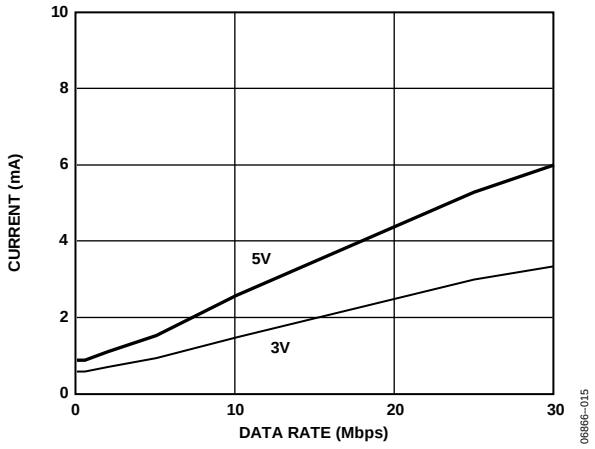


Figure 11. ADuM3211 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM321x digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM321x incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells were added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices is minimized by use of a guarding and isolation technique between the PMOS and NMOS devices.
- Areas of high electric field concentration are eliminated using 45° corners on metal traces.
- Supply pin overvoltage is prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM321x improves system-level ESD reliability, it is no substitute for a robust system-level design. For detailed recommendations on board layout and system-level design, see AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

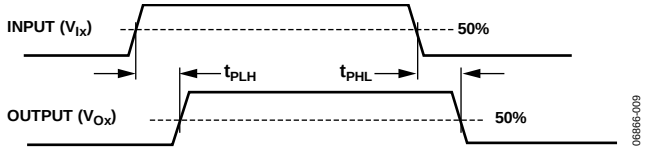


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM321x component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM321x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 2 µs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state (see Table 34 and Table 35) by the watchdog timer circuit.

The ADuM321x is immune to external magnetic fields. The limitation on the ADuM321x magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM321x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \Sigma\pi r_n^2, n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM321x and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 13.

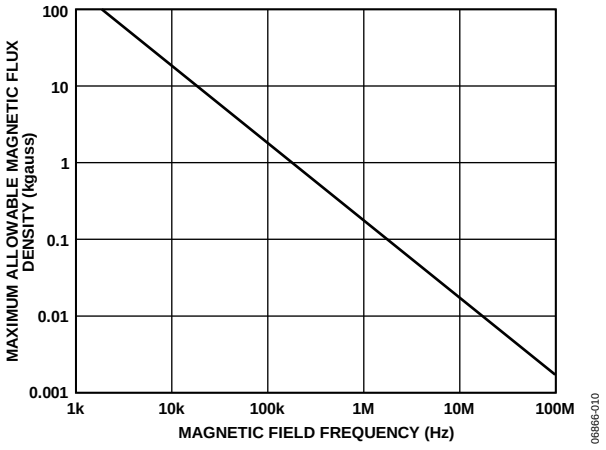


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM321x transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM321x is immune and can be affected only by extremely large currents operated at a high frequency and very close to the component. For the 1 MHz example, one would have to place a 0.5 kA current 5 mm away from the ADuM321x to affect the operation of the component.

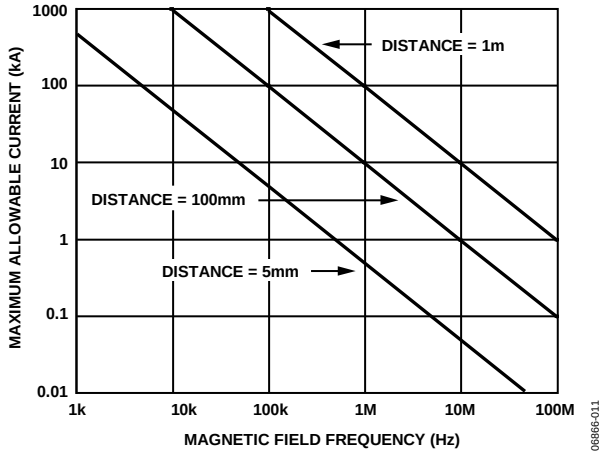


Figure 14. Maximum Allowable Current for Various Current-to-ADuM3210/ADuM3211 Spacings

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM321x isolator is a function of the supply voltage, channel data rate, and channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).
f_r is the input stage refresh rate (Mbps).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled.

Figure 6 provides per-channel input supply currents as a function of data rate. Figure 7 and Figure 8 provide per-channel output supply currents as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 11 provide total I_{DD1} and I_{DD2} supply current as a function of data rate for the ADuM3210 and ADuM3211 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM321x.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 31 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM321x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the most stringent. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 31 can be applied while maintaining the 50-year minimum lifetime provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 31.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

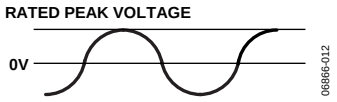


Figure 15. Bipolar AC Waveform

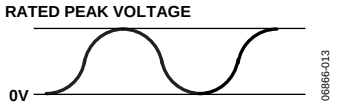


Figure 16. Unipolar AC Waveform

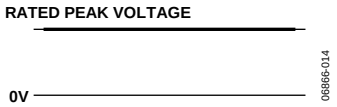
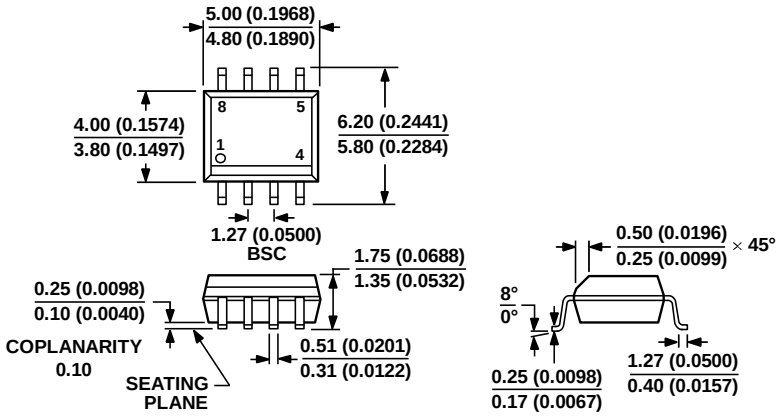


Figure 17. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 18. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Option[1]
ADuM3210ARZ[2]	2	0	1	100	5	−40°C to +105°C	R-8
ADuM3210ARZ-RL7[2]	2	0	1	100	5	−40°C to +105°C	R-8
ADuM3210BRZ[2]	2	0	10	50	3	−40°C to +105°C	R-8
ADuM3210BRZ-RL7[2]	2	0	10	50	3	−40°C to +105°C	R-8
ADuM3210TRZ[2]	2	0	10	50	3	−40°C to +125°C	R-8
ADuM3210TRZ-RL7[2]	2	0	10	50	3	−40°C to +125°C	R-8
ADuM3211ARZ[2]	1	1	1	100	6	−40°C to +105°C	R-8
ADuM3211ARZ-RL7[2]	1	1	1	100	6	−40°C to +105°C	R-8
ADuM3211BRZ[2]	1	1	10	50	4	−40°C to +105°C	R-8
ADuM3211BRZ-RL7[2]	1	1	10	50	4	−40°C to +105°C	R-8
ADuM3211TRZ[2]	1	1	10	50	4	−40°C to +125°C	R-8
ADuM3211TRZ-RL7[2]	1	1	10	50	4	−40°C to +125°C	R-8

[1] R-8 = 8-lead, narrow body SOIC_N.
[2] Z = RoHS Compliant Part.

NOTES