

I.8 Volt-only Flash Memory Technology

Technology Background



July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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Introduction

AMD's flash technology leadership and innovation have produced a new generation of single-power-supply flash memory devices. The **Am29SL800B** is the first of a new family of Super Low voltage flash memory devices from AMD. This device performs read, program, and erase operations using only a single power supply down to **1.8 volts**, while maintaining performance comparable to 5.0 volt-only technology. The device offers all the features of AMD's industry-standard 2.7 volt-only Am29LV800B device at substantially reduced power consumption, making it the ideal choice for low-power, battery-operated portable applications such as cellular phones, PDAs, and pagers.

The following is an abbreviated list of the Am29SL800B distinctive characteristics:

- 1.8 V to 2.2 V device V_{CC} operating range**
- 1 mA typical active read current at 1 MHz (5 mA at 5 MHz)**
- 10 mA typical active program/erase current**
- 0.2 μ A typical standby current**
- Automatic Sleep Mode (no turn-on penalty)**
- Minimum 1,000,000 program/erase cycle guarantee per sector**

For a complete list of features, operational description and specifications see publication number 21545 (the Am29SL800B data sheet). The remainder of this document will focus on the fundamentals of flash technology at 1.8 volts.

What Makes Operating at 1.8 Volts so Difficult?

Flash memory technology is a very complex science, as exemplified by the small number of volume manufacturers present today in the world. Performing this science from a single 1.8 volt source, while maintaining performance and reliability with minimal die size impact, was a significant engineering achievement. The development of this product resulted in several patents specific to low voltage operation.

There are three major operations that a flash memory device performs: program, erase and read. The following is an examination of each of these processes.

The Flash Read Operation

AMD's flash memory cell is composed of a single stacked gate transistor. The gate structure of this transistor consists of a polysilicon control gate located directly above a polysilicon floating gate, separated by a dielectric (see Figure 1). The amount of charge present on the floating gate affects the turn-on threshold (V_t) of the transistor. Imagine the charge on the

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floating gate as a voltage source in series with the control gate. Charge is moved on and off the floating gate by the program and erase operations respectively. If the voltage on the control gate exceeds the resultant V_t , the transistor begins to conduct, and a current (I_{ds}) proportional to this voltage begins to flow from the drain to the source. The proportionality factor is the transconductance of the transistor (G_m). The current I_{ds} flows in the bit line through an active load. It is the voltage developed across the load that is compared to a preset reference (V_{ref}) to determine the state of the cell (see Figure 2).

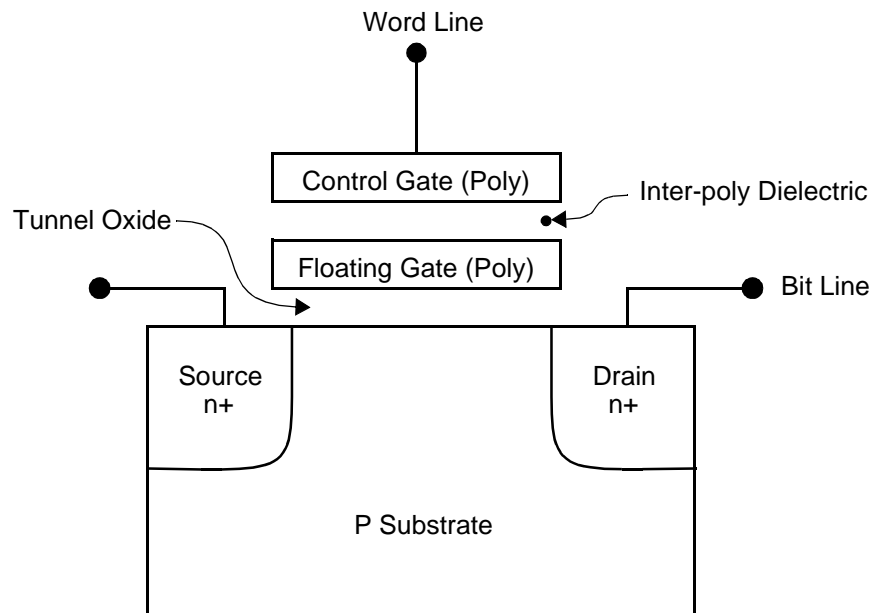


Figure 1. AMD Flash Memory Cell

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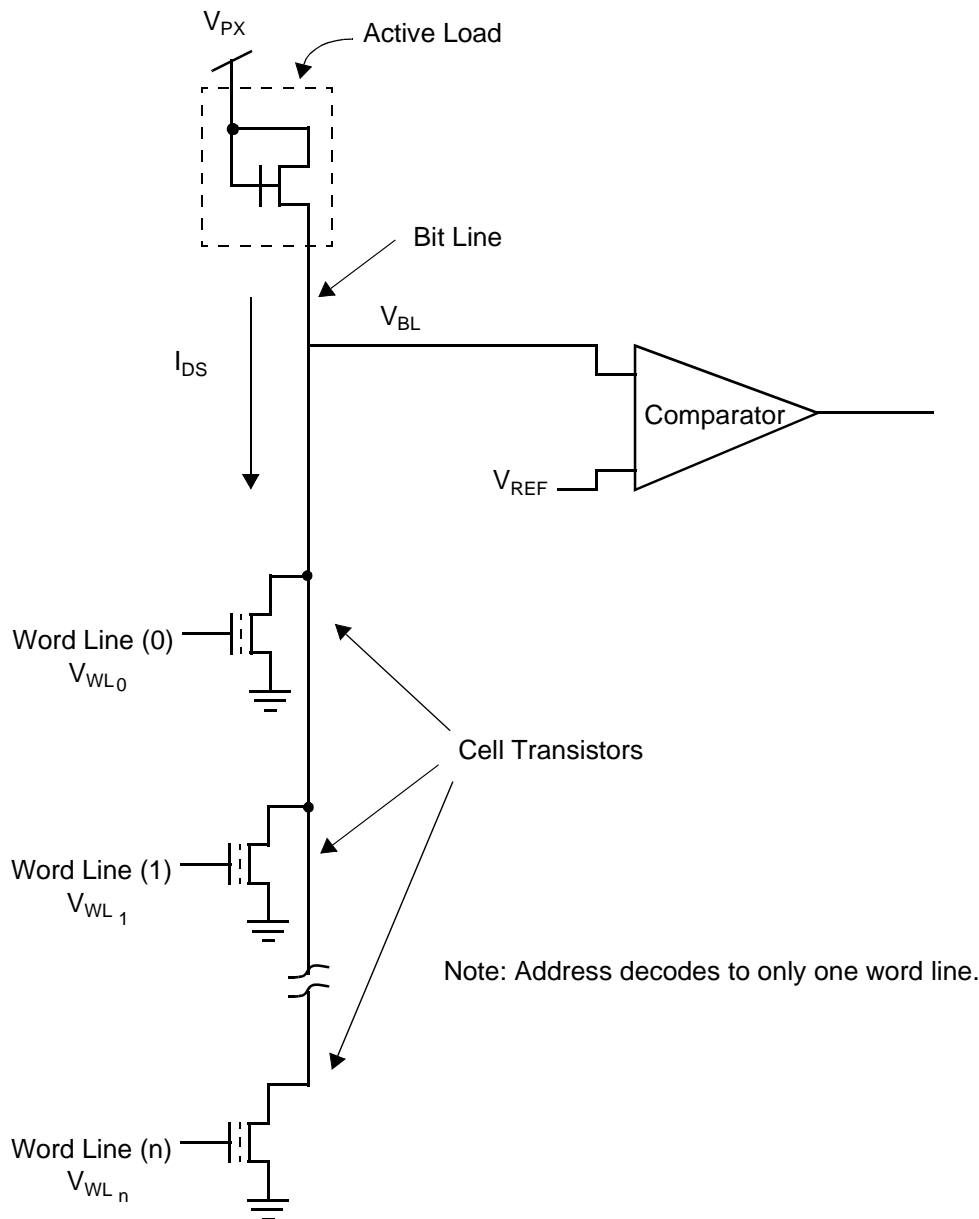


Figure 2. Flash Cell Sensing

At this point a few observations can be made. The operation of the flash memory cells and sensing circuits is analog in nature with transistors operating in their active (linear) regions. Reliable operation of these circuits in the presence of external noise requires margin in the design. Cycle endurance of the device is dependent on cell V_t ; that is, the difference in V_t between the programmed state and the erased state. Finally, the performance of these circuits is a function of the voltages applied. Reducing the external supply voltage would appear to

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have severe negative impact on the read operation of the device in terms of reliability and performance.

To achieve robust read operation, an approach similar to that used in the 2.7 volt-only devices is taken. These devices utilize a dynamic circuit design approach. There are many advantages to this approach, including high performance and reduced power consumption. For this discussion, however, the main advantage is the limited time that elevated currents are required to complete the read access. This allows use of very silicon-efficient booster circuits on the wordline to provide the required control gate voltage. This enables the Super Low voltage family to use the same proven, highly reliable memory cell structure as in the 5 volt-only and 2.7 volt-only device families. Operating at the same V_t levels results in the same guaranteed high endurance (1,000,000 cycles minimum). An additional benefit to the booster circuit is the noise isolation it provides. The booster circuit essentially decouples the word line allowing line levels to be tightly controlled during the access.

To achieve performance at 1.8 volts, a new thin gate oxide transistor is used in the peripheral circuits. Reducing the gate oxide thickness from 150 Å down to 100 Å increases the transconductance (gain) of these transistors while reducing their threshold voltage. The net effect is to bring circuit operating currents up to a level consistent with the desired level of performance and active power consumption.

The proven AMD flash memory cell structure and the innovative techniques discussed above combine to deliver a highly reliable, high performance device capable of operating from a single 1.8 volt supply.

The Flash Programming Operation

The Program operation deposits electrons (charge) on the cell's floating gate. In AMD devices, Channel Hot Electron injection (CHE) is the mechanism utilized. CHE depends on imparting more kinetic energy to the channel electrons than can be transferred to the silicon lattice, thus making them "hot." In order for these electrons to make it onto the floating gate, they need to become hot enough (gain enough energy) to overcome the tunnel oxide potential barrier. Creating the environment for CHE requires a high bias on the control gate (8 V) and elevated drain voltage (5 V). Reducing the external supply voltage presents an obvious challenge.

A charge pump approach is utilized to support the CHE programming environment. Generating the voltage levels required isn't trivial, but the real issue is in managing the current. Silicon efficient implementation demands maintaining a strict power budget. This is

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accomplished through a unique bit sensing circuit in conjunction with a proprietary, intelligent programming algorithm. Together they exploit the fact that at the location selected for programming, only the bits to be programmed with a logic “0” require programming current (the other bits are already at logic “1” from a previous erase operation). Managing the current makes this approach silicon efficient, while maintaining overall programming performance.

The Flash Erase Operation

The erase operation removes electrons (charge) from the cell’s floating gate. In AMD devices Fowler-Nordheim tunneling (FN) is the mechanism employed. FN tunneling is a quantum mechanical process whose explanation is beyond the scope of this paper. Understanding the constraints this mechanism places on the design is our interest here. FN tunneling requires an electric field across the tunneling oxide. The strength of this field for a given oxide thickness determines the erase performance. Again, reducing the external supply voltage while maintaining performance presents yet another challenge.

AMD pioneered its patented Negative Gate Erase (NGE) technique several years ago as a solution to the problem of maintaining erase performance without requiring multiple external voltage sources. The NGE technique has proven to be a key enabler of AMD’s ability to offer first 5 volt-only followed by 2.7 volt-only, 2.2 volt-only, and now 1.8 volt-only devices. NGE takes advantage of the superposition principle of electric fields. Applying a negative bias to the control gate and a small positive bias to the source generates the resultant field intensity required for FN tunneling (see Figure 3). The key here is the current reduction as a result of reducing the source voltage. Keeping the source voltage low suppresses avalanche-dominated conduction between the source and the substrate, reducing overall internal power generating requirements. NGE therefore allows a charge pump approach to be utilized with negligible impact on die size, while maintaining erase performance.

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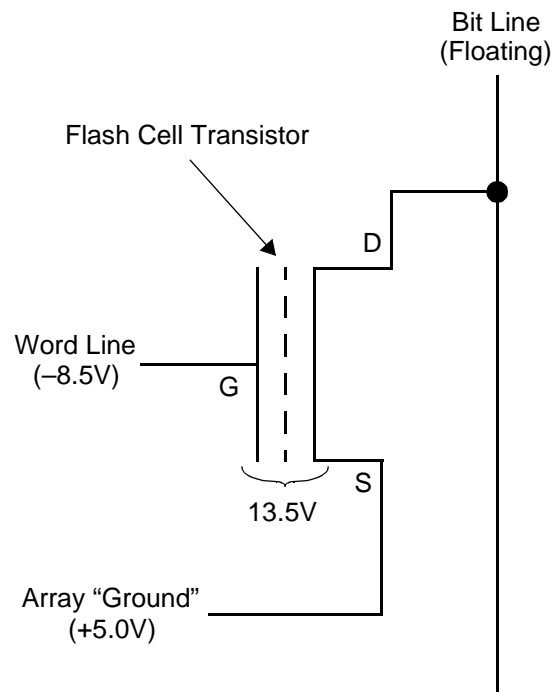


Figure 3. AMD Negative Gate Erase

Summary

Technology leadership, experience and creativity of AMD's engineering resources have once again lead the arrival of the next generation of low voltage flash memory devices. These Super Low voltage high performance devices operate from a single 1.8 volt supply, reducing active read current to just 1.0 mA (at 1.0 MHz). The reduced power consumption, silicon efficient design, and industry-leading guaranteed minimum endurance of 1,000,000 cycles combine to make this device family an ideal choice for cost-sensitive, battery-powered applications.



One AMD Place
P.O. Box 3453
Sunnyvale,
California 94088-3453
USA
(408) 732-2400
(800) 538-8450
TWX: 910-339-9280
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TECHNICAL SUPPORT

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Fax: +44-(0)1276 803298
BBS: +44-(0)1276 803211
FRANCE: 0800 90 8621
GERMANY: 089-450-53199
ITALY: 1678-77224
EUROPE E-mail: euro.tech@amd.com
FAR EAST Fax: (852) 2956-0599
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