

National Semiconductor

100353 Low Power 8-Bit Register

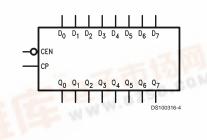
General Description

The 100353 contains eight D-type edge triggered, master/ slave flip-flops with individual inputs (D_n) , true outputs (Q_n) , a clock input (CP), and a common clock enable pin (CEN). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the CEN input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.



The 100353 output drivers are designed to drive 50Ω termination to -2.0V. All inputs have 50 k Ω pull-down resistors.

Logic Symbol



Features

Low power operation

Pin Names

 $D_0 - D_7$

- 2000V ESD protection
- Voltage compensated operating range = -4.2V to -5.7V

Data Inputs

Description

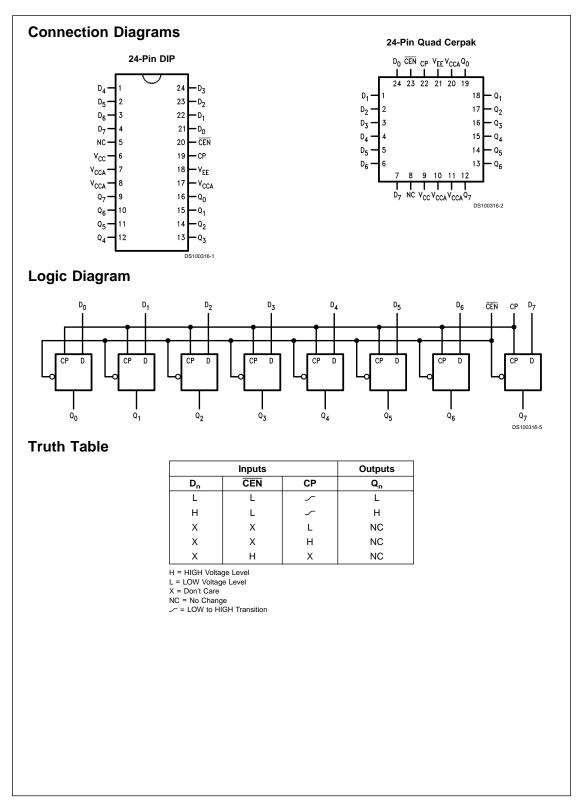
Available to MIL-STD-883



August 1998

CEN Clock Enable Input CP Clock Input (Active Rising Edge) Data Outputs $Q_0 - Q_7$ NC No Connect DS100316 © 1998 National Semiconductor Corporation www.national.com





Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impared

Storage Temperature (T _{STG})	–65°C to +150°C
Maximum Junction Temperature (T _J)	
Ceramic	+175°C
V _{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V _{EE} to + 0.5V
Output Current (DC Output HIGH)	–50 mA

ESD (Note 2)

Recommended Operating Conditions

Case Temperature (T_C) Military -55°C to +125°C Supply Voltage (V_{EE}) -5.7V to -4.2V Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

≥2000V

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

 V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_{C} = -55°C to +125°C

Symbol	Parameter	Min	Max	Units	Tc	Conditions	Notes
V _{он}	Output HIGH Voltage	-1025	-870	mV	0°C to		
					+125°C		
		-1085	-870	mV	–55°C	V _{IN} = V _{IH} (Max) Loading	with (Notes 3, 4, 5)
V _{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to	or V_{IL} (Min) 50 Ω to	-2.0V
					+125°C		
		-1830	-1555	mV	–55°C		
V _{онс}	Output HIGH Voltage	-1035		mV	0°C to		
					+125°C		
		-1085		mV	–55°C	$V_{IN} = V_{IH}$ (Min) Loading	with (Notes 3, 4, 5)
V _{OLC}	Output LOW Voltage		-1610	mV	0°C to	or V _{IL} (Max) 50Ω to	-2.0V
					+125°C		
			-1555	mV	–55°C		
V _{IH}	Input HIGH Voltage	-1165	-870	mV	–55°C to	Guaranteed HIGH Signal for all I	nputs (Notes 3, 4, 5, 6
					+125°C		
VIL	Input LOW Voltage	-1830	-1475	mV	–55°C to	Guaranteed LOW Signal for all Ir	puts (Notes 3, 4, 5, 6
					+125°C		
l _{IL}	Input LOW Current	0.50		μA	–55°C to	$V_{EE} = -4.2V$	(Notes 3, 4, 5)
					+125°C	$V_{IN} = V_{IL}$ (Min)	
I _{IH}	Input HIGH Current		240	μA	0°C to	$V_{EE} = -5.7V$	(Notes 3, 4, 5)
					+125°C	$V_{IN} = V_{IH}$ (Max)	
			340	μA	–55°C		
I _{EE}	Power Supply Current				–55°C to	Inputs Open	
		-132	-42	mA	+125°C	$V_{EE} = -4.2V$ to $-5.7V$	(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

AC Electrical Characteristics

Symbol	Parameter Parameter		–55°C	T _c =	+25°C	T _c = -	+125°C	Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			I
f _{max}	Toggle Frequency	400		400		400		MHz	Figures 1, 2	(Note 10)

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AC Electrical Characteristics (Continued)

Symbol	Parameter	T _C = -55°C		T _C = +25°C		T _c = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t _{PLH}	Propagation Delay	0.70	3.30	0.80	3.10	0.80	3.50	ns		(Notes 7, 8,
t _{PHL}	CP to Output								Figures 1, 2	9, 11)
t _{TLH}	Transition Time	0.40	2.20	0.40	2.20	0.40	2.20	ns		(Note 10)
t _{THL}	20% to 80%, 80% to 20%									
t _s	Setup Time									
	D _n	0.30		0.30		0.30				
	CEN (Disable Time)	0.60		0.60		0.60		ns	Figures 1, 3	(Note 10)
	CEN (Release Time)	1.40		1.40		1.40				
t _h	Hold Time D _n	1.50		1.50		1.50		ns	Figures 1, 4	(Note 10)
t _{pw} (H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figures 1, 2	(Note 10)

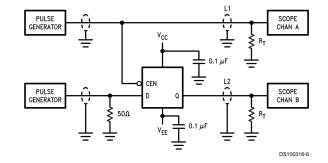
Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and -55°C, temperatures, Subgroups A10 and A11. Note 10: Not tested at +25°C, +125°C, and -55°C temperature (design characterization data).

Note 11: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

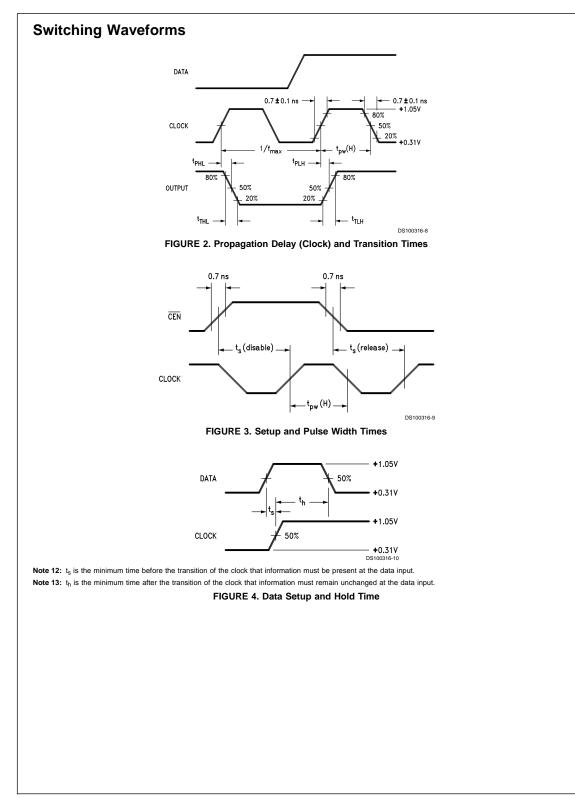


Notes:

 V_{CC} , V_{CCA} = +2V, V_{EE} = -2.5V

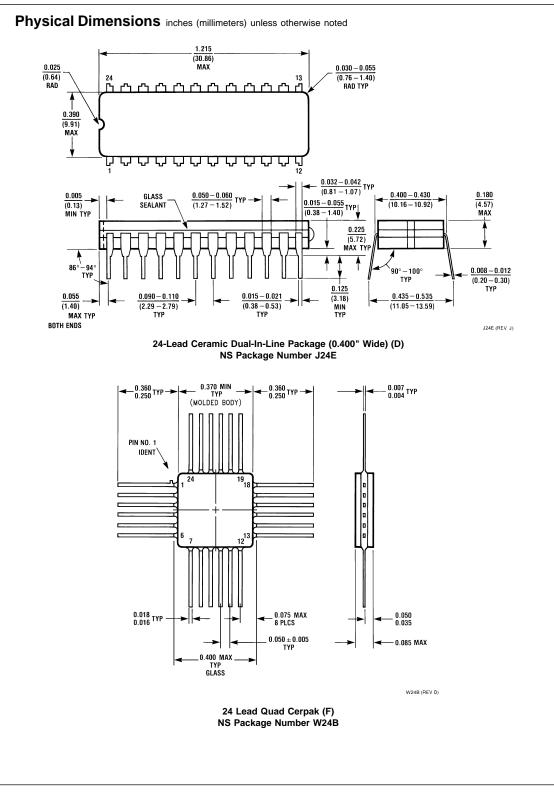
L1 and L2 = equal length 50Ω impedance lines R_T = 50 Ω terminator internal to scopeDecoupling 0.1 µF from GND to V_{CC} and V_{EE} All unused outputs are loaded with 50Ω to GNDC_L = Fixture and stray capacitance \leq 3 pF

FIGURE 1. AC, Toggle Frequency Test Circuit



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