REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes IAW NOR 5962-R410-97.	97-08-11	Monica L. Poelking
B	Add Radiation Hardness Assurance limits. Editorial changes throughout - jak	98-04-20	Monica L.Poelking

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD
MICROCIRCUIT DRAWING

CHECKED BY
Thomas J Ricciuti

THIS DRAWING IS AVAILABLE
FOR USE BY ALL
DEPARTMENTS

AND AGENCIES OF THE
DEPARTMENT OF DEFENSE

AMSC N/A

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
92-12-23

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216

MICROCIRCUITS, DIGITAL, ADVANCED CMOS, 4-BIT PRESETTABLE BINARY COUNTER, ASYNCHRONOUS RESET, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-91722**

SHEET 1 OF 23

DSCC FORM 2233
APR 97

5962-E228-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0035702 T01

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example.

5962	R	91722	01	V	E	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

________________ V ________________/
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	54ACT161	4-bit presettable binary counter, asynchronous reset, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Due to internal noise problems, device type 01 does not meet the minimum V_{IH} threshold limit that is characteristic of this technology family.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 2/
Output voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 2/
DC input diode current (I_{IK}) ($-0.5 \text{ V} \leq V_{IN} \leq V_{CC} + 0.5 \text{ V}$)	±20 mA
DC output diode current (I_{OK}) ($-0.5 \text{ V} \leq V_{OUT} \leq V_{CC} + 0.5 \text{ V}$)	±20 mA
DC output current (I_{OUT}) (per output pin)	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) (per pin)	±250 mA 3/
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions. 1/ 2/ 5/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	3.0 V dc 6/
Case operating temperature range (T_C)	-55°C to +125°C
Input edge rate ($\Delta v/\Delta t$) maximum (from V_{IN} = 0.8 V to 2.0 V, 2.0 V to 0.8 V)	125 mV/ns
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+24 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} and GND pins.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.

6/ For dynamic operation, a V_{IH} level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a $V_{IH} \geq 2.0$ V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system.

7/ Values will be added when they become available from the qualified source.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 State diagram. The state diagram shall be as specified on figure 4.

3.2.6 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.8 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

   (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

   (2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

Table I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified		Device type and Device class	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Positive input clamp voltage 3022	V_{IC+} 4/ 5/	For input under test, I_{IN} = 1.0 mA		All Q, V	0.0 V	1	0.4	1.5	V
			M, D, L, R	All V	0.0 V	1	0.4	1.5	
Negative input clamp voltage 3022	V_{IC-} 4/ 5/	For input under test, I_{IN} = -1.0 mA		All Q, V	Open	1	-0.4	-1.5	V
			M, D, L, R	All V	Open	1	-0.4	-1.5	
High level output voltage 3006	V_{OH} 4/ 5/ 6/	For all inputs affecting output under test, V_{IN} = 3.0 V or 0.8 V		All All	4.5 V	1, 2, 3	4.4		V
		For all other inputs, V_{IN} = V_{CC} or GND		All All	5.5 V		5.4		
		I_{OH} = -50 µA	M, D, L, R	All All	5.5 V	1	5.4		
		For all inputs affecting output under test, V_{IN} = 3.0 V or 0.8 V		All All	4.5 V	1, 2, 3	3.7		
		For all other inputs, V_{IN} = V_{CC} or GND	M, D, L, R	All All	4.5 V	1	3.7		
		I_{OH} = -24 mA		All All	5.5 V	1, 2, 3	4.7		
		For all inputs affecting output under test, V_{IN} = 3.0 V or 0.8 V		All All	5.5 V	1, 2, 3	3.85		
		For all other inputs, V_{IN} = V_{CC} or GND I_{OH} = -50 mA 7/	M, D, L, R	All All	5.5 V	1	3.85		
Low level output voltage 3007	V_{OL} 4/ 5/ 6/	For all inputs affecting output under test, V_{IN} = 3.0 V or 0.8 V		All All	4.5 V	1, 2, 3		0.1	V
		For all other inputs, V_{IN} = V_{CC} or GND		All All	5.5 V			0.1	
		I_{OL} = 50 µA	M, D, L, R	All All	5.5 V	1		0.1	
		For all inputs affecting output under test, V_{IN} = 3.0 V or 0.8 V		All M	4.5 V	1		0.4	
		For all other inputs, V_{IN} = V_{CC} or GND	M, D, L, R	All All	4.5 V	1		0.4	
		I_{OL} = 24 mA		All M	4.5 V	2, 3		0.5	
				All M	5.5 V	1		0.4	
						2, 3		0.5	
				All V	4.5 V	1, 3		0.4	
						2		0.5	
				All V	5.5 V	1, 3		0.4	
						2		0.5	
		For all inputs affecting output under test, V_{IN} = 3.0 V or 0.8 V		All All	5.5 V	1, 2, 3		1.65	
		For all other inputs, V_{IN} = V_{CC} or GND I_{OL} = 50 mA 7/	M, D, L, R	All All	5.5 V	1		1.65	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-91722**
		REVISION LEVEL B	SHEET 7

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ $+4.5 V \leq V_{CC} \leq +5.5 V$ unless otherwise specified		Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
							Min	Max	
Input capacitance 3012	C_{IN}	See 4.4.1c $T_C = +25°C$		All All	GND	4		10.0	pF
Power dissipation capacitance	C_{PD} 8/	See 4.4.1c $T_C = +25°C$, f = 1 MHz		All All	5.0 V	4		50	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 4/ 5/ 9/	For input under test, $V_{IN} = V_{CC} - 2.1$ V For all other inputs, $V_{IN} = V_{CC}$ or GND		All Q, V	5.5 V	3		1.6	mA
						1, 2		1.0	
				All M	5.5 V	1, 2, 3		1.6	
			M, D	All	5.5 V	1		1.6	
			L, R	All				3.5	
Quiescent supply current outputs high 3005	I_{CCH} 4/ 5/	For all inputs, $V_{IN} = V_{CC}$ or GND		All Q, V	5.5 V	1		2.0	µA
						2		40.0	
				All M	5.5 V	1		8.0	
						2, 3		160.0	
			M	All	5.5 V	1		100.0	
			D	All				1.0	mA
			L, R					3.5	
Quiescent supply current outputs low 3005	I_{CCL} 4/ 5/	For all inputs, $V_{IN} = V_{CC}$ or GND		All Q, V	5.5 V	1		2.0	µA
						2		40.0	
				All M	5.5 V	1		8.0	
						2, 3		160.0	
			M	All	5.5 V	1		100.0	
			D	All				1.0	mA
			L, R					3.5	
Input leakage current high 3010	I_{IH} 4/ 5/	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All Q, V	5.5 V	1		0.1	µA
						2		1.0	
				All M	5.5 V	1		0.1	
						2, 3		1.0	
			M, D, L, R	All All	5.5 V	1		0.1	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-91722**
		REVISION LEVEL B	SHEET **8**

TABLE I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ $+4.5\ V \leq V_{CC} \leq +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input leakage current low 3009	I_{IL} 4/ 5/	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND	All Q, V	5.5 V	1		-0.1	μA
					2		-1.0	
			All M	5.5 V	1		-0.1	
					2, 3		-1.0	
		M, D, L, R	All All	5.5 V	1		-0.1	
Low level ground bounce noise	V_{GBL} 10/	V_{LD} = 2.5 V I_{OL} = +24 mA (See figure 5)	All Q, V	4.5 V	4		1500	mV
High level ground bounce noise	V_{GBH} 10/	V_{LD} = 2.5 V I_{OH} = -24 mA (See figure 5)	All Q, V	4.5 V	4		1500	mV
Latch-up input/output over-voltage	I_{CC} (O/V1) 11/	$t_w \geq 100\ \mu s$, $t_{cool} \geq t_w$ $5\ \mu s \leq t_r \leq 5\ ms$ $5\ \mu s \leq t_f \leq 5\ ms$ V_{test} = 6.0 V V_{CCQ} = 5.5 V V_{over} = 10.5 V	All Q, V	5.5 V	2		200	mA
Latch-up input/output positive over-current	I_{CC} (O/I1+) 11/	$t_w \geq 100\ \mu s$, $t_{cool} \geq t_w$ $5\ \mu s \leq t_r \leq 5\ ms$ $5\ \mu s \leq t_f \leq 5\ ms$ V_{test} = 6.0 V V_{CCQ} = 5.5 V $I_{trigger}$ = +120 mA	All Q, V	5.5 V	2		200	mA
Latch-up input/output negative over-current	I_{CC} (O/I1-) 11/	$t_w \geq 100\ \mu s$, $t_{cool} \geq t_w$ $5\ \mu s \leq t_r \leq 5\ ms$ $5\ \mu s \leq t_f \leq 5\ ms$ V_{test} = 6.0 V V_{CCQ} = 5.5 V $I_{trigger}$ = -120 mA	All Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 11/	$t_w \geq 100\ \mu s$, $t_{cool} \geq t_w$ $5\ \mu s \leq t_r \leq 5\ ms$ $5\ \mu s \leq t_f \leq 5\ ms$ V_{test} = 6.0 V V_{CCQ} = 5.5 V V_{over} = 9.0 V	All Q, V	5.5 V	2		100	mA
Functional tests 3014	4/ 5/ 12/	V_{IL} = 0.4 V V_{IH} = 3.0 V Verify output V_{OUT}	All All	4.5 V	7, 8	L	H	
		M, D, L, R	All All		7	L	H	
			All M	5.5 V	7, 8	L	H	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-91722**
		REVISION LEVEL B	SHEET **9**

Table I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\text{ V} \le V_{CC} \le +5.5\text{ V}$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, CP to Qn (count mode) 3003	t_{PHL} t_{PLH} 4/ 5/ 13/	C_L = 50 pF minimum R_L = 500Ω	All M	4.5 V	9	1.0	9.5	ns
		(See figure 6) M, D, L, R	All All		9	1.0	9.5	
			All M		10, 11	1.0	10.5	
			All V		9, 11	1.0	9.5	
			All V		10	1.0	10.5	
Propagation delay time, CP to Qn (load mode) 3003	t_{PHL} t_{PLH} 4/ 5/ 13/	C_L = 50 pF R_L = 500Ω	All M	4.5 V	9	1.0	8.5	ns
		(See figure 6) M, D, L, R	All All		9	1.0	8.5	
			All M		10, 11	1.0	10.0	
			All V		9, 11	1.0	8.5	
			All V		10	1.0	10.0	
Propagation delay time, CP to TC 3003	t_{PHL} t_{PLH} 4/ 5/ 13/	C_L = 50 pF minimum R_L = 500Ω	All M	4.5 V	9	1.0	12.0	ns
		(See figure 6) M, D, L, R	All All		9	1.0	12.0	
			All M		10, 11	1.0	14.0	
			All V		9, 11	1.0	12.0	
			All V		10	1.0	14.0	
Propagation delay time, CET to TC 3003	t_{PHL} t_{PLH} 4/ 5/ 13/	C_L = 50 pF minimum R_L = 500Ω	All M	4.5 V	9	1.0	8.5	ns
		(See figure 6) M, D, L, R	All All		9	1.0	8.5	
			All M		10, 11	1.0	9.5	
			All V		9, 11	1.0	8.5	
			All V		10	1.0	9.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, MR to Qn 3003	t_{PHL} 4/ 5/ 13/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All M	4.5 V	9	1.0	8.5	ns
		M, D, L, R	All All		9	1.0	8.5	
			All M		10, 11	1.0	10.0	
			All V		9, 11	1.0	8.5	
			All V		10	1.0	10.0	
Propagation delay time, MR to TC 3003	t_{PHL} 4/ 5/ 13/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All M	4.5 V	9	1.0	10.0	ns
		M, D, L, R	All All		9	1.0	10.0	
			All M		10, 11	1.0	11.5	
			All V		9, 11	1.0	10.0	
			All V		10	1.0	11.5	
Maximum clock frequency 3003	f_{MAX} 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All All	4.5 V	9	95		MHz
					10, 11	85		
Input setup time, high or low PE to CP	t_s 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All M	4.5 V	9	8.5		ns
			All M		10, 11	11.0		
			All V		9, 11	8.5		
			All V		10	11.0		
Input setup time, high or low Pn to CP	t_s 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All M	4.5 V	9	9.5		ns
			All M		10, 11	13.0		
			All V		9, 11	9.5		
			All V		10	13.0		

See footnotes at end of table.

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Table I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input setup time, high or low CEP, CET to CP	t_s 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All M	4.5 V	9	5.5		ns
			All M		10, 11	7.0		
			All V		9, 11	5.5		
			All V		10	7.0		
Input hold time, high or low PE to CP	t_h 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All All	4.5 V	9, 10, 11	0.0		ns
Input hold time, high or low Pn to CP	t_h 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All All	4.5 V	9, 10, 11	0.0		ns
Input hold time, high or low CEP, CET to CP	t_h 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All All	4.5 V	9, 10, 11	0.5		ns
Clock pulse width, high or low (count and load modes)	t_w 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All All	4.5 V	9, 10, 11	5.0		ns
$\overline{\text{MR}}$ pulse width low	t_w 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All M	4.5 V	9	5.0		ns
			All M		10, 11	6.5		
			All V		9, 11	5.0		
			All V		10	6.5		
Recovery time, MR to CP	t_{rec} 14/	C_L = 50 pF minimum R_L = 500Ω (See figure 6)	All M	4.5 V	9	0.0		ns
			All M		10, 11	0.5		
			All V		9, 11	0.0		
			All V		10	0.5		

See footnotes on next sheet.

Table I. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. $T_C = +25°C$.
b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. $T_C = +25°C$.
c. All I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

Additional detailed information on qualified devices (i.e. pin for pin conditions and testing sequence) is available from the qualifying activity (DCSS-VQC) upon request.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$.

4/ RHA samples do not have to be tested at -55°C and +125°C prior to irradiation.

5/ When performing postirradiation electrical measurements for RHA level, $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$.

6/ For dynamic operation, a V_{IH} level between 2.0 V and 3.0 V may be recognized by this device as a high logic level input. For static operation, a $V_{IH} \geq 2.0$ V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system.

7/ Transmission driving tests are performed at $V_{CC} = 5.5$ V with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IL} = 3.0$ V or 0.8 V.

8/ Power dissipation capacitance (C_{PD}) determines the no load power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC}) f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$. The dynamic current consumption, $I_S = (C_{PD} + C_L) V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$. For both P_D and I_S: n is the number of device inputs at TTL levels; f is the frequency of the input signal; and d is the duty cycle of the input signal.

9/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.

10/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = i.e, ±24 mA) and 50 pF of load capacitance (see figure 5). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f = 3.5 \pm 1.5$ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (see figure 5). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

TABLE I. Electrical performance characteristics - Continued.

11/ See JEDEC STD. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$ and V_{over}, are to be accurate within ±5 percent.

12/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. $H \geq 2.5$ V, $L < 2.5$; high inputs = 3.0 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated. The V_{IH} level used for functional testing shall be 3.0 V ±0 percent.

13/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum AC limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

14/ This parameter shall be guaranteed, if not tested, to the limits in table I, herein.

Device type	01	
Case outlines	E, F	2
Terminal number	Terminal symbol	
1	$\overline{\text{MR}}$	NC
2	CP	$\overline{\text{MR}}$
3	P0	CP
4	P1	P0
5	P2	P1
6	P3	NC
7	CEP	P2
8	GND	P3
9	$\overline{\text{PE}}$	CEP
10	CET	GND
11	Q3	NC
12	Q2	$\overline{\text{PE}}$
13	Q1	CET
14	Q0	Q3
15	TC	Q2
16	V_{CC}	NC
17	- - -	Q1
18	- - -	Q0
19	- - -	TC
20	- - -	V_{CC}

PIN Description	
Terminal Symbol	Description
CEP	Count enable parallel control input
CET	Count enable trickle control input
CP	Clock pulse timing input (active rising edge)
$\overline{\text{MR}}$	Asynchronous master reset control input (active low)
Pn	Parallel data inputs (n = 0 to 3)
$\overline{\text{PE}}$	Parallel enable control input (active low)
Qn	Flip-flop outputs (n = 0 to 3)
TC	Terminal count output

FIGURE 1. Terminal connections.

$\overline{\text{MR}}$	$\overline{\text{PE}}$	CET	CEP	Function
L	X	X	X	Reset (Qn = L, TC = L) (See note 1)
H	L	X	X	Load (Qn = Pn) (See notes 2 and 3)
H	H	H	H	Count (See notes 2, 3, and 4)
H	H	L	X	No change (See notes 2, 3, and 5)
H	H	X	L	No change (See notes 2, 3, and 5)

H = High voltage level
L = Low voltage level
X = Irrelevant

NOTES:

1. The reset operation occurs regardless of the input conditions of the other control inputs and timing input.
2. Action occurs on the rising edge of the clock (CP) input when the appropriate setup, hold, and pulse width timing requirements have been met in table I herein.
3. TC = H, whenever the conditions satisfy the logic equation, TC = Q0 ● Q1 ● Q2 ● Q3 ● CET are valid. For any other conditions, TC = L. The TC output will react to the CET input independent of the clock input. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers, or counters.
4. For the counting sequence, see the state diagram on figure 4.
5. Outputs maintain their current output state. For TC, the conditions in note 3 apply.

FIGURE 2. Truth table.

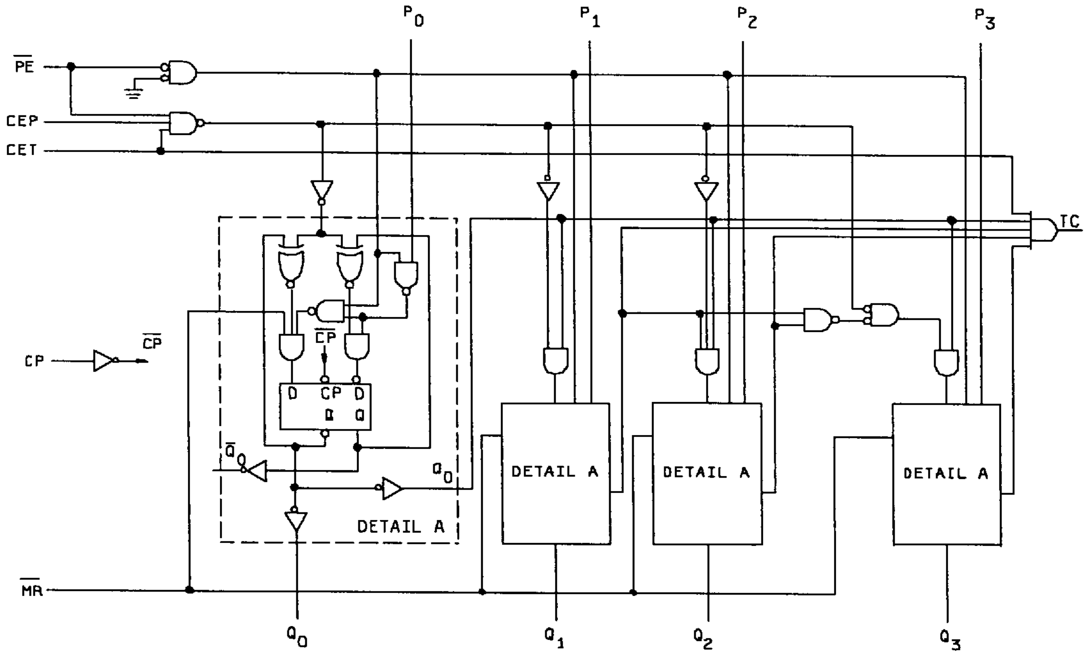

FIGURE 3. Logic diagram.

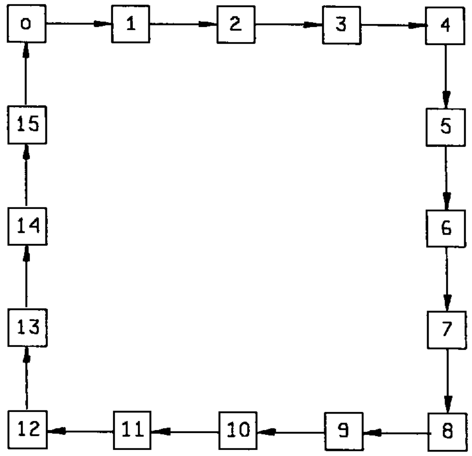

FIGURE 4. State diagram.

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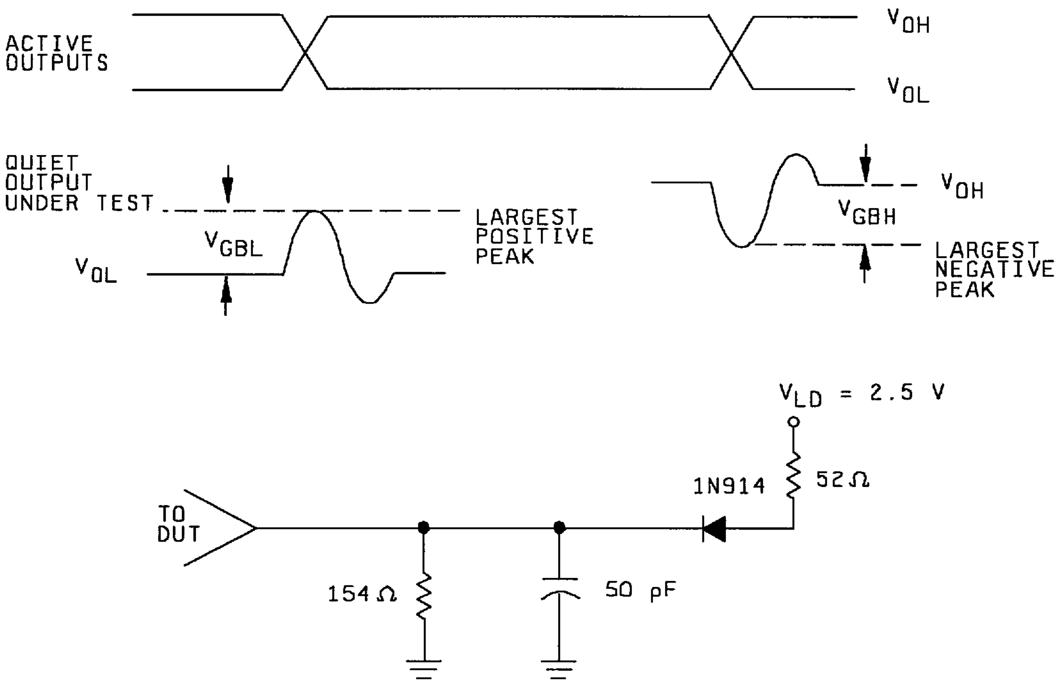

NOTE: Resistor and capacitor tolerances = ±10%.

FIGURE 5. Ground bounce waveforms and test circuit.

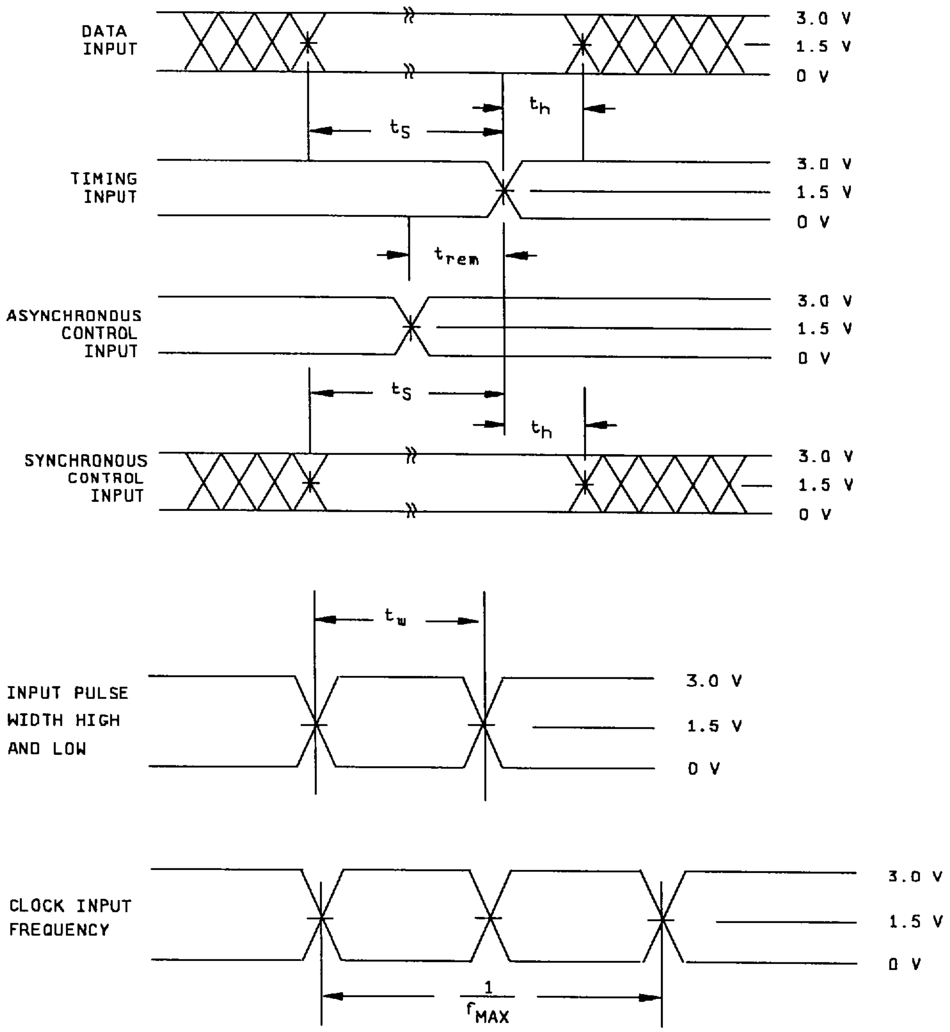

FIGURE 6. Switching waveforms and test circuit.

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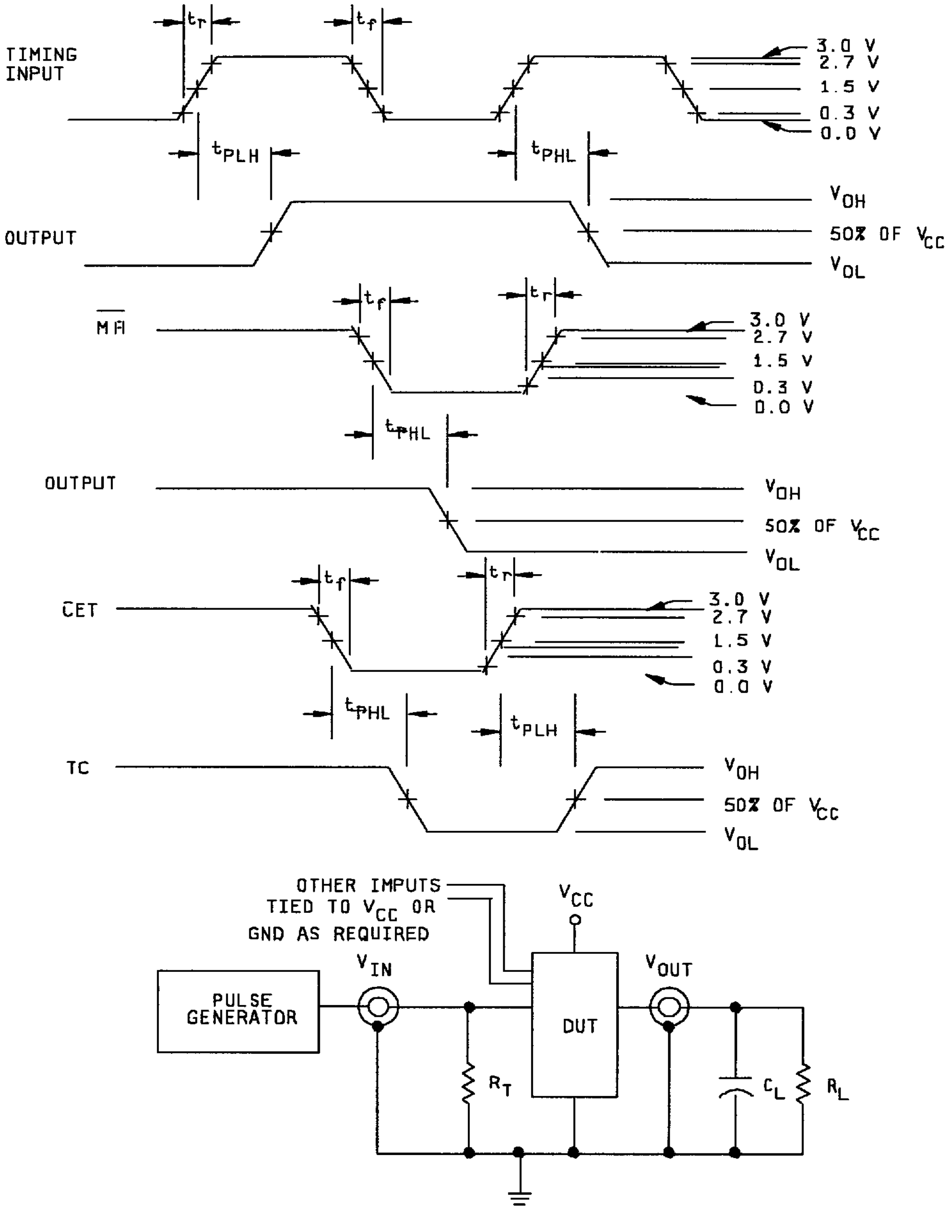

NOTES:
1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_T = 50Ω or equivalent, R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0V; PRR ≤ 10 MHz; $t_r \leq 3.0$ ns; $t_f \leq 3.0$ ns; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit - Continued.

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Latch-up and ground bounce tests are required for device classes Q and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground-bounce tests, test all applicable pins on five devices with zero failures.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A = +125°C$, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

d. RHA tests for device class M for levels M, D, L, R, F, G, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

e. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

f. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25°C \pm 5°C$, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, and as specified herein:

Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

1. Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.
2. Inputs tested low, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on class M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end point electrical parameter limits shall be as specified in table I herein and shall be the preirradiation end point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor- prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-04-20

Approved sources of supply for SMD 5962-91722 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9172201MEA	27014	54ACT161DMQB
5962-9172201MFA	27014	54ACT161FMQB
5962-9172201M2A	27014	54ACT161LMQB
5962R9172201MEA	27014	54ACT161DMQB-RH
5962R9172201MFA	27014	54ACT161FMQB-RH
5962R9172201M2A	27014	54ACT161LMQB-RH
5962R9172201VEA	27014	54ACT161JRQMLV
5962R9172201VFA	27014	54ACT161WRQMLV
5962R9172201V2A	27014	54ACT161ERQMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Point of contact: 5 Foden Road South Portland, ME 04106-1706

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.