GENERAL DESCRIPTION

The CL1208H is a CMOS 10-bit A/D converter for video applications. It is a three-step pipelined A/D converter which consists of sample & hold, three multiplying DACs, a 4-bit flash adc and three 3-bit flash adcs.
The maximum conversion rate of CL1208H is 10MSPS and supply voltage is 5V single.

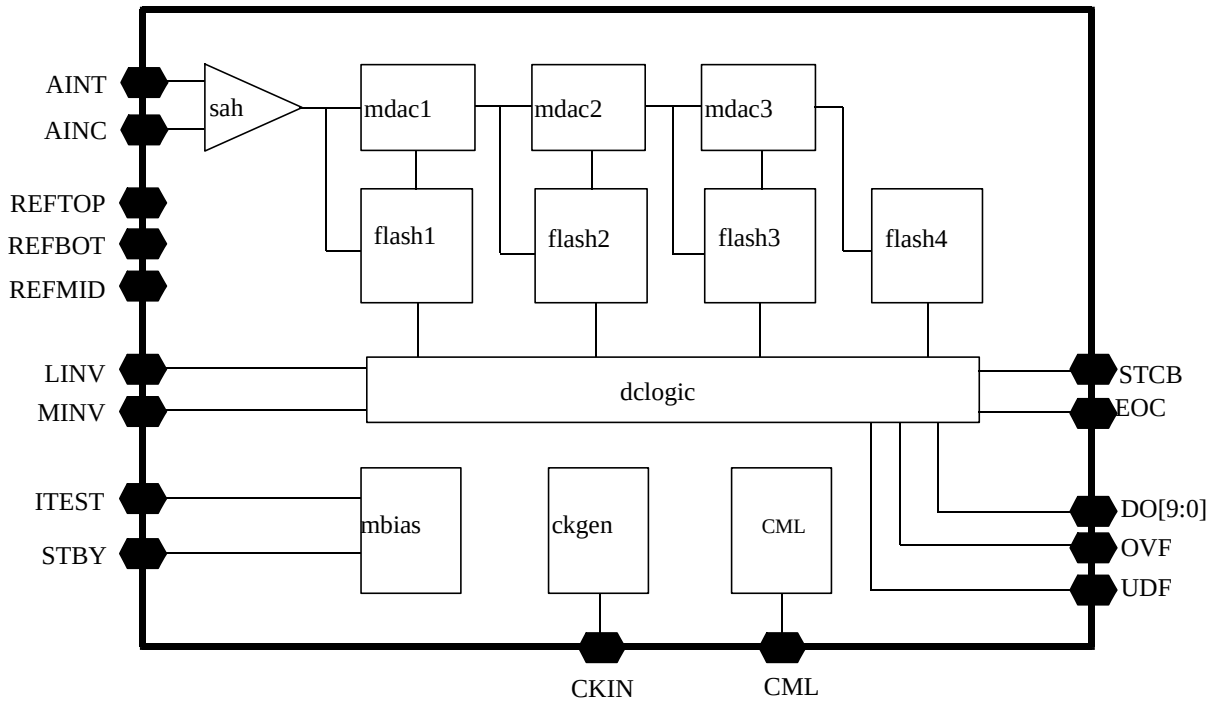
FEATURES

- **Resolution : 10Bit**
- **Differential Linearity Error : ±1.0 LSB**
- **Integral Linearity Error : ±1.0 LSB**
- **Maximum Conversion Rate : 10MSPS**
- **Sample & Hold Function Implemented**
- **Low Power Consumption : 125mW**
- **Power Supply : 5V Single**
- **Operation Temperature Range : 0º C ~70º C**

TYPICAL APPLICATIONS

- PC or computer based video signal processing such as multi-media, scanner, etc.
- General Purpose video applications including camcorder, digital video, broad-casting and studio equipments.
- Medical electronics such as digital scope, transit recorder, radar.

FUNCTIONAL BLOCK DIAGRAM



CORE PIN DESCRIPTION

NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
AINT	AI	piar50_bb	Analog Input + (Vp-p : 5Vp-p)
AINC	AI	piar50_bb	Analog Input : (DC=2.5V)
REFMID	AO	pia_bb	Reference Mid Point (Test Pin)
REFTOP	AI	pia_bb	Reference Top (3.75V)
REFBOT	AI	pia_bb	Reference Bottom(1.25V)
MINV	DI	picc_bb	high=invert MSB(normally gnd)
LINV	DI	picc_bb	high=invert all LSB(normally gnd)
VDDA	AP	vdda	Analog Power (5V)
VSSA	AG	vssa	Analog Ground
ITEST	BD	pia_bb	open=use internal bias point
STBY	DI	picc_bb	high=power saving standby mode
CKIN	DI	picc_bb	Sampling Clock Input
CML	AO	pia_bb	Internal Bias Point(Test Pin)
DO[9:0]	DO	pot2_bb	Digital Output
OVF	DO	pot2_bb	Over Fkow
UDF	DO	pot2_bb	Under Flow
STCB	DI	picc_bb	Start of Conversion(normally high)
EOC	DO	pot2_bb	End of Conversion
VBB	AB	vbba	Sub Bias
VSSD	DG	vssd	Digital Ground
VDDD	DP	vddd	Digital Power

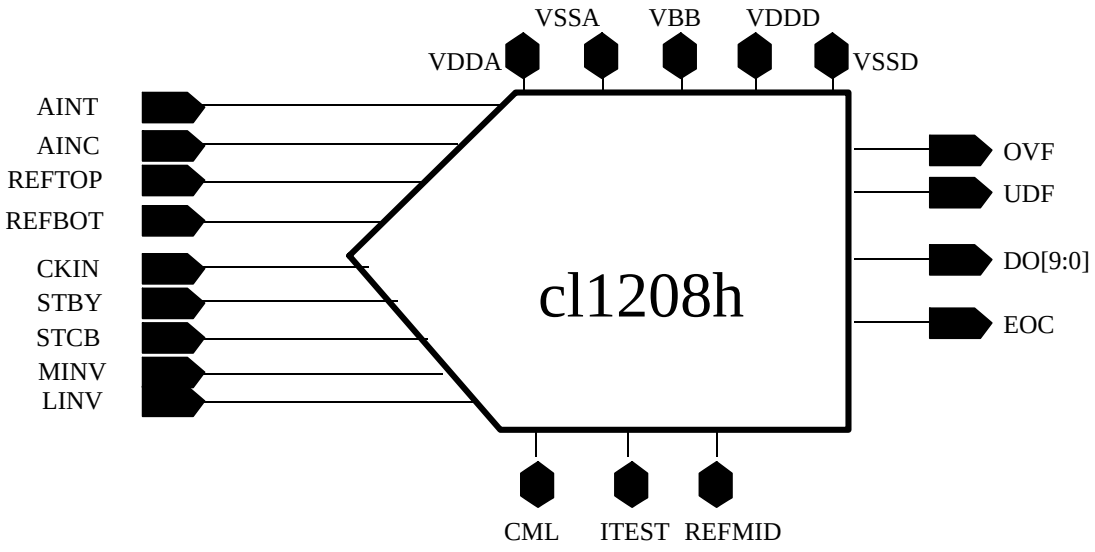
I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- AG : Analog Ground
- AB : Analog Sub Bias
- DP : Digital Power
- DG : Digital Ground
- DB : Digital Sub Vias

- BD : Bidirectional Port

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	7.0	V
Analog Input Voltage	AIN	VSS to VDD	V
Digital Input Voltage	CLK	VSS to VDD	V
Digital Output Voltage	V_{OH}, V_{OL}	VSS to VDD	V
Reference Voltage	REFTOP/REFBOT	3.75 / 1.25	V
Storage Temperature Range	Tstg	-45 to 125	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5KΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA - VSSA VDDD - VSSD	4.75	5.0	5.25	V
Supply Voltage Difference	VDDA - VDDD	-0.1	0.0	0.1	V
Reference Input Voltage(Internally)	REFTOP REFBOT	- -	3.75 1.25	- -	V
Analog Input Voltage	AINT	0	-	5	V
Digital Input 'L' Voltage Digital Input 'H' Voltage	V_{IL} V_{IH}	- 4.5	- -	0.5 -	V
Operating Temperature	Topr	0	-	70	°C

NOTES

1. It is strongly recommended that all the supply pins (VDDA, VDDD) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

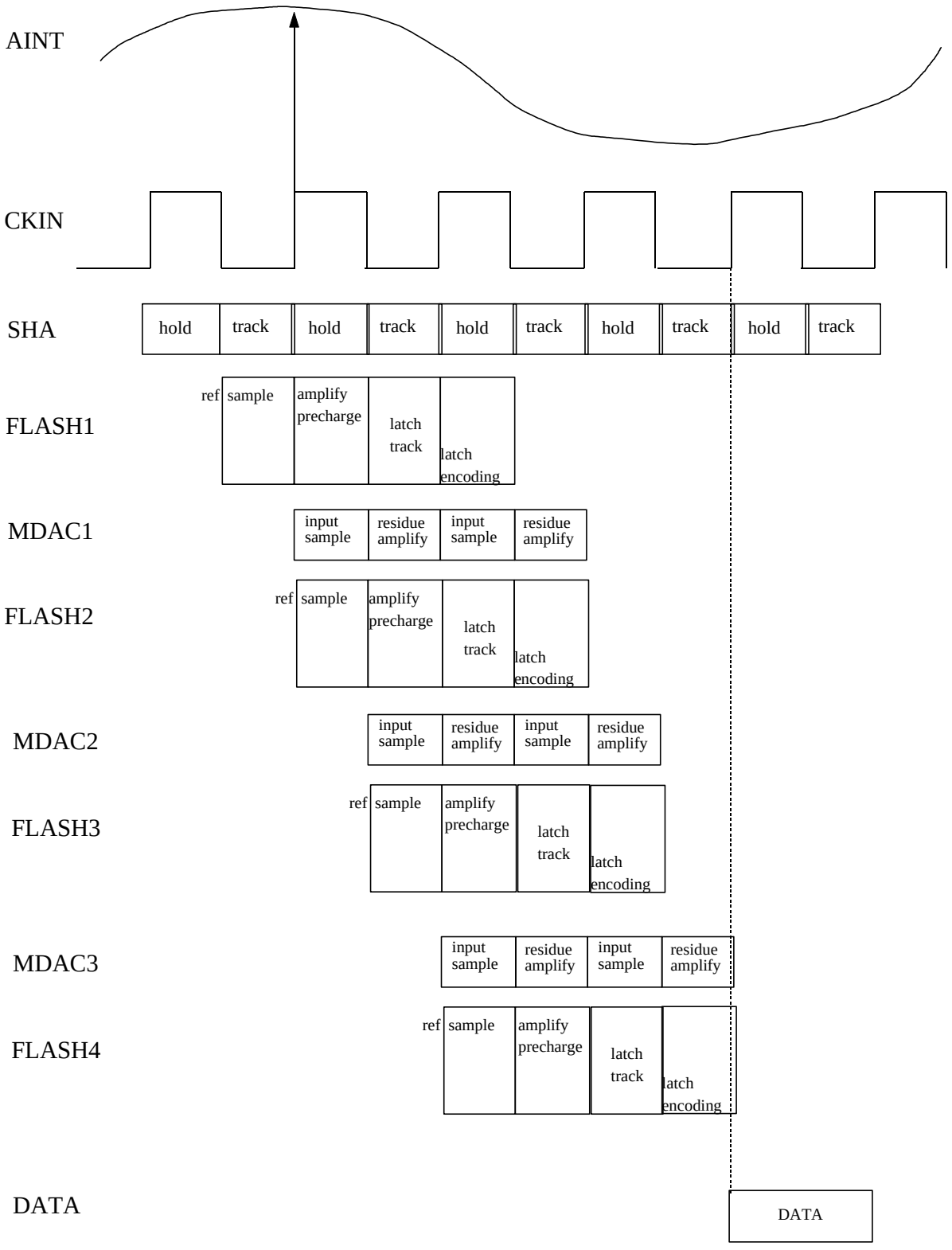
Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Reference Current	IREF	1.5	2	3	mA	
Differential Linearity Error	DLE	-	-	±1.0	LSB	AINT : 0 ~ 5.0V (Ramp Input)
Integral Linearity Error	ILE	-	-	±1.0	LSB	Fck : 1MHz
Bottom Offset Voltage Error	EOB	-	-	20	LSB	
Top Offset Voltage Error	EOT	-	-	20	LSB	

NOTES
1. Converter Specifications (unless otherwise specified)
   VDDA=5.0V VDDD=5.0V
   VSSA=GND VSSD=GND
   Ta=25º C
2. TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Maximum Conversion Rate	fc	10	-	-	MSPS	AINT : 1MHz Sine Signal (source resolution > 12bit)
Dynamic Supply Current	Ivdd	-	25	30	mA	fc=10MHz (without system load)
Signal - to - Noise, Distortion Ratio	SNDR	50	54	-	dB	AINT = 1MHz fc = 10MHz

TIMING DIAGRAM(Main Function)



FUNCTIONAL DESCRIPTION

1. CL1208H is a four step A/D Converter comprising a 4-bit flash ADC, three 3-bit flash ADC and three multiplying DAC. The N-bit flash ADC is composed of $2^{(n-1)}$ latching comparators, and multiplying DAC is composed of 2*(N+2) capacitors and two fully-differential amplifier.

2. CL1208H operates as follows. During the first "L" cycle of external clock the analog input data is tracked and sampled, and the input is held from the rising edge of the external clock, which is fed to the first 4-bit flash ADC, and the first multiplying DAC. Multiplying DAC reconstructs a voltage corresponding to the first 4-bit ADC's output, and finally amplifies a residue voltage by 2^3. The second 3-bit flash ADC, and MDAC are worked as same manner, finally amplifiers a residue voltage, which is the difference between first MDAC's output and reconstructed voltage by 2^2. The third 3-bit flash ADC, and MDAC are worked as previous stages. Finally amplified residue voltage at the third multiplying DAC is fed to the last 3-bit flash ADC decides final 3-bit digital digital code.

3. CL1208H has the error correction scheme, which handles the output from mismatch in the first, second, third and fourth flash ADC.

MAIN BLOCK DESCRIPTION

1. SAH

SAH(track and hold) is the circuit that samples the analog input signal and hold that value until next sample-time. It is good as small as its different value between analog input signal and output signal. SAH amp gain must be higher than 66dB at least for less than 1/2LSB of SAH error voltage at 10bit ADC and its conversion frequency is 20MHz, its settling-time must be shorten than 18ns. This SAH is consist of fully differential op amp, switching tr. and sampling capacitor. The sampling clock are non-overlapping clocks(Q1,Q2) and sampling capacitor value is 1.2pF. SAH uses independent bias to protect interruption of any other circuit. SAH amp is designed that open-loop dc gain is higher than 70dB, phase margin is higher than 60degree. Its input block is designed to be the rail-to-rail architecture using complementary different pair.

2. FLASH

The 4-bit flash converter compare analog signal (SAH output) with reference voltage, and that result transfer to MDAC and digital correction logic block. It is realized fully differential comparators of 15EA. Considering self-offset, dynamic feed through error, it should distinguish 40mV at least. First, the comparators charge the reference voltage at the sampling capacitors before transferred SAH output. Q2 works this process and Q1 discharges this sampling capacitance. That is, the comparators compare relative different values dual input voltage with dual reference voltage. Its output during Q1 operation is stored at the pre-latch block by Q1P.

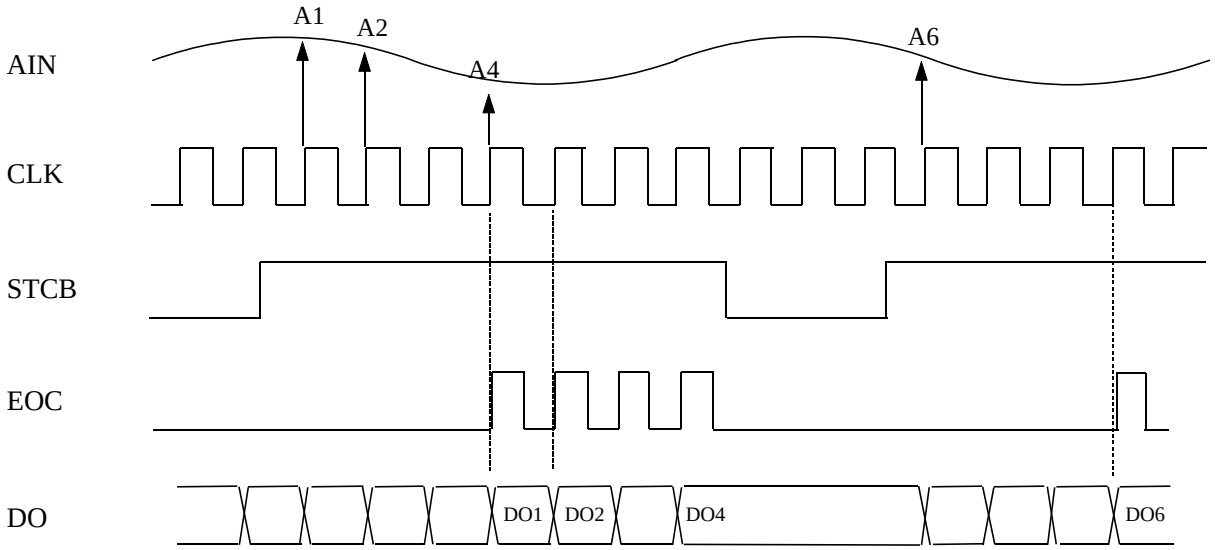
3. MDAC

MDAC is the most important block at this ADC and it decides the characteristics. MDAC is consist of amp1,amp2, selection logic and capacitor array(c_array). C_array's compositions are the capacitors to charge the analog input and and the reference voltage, Switches to control the path. Selection logic controls the c_array internal switches. If Q1 is high, selection's output are all low, the switches of tsw1 are off, the switches of tsw2 are all on. Therefore the capacitors of c_array charge analog input values holded at SAH. If Q2 is high, it is reversed and final MDAC output voltage is described the following equation.

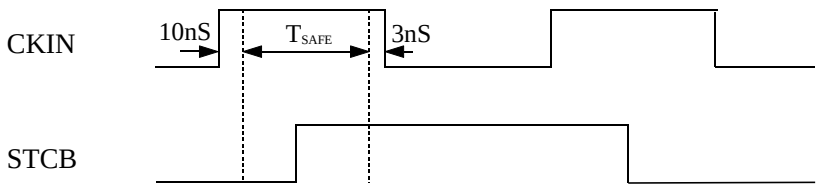
Vout = (AIN - Vref)*8-Vref/2
AIN=AINT-2.5V

TIMING DIAGRAM (OPTIONAL)

1. Main Waveform



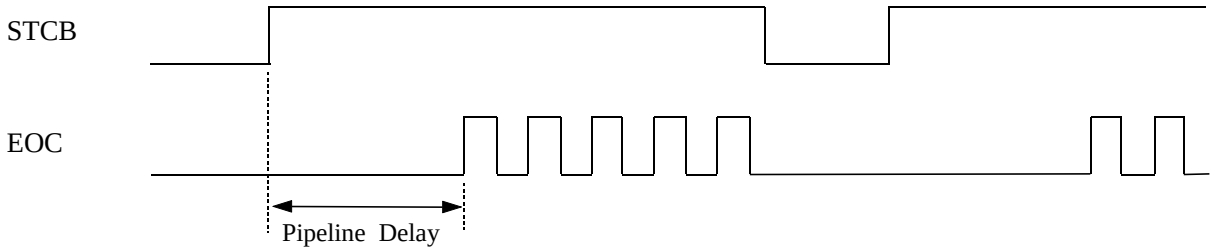
2. STCB / CKIN



The A/D converter does data conversion when STCB(Start of Conversion Bar) signal is just "HIGH". Otherwise, output data (DO[9:0]) keeps the current states.

The STCB signal should be changed during "Tsafe" with the "HIGH" level of the clock to operation as shown in the main waveform.

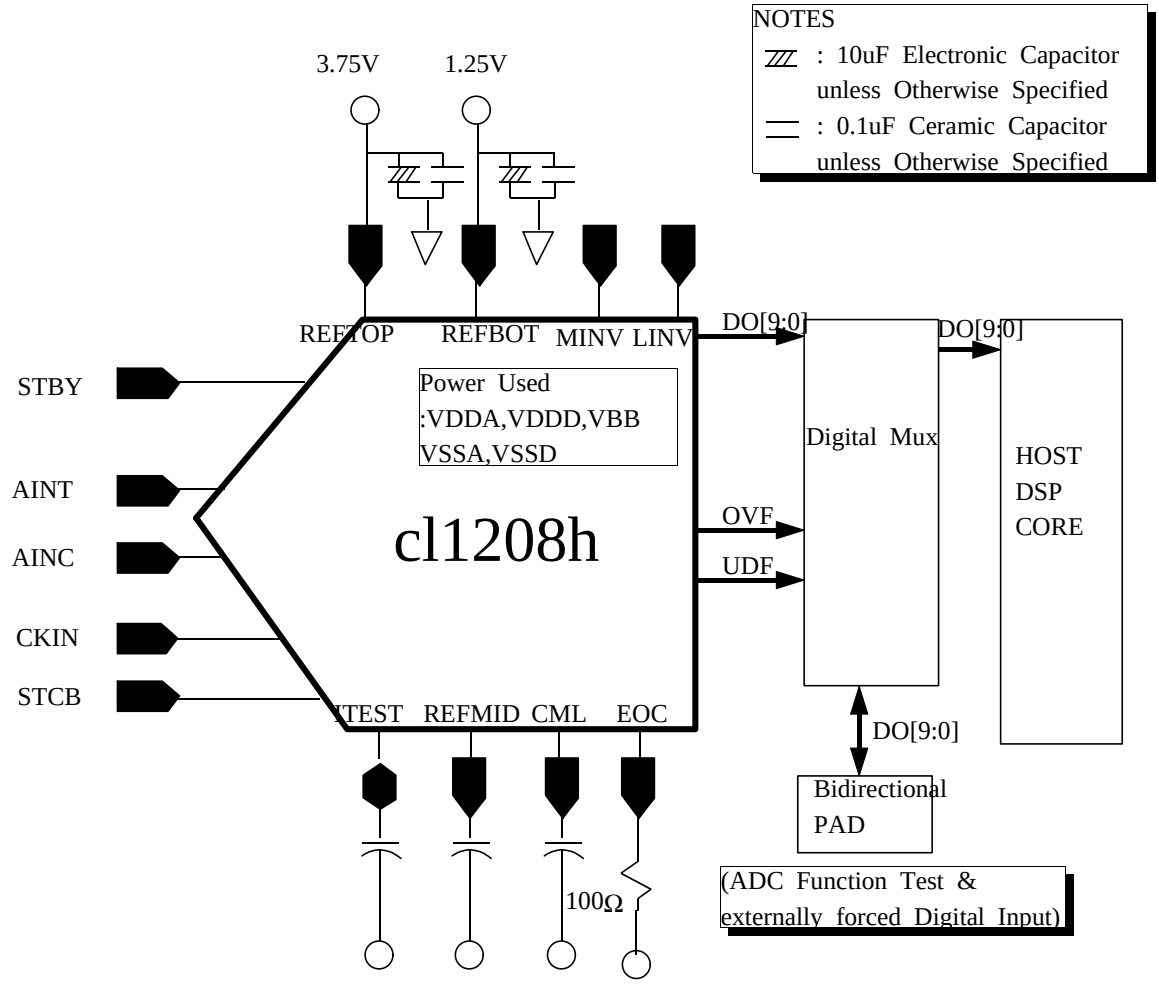
3. Pipeline Delay



After STCB goes "HIGH", the A/D converter requires the pipeline delay of 3 clock period to generate EOC signal and data outputs.

CORE EVALUATION GUIDE

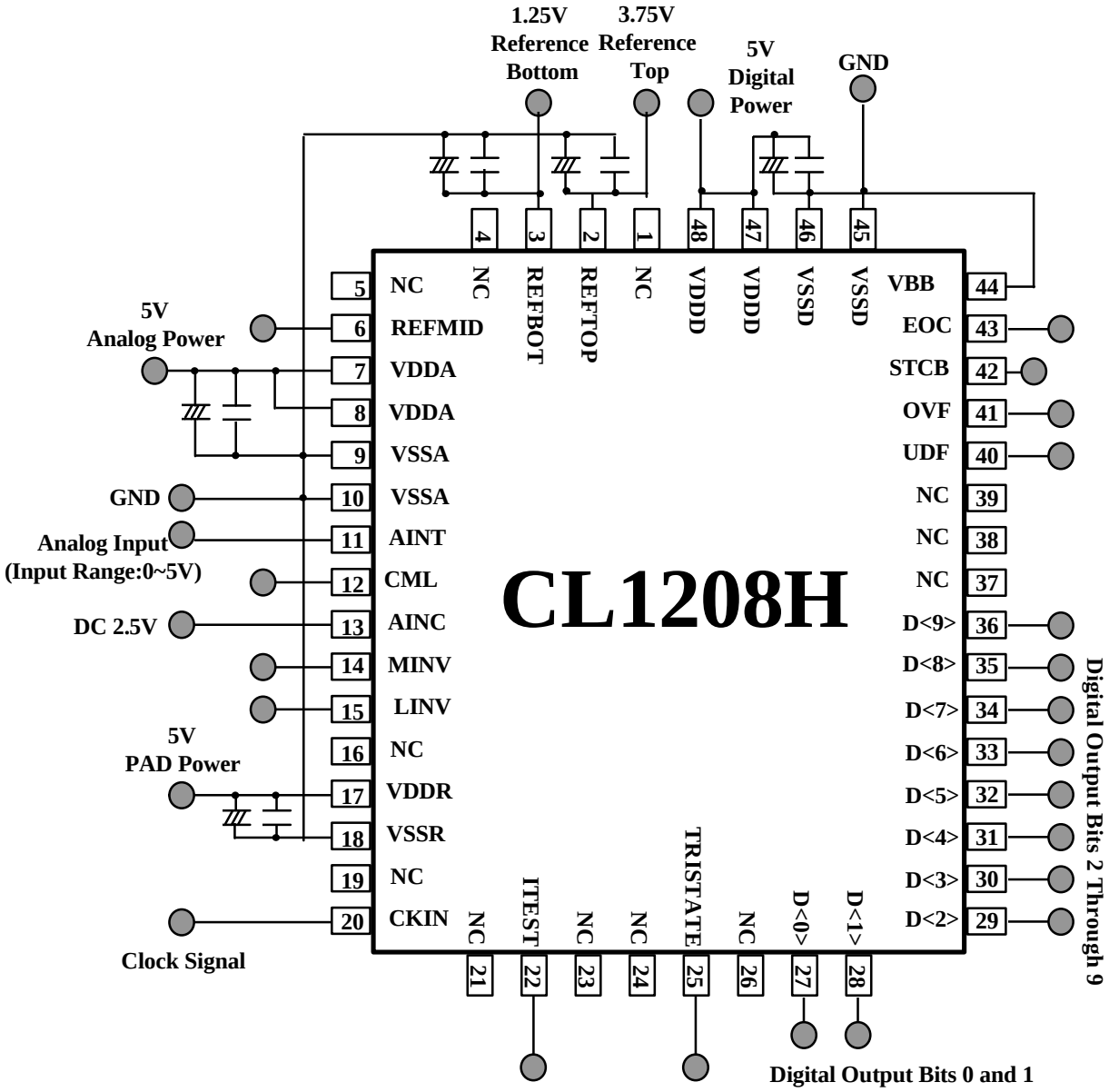
1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased internally through resistor devider.



PACKAGE CONFIGURATION

NOTES

1. You can test ADC function by checking external bidirectional pad connected to internal signal path.
2. ESD (ElectroStatic Discharge) sensitive device. Although the digital control inputs are diode protected, permanent damage may occur on devices subjected to high electrostatic discharges. It is recommended that unused devices be stored in conductive foam or shunts to avoid performance degradation or loss of functionality. The protective foam should be discharged to the destination socket before devices are inserted.
3. NC denotes "No Connection".



PACKAGE PIN DESCRIPTION

NAME	PIN NO.	I/O TYPE	PIN DESCRIPTION
REFTOP	2	AI	External Reference Top Bias.(3.75V)
REFBOT	3	AI	External Reference Bottom Bias.(1.25V)
REFMID	6	AO	Reference Mid Point (Test Pin)
VDDA	7,8	AP	5V Analog Power
VSSA	9,10	AG	Analog Grounf
AINT	11	AI	Analog Input (+) Input Range : 0~5V
CML	12	AO	Internal Bias Point (Test Pin)
AINC	13	AI	Analog Input. (-) DC 2.5V
MINV	14	DI	high = invert MSB(normally gnd)
LINV	15	DI	high = invert all LSB(normally gnd)
VDDR	17	PP	Ouput Driver Power
VSSR	18	PG	Output Driver Ground
STBY	19	DI	High = power saving standby mode (normally gnd)
CKIN	20	DI	Sampling Clock Input
ITEST	22	BD	open=use internal bias point
TRISTATE	25	DI	high = high impedance digital output (normally gnd)
D[9:0]	27~36	DO	Digital Output
UDF	40	DO	Underflow Output Signal
OVF	41	DO	Overflow Output Signal
STCB	42	DI	Start of Conversion (normally high)
EOC	43	DO	End of Conversion
VBB	44	DB	Substrate Ground
VSSD	45,46	DG	Digital Ground
VDDD	47,48	DP	Digital Power

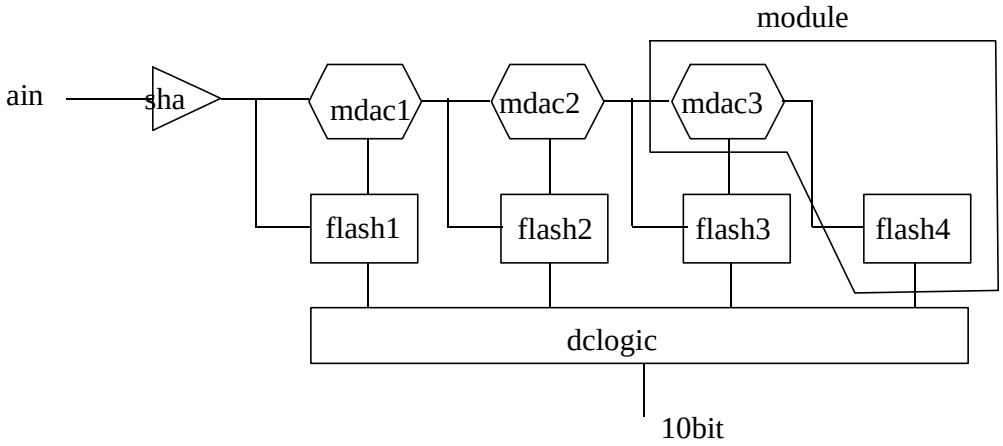
NOTES

1. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.

USER GUIDE

1. Resolution Control.

- Modular structure is the most important feature of CL1208H.
- You can get any resolution you want by combining each primary module (MDAC + FLASH) without major circuit change.
- It means you don't have to redesign the most difficult analog block for another resolution.
- But this simple resolution control method has a limit up to 10bits, otherwise the internal op-amp must be redesigned.



2. Speed Up

- The initial target speed of CL1208H was 10MHz, but it proved to operate well at 15MHz or more due to a lot of design margin.

3. Input Range Variation.

- The default of the input of this ADC is differential -2.5V ~ +2.5V.
- The bias voltage of both AINT and AINC is 1.25V~3.75V, and their offset is 2.5V.
- In order to alter to another input voltage range, change the voltage values of AINT and AINC after setting Reftop and Refbot to the maximum value of input range.
- If you want single ended input, fix AINC to 2.5V as a ground and the internal input voltage level is V(aint)-2.5V.

4. Verilog Modeling

- Verilog modeling needs 64bits for only one analog real signal.

FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic cheking table and fill out the additional questions.
We appreciate your interest in our products. Thank you very much.

Characteristic	Min	Typ	Max	Unit	Remarks
Analog Power Supply Voltage				V	
Digital Power Supply Voltage				V	
Bit Resolution				Bit	
Reference Input Voltage				V	
Analog Input Voltage				Vpp	
Operating Temperature				ºC	
Integral Non-linearity Error				LSB	
Differential Non-linearity Error				LSB	
Bottom Offset Voltage Error				mV	
Top Offset Voltage Error				mV	
Maximum Conversion Rate				MSPS	
Dynamic Supply Current				mA	
Power Dissipation				mW	
Signal-to-noise Ratio				dB	
Pipeline Delay				CLK	
Digital Output Format (Provide detailed description & timing diagram)					

1. Between single input-output and differential input-output configurations, which one is suitable for your system and why?

2. Please comment on the internal/external pin configurations you want our ADC to have, if you have any reason to prefer some type of configuration.

3. Freely list those functions you want to be implemented in our ADC, if you have any.