MP8042

High Current, Dual Channel Power Half-Bridge

The Future of Analog IC Technology™

INITIAL RELEASE – SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP8042 is a dual channel power half-bridge that can be configured as the output stage of a Class-D audio amplifier. Each channel can be driven independently as stereo single ended audio amplifiers, or driven complementary in a bridge tied load (BTL) audio amplifier configuration.

The MP8042 features a low current shutdown mode, standby mode, input under voltage protection, thermal shutdown and fault flag signal output. Both channels of the driver interface with standard logic signals. The MP8042 is available in a 20-pin TSSOP (with Exposed Pad) package.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV8042DF-00B	3.5"X x 4.0"Y x 1.0"Z

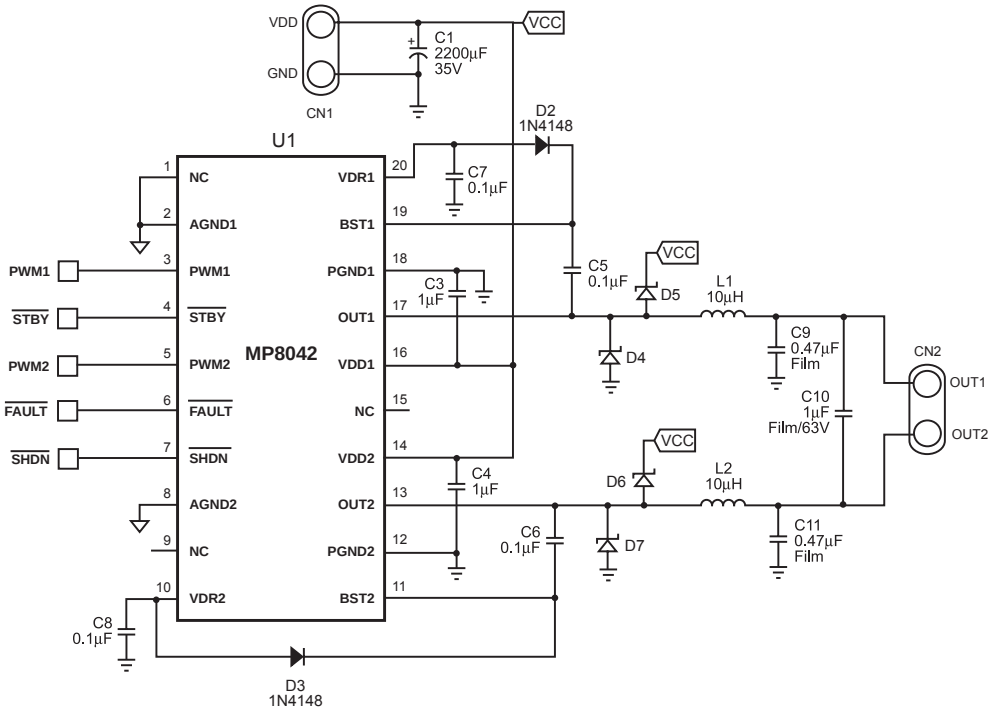
FEATURES

- ±5A Peak Current Output
- Up to 600KHz Switching Frequency
- Protected Integrated Power 150mΩ Switches
- 30ns Switch Dead Time
- All Switches Current Limited
- Internal Under Voltage Protection
- Internal Thermal Protection
- 2.1mA Operating Current
- Fault Output Flag
- Stereo Single Ended: 20W/Channel, 4Ω Load
- Bridge Tied Load Output Power: 40W, 8Ω Load

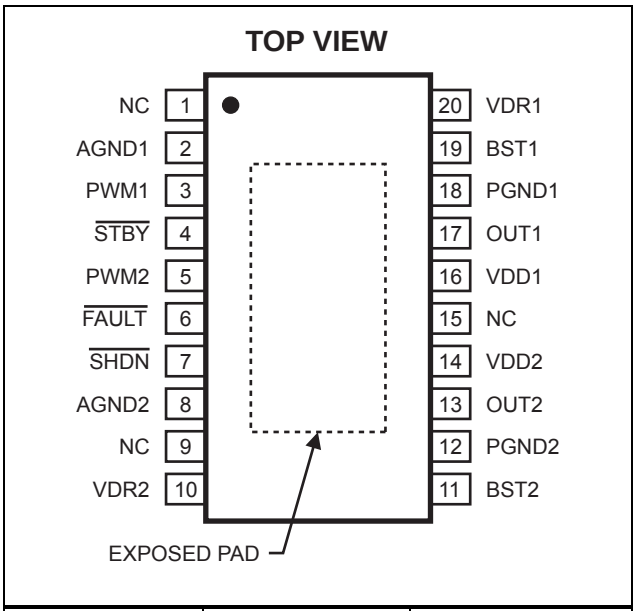
APPLICATIONS

- Class D Audio Drivers
- Full or Half-Bridge DC-DC Switching Regulators
- Motor Drivers

TYPICAL APPLICATION



PACKAGE REFERENCE



Part Number*	Package	Temperature
MP8042DF	TSSOP20F	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP8042DF–Z)
For RoHS Compliant Packaging, add suffix –LF (eg. MP8042DF–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

VDD1/2 Supply Voltage 26V
OUT1/2 Pin Voltage..... –0.3V to V_{DD} + 0.3V
OUT1/2 to BST1/2 ..... –0.3V to +6V
Voltage at All Other Pins ..... –0.3V to +6V
Storage Temperature .....–55°C to +150°C

Recommended Operating Conditions (2)

VDD1/2 Supply Voltage..... 7.5V to 24V
Peak Output Current..... 6A Maximum
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
TSSOP20F	40	6....	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{DD1} = V_{DD2} = 12V, $V_{\overline{SHDN}}$ = 5V, T_A = +25°C, unless otherwise specified.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VDD Operating Current		I_{LOAD} = 0A		2.1	2.5	mA
VDD Shutdown Current		V_{SHDN} = 0V		4.0	10	µA
VDD Operating Threshold, Low			5.8	6.1		V
VDD Operating Threshold, High				6.63	7.2	V
$\overline{STBY}$ Threshold, Low			1.0	1.2		V
$\overline{STBY}$ Threshold, High				1.85	2.0	V
$\overline{SHDN}$ Threshold, Low			1.0	1.2		V
$\overline{SHDN}$ Threshold, High				1.9	2.0	V
$PWM_{1,2}$ Threshold, Low			1.5	1.69		V
$PWM_{1,2}$ Threshold, High				1.83	2.0	V
PWM Input Bias Current				1		µA
OUT On Resistance (4)		V_{DD} = 7.5V, High-Side and Low-Side		0.15		Ω
OUT Current Limit (4)		V_{PWM} = 5, Sinking		5		A
		V_{PWM} = 0, Sourcing		5		A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 12V, $V_{\overline{SHDN}}$ = 5V, T_A = +25°C, unless otherwise specified.

Parameters	Symbol	Condition	Min	Typ	Max	Units
OUT Switching Frequency		V_{PWM} = 0 to 2V, 50% Duty Cycle			0.6	MHz
OUT Maximum Duty Cycle (5)		V_{DD} = 7.5V, V_{PWM} = 2V, C_{BST} = 100nF, f_{SW} = 3.3KHz		99.5		%
OUT Rise/Fall Time (4)		V_{PWM} = 0V to 5V		10		ns
PWM Pulse Width		V_{PWM} = 0V to 2V, High or Low Pulse		200		ns
Dead Time (4)		I_{OUT}= ±100mA		30		ns
PWM to OUT Delay Time Rising		V_{PWM} = 0V to 5V		37	45	ns
PWM to OUT Delay Time Falling		V_{PWM} = 5 to 0V		54	65	ns
Thermal Shutdown Temperature (4)		T_J Rising, Hysteresis = 20°C		150		°C

Notes:

4) Guaranteed by design, not production tested.

5) OUT drives low for 1.5µs every 300µs to charge the BST to SW capacitor.

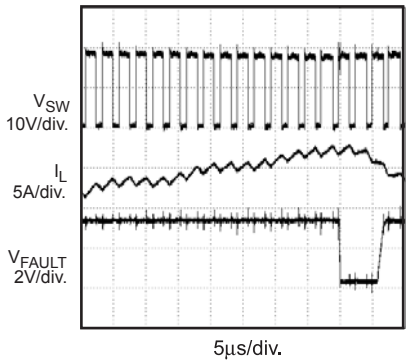
PIN FUNCTIONS

Pin #	Name	Description
1	NC	No Connect.
2	AGND1	Analog Ground 1.
3	PWM1	Driver Logic Input 1. Drive PWM1 with the signal that controls the MP8042 OUT1. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch.
4	$\overline{\text{STBY}}$	Standby Input. Default low (internal pull-down). If driven high, the output of drivers is determined by the PWM1/2. If driven low, the output of both drivers is high impedance.
5	PWM2	Driver Logic Input 2. Drive PWM2 with the signal that controls the MP8042 OUT2. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
6	$\overline{\text{FAULT}}$	Fault Output. A low output at $\overline{\text{FAULT}}$ indicates that the MP8042 has detected an over temperature, over current condition or the voltage to the driver is less than 5V. This output is open drain.
7	$\overline{\text{SHDN}}$	Shutdown Input. When low, both channels will be shut off.
8	AGND2	Analog Ground 2.
9	NC	No Connect.
10	VDR2	Gate Drive Supply Bypass 2. The voltage at VDR2 is supplied from an internal regulator from VDD2. VDR2 powers the internal circuitry and internal MOSFET gate drive for the OUT2 stage. Bypass VDR2 to AGND2 with a 0.1μF to 10μF capacitor.
11	BST2	Bootstrap Supply 2. BST2 powers the high-side gate of the OUT2 stage. Connect a 0.1μF or greater capacitor between BST2 and OUT2.
12	PGND2	Power Ground 2. Connect the exposed pad on bottom side to the ground plane.
13	OUT2	Switched Output 2. Connect the output LC filter to OUT2. OUT2 is valid approximately 100μs after VDD2 goes high.
14	VDD2	Power Supply Input 2. Connect VDD2 to the positive side of the input power supply. Bypass VDD2 to AGND2 as close to the IC as possible.
15	NC	No Connect.
16	VDD1	Power Supply Input 1. Connect VDD1 to the positive side of the input power supply. Bypass VDD1 to GND1 as close to the IC as possible.
17	OUT1	Switched Output 1. Connect the output LC filter to OUT1. OUT1 is valid approximately 100μs after VDD1 goes high.
18	PGND1	Power Ground 1. Connect the exposed pad on bottom side to the ground plane.
19	BST1	Bootstrap Supply 1. BST1 powers the high-side gate of the OUT1 stage. Connect a 0.1μF or greater capacitor between BST1 and OUT1.
20	VDR1	Gate Drive Supply Bypass 1. The voltage at VDR1 is supplied from an internal regulator from VDD1. VDR1 powers the internal circuitry and internal MOSFET gate drive for the OUT1 stage. Bypass VDR1 to AGND1 with a 0.1μF to 10μF capacitor.

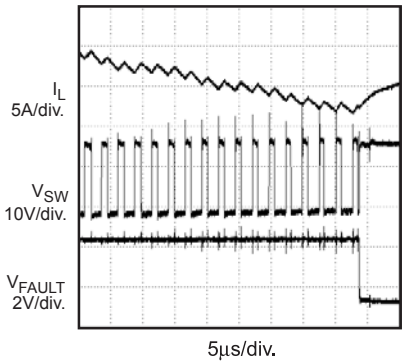
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD1} = V_{DD2} = 12V, $V_{\overline{SHDN}}$ = 5V, T_A = +25°C, unless otherwise specified.

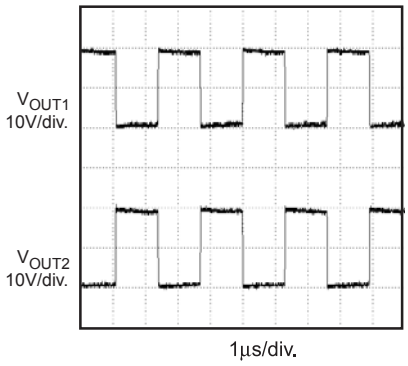
Short Circuit Positive Current



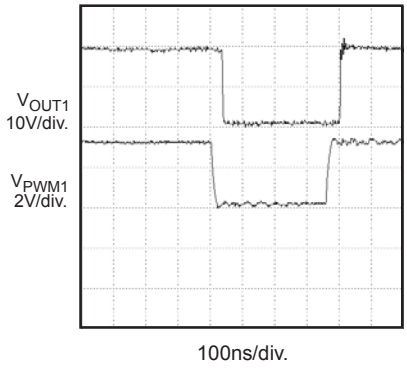
Short Circuit Negative Current



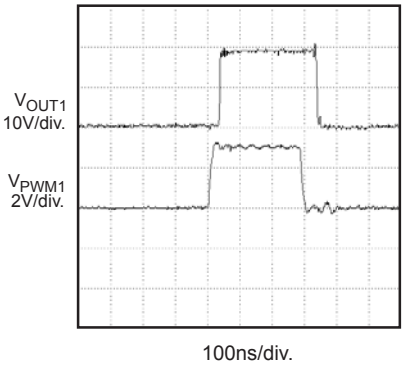
Normal Switch Waveform



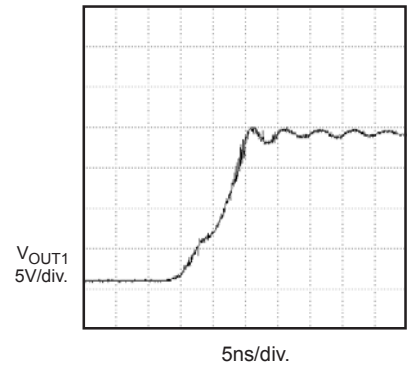
Input/Output Waveform Negative Pulse



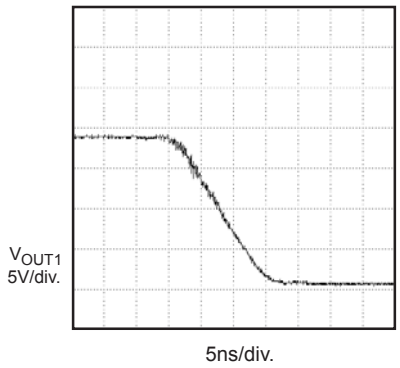
Input/Output Waveform Positive Pulse



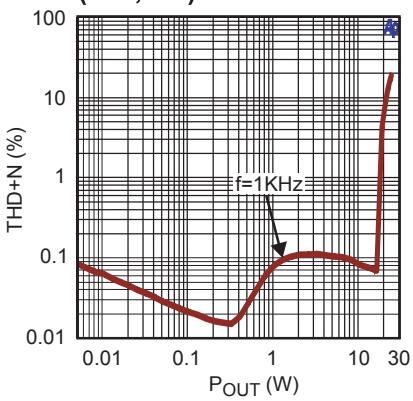
Output Rise-Time



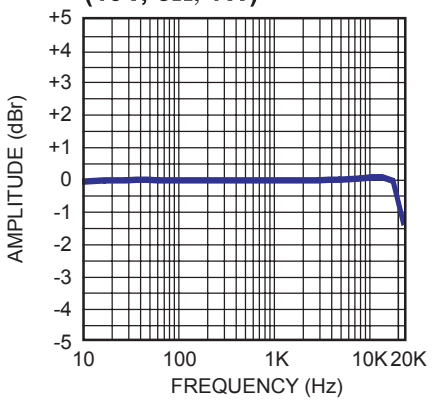
Output Fall-Time



THD+N vs. P_{OUT} (19V, 8Ω)



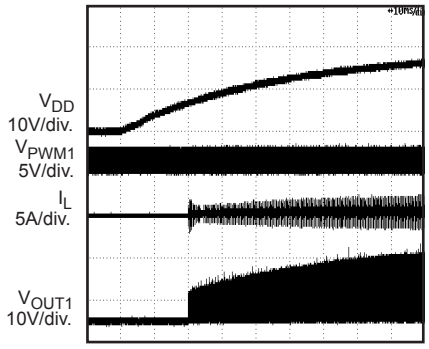
Frequency Response (19V, 8Ω, 1W)



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

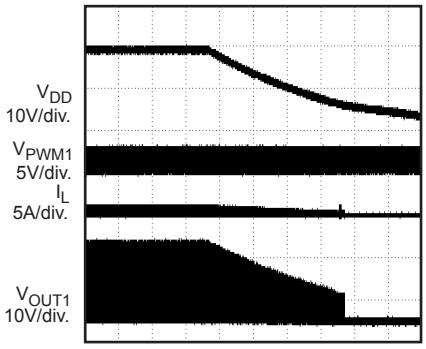
V_{DD1} = V_{DD2} = 12V, $V_{\overline{SHDN}}$ = 5V, T_A = +25°C, unless otherwise specified.

Start-up



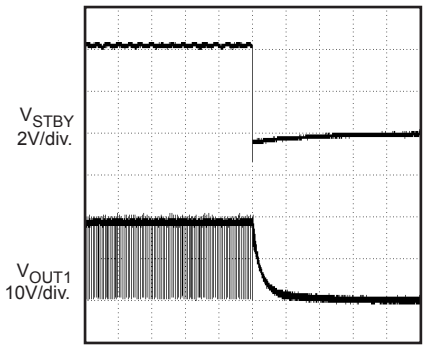
50ms/div.

Shut-down



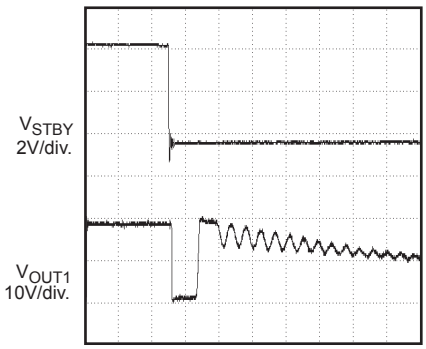
50ms/div.

Standby



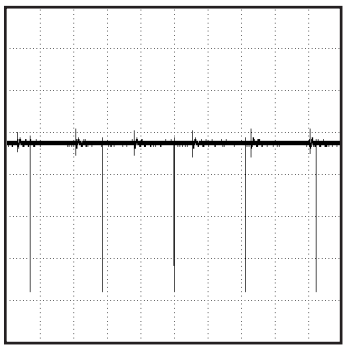
50µs/div.

Standby



50µs/div.

BS Recharge Cycling (V_{DD} = 19V, R_L = 16Ω)



200µs/div.

OPERATION

The MP8042 is a high voltage, dual channel power half- bridge that can be configured as the output of a Class D amplifier. The output is in phase with the input, and the dead time is optimized for symmetrical performance, regardless of load conditions.

The shutdown pin ($\overline{SHDN}$), when set low, causes both channels 1 and 2 to be shut off. When the standby pin ($\overline{STBY}$) is pulled low, it causes the outputs of both channels to go into high impedance. However, when the voltage across the BST1/2 and OUT1/2 pins drops sufficiently low, the bottom MOSFET is turned on to refresh the external bootstrap capacitor. For a bootstrap capacitor of 100nF, the refresh time is approximately 300µs.

In order to prevent erratic operation, two under voltage lockout (UVLO) circuits are used. One of them is to ensure that the supply for the bottom gate drive circuit is sufficiently high and the other is for the top gate driver.

Fault Protection

To protect the power MOSFETs, two layers of protection are provided. The first is the current limit, wherein if the current through either the top or the bottom MOSFET exceeds an internally preset value of 5A, that particular MOSFET is immediately shut down and the complementary MOSFET is turned on. If this fails to reset the current and there is an indication that the current is going to runaway, the current foldback will kick in. This ensures that the current is reset close to zero before resuming operation.

Thermal monitoring is also integrated into the MP8042. If the die temperature rises above 150°C, both switches are turned off. The temperature must fall below 140°C before normal operation resumes.

Fault Output

The MP8042 includes an open drain, active low fault indicator output ($\overline{FAULT}$). A fault will be indicated if one of the following conditions is detected: the current limit is tripped, the thermal shutdown is tripped, the UVLO for the bottom gate driver is tripped or the part is disabled.

A fault on any channel causes the $\overline{FAULT}$ pin to be pulled low. However, only that fault channel has its output set to high impedance.

Do not apply more than 6V to the $\overline{FAULT}$ pin.

BLOCK DIAGRAM

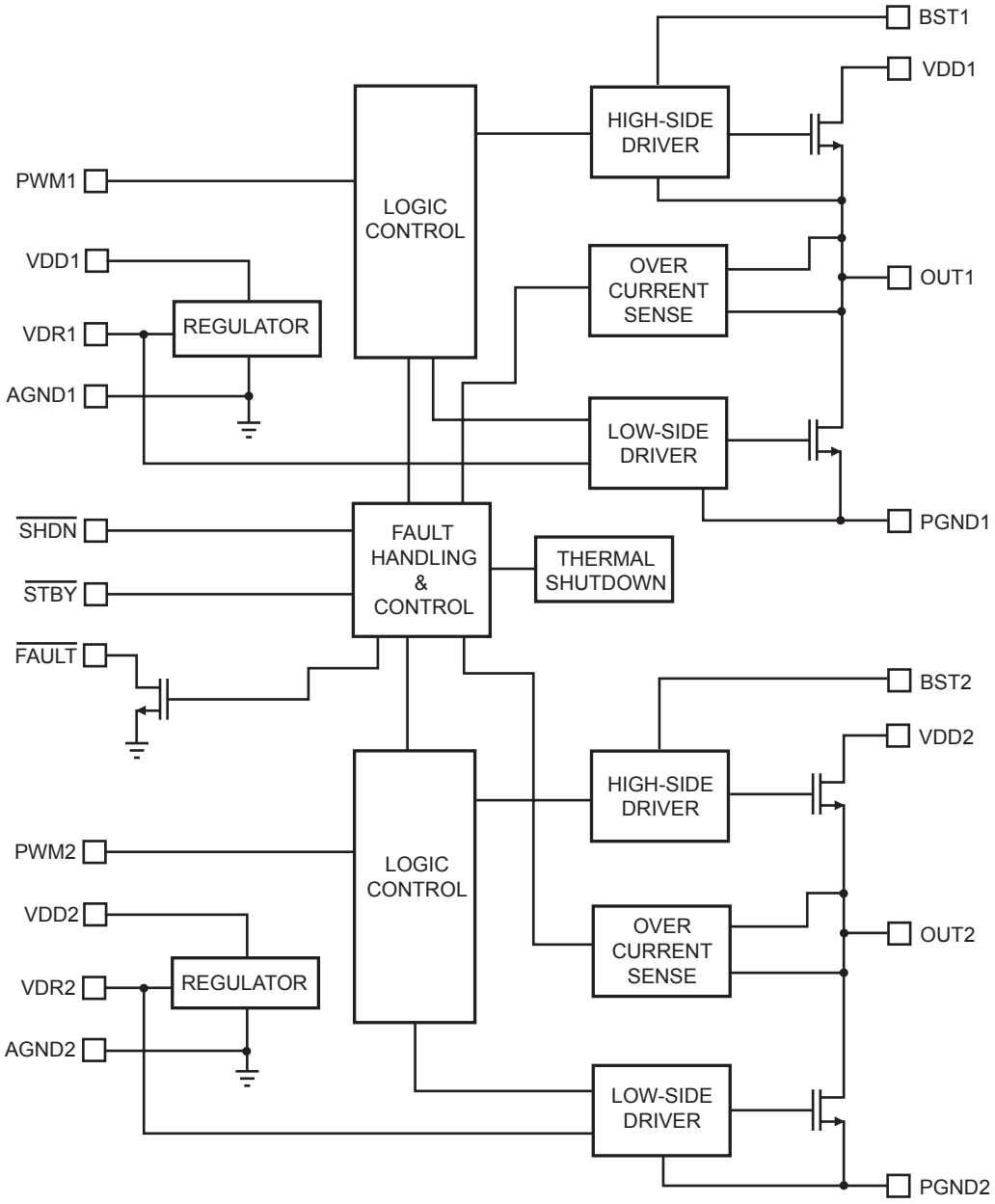
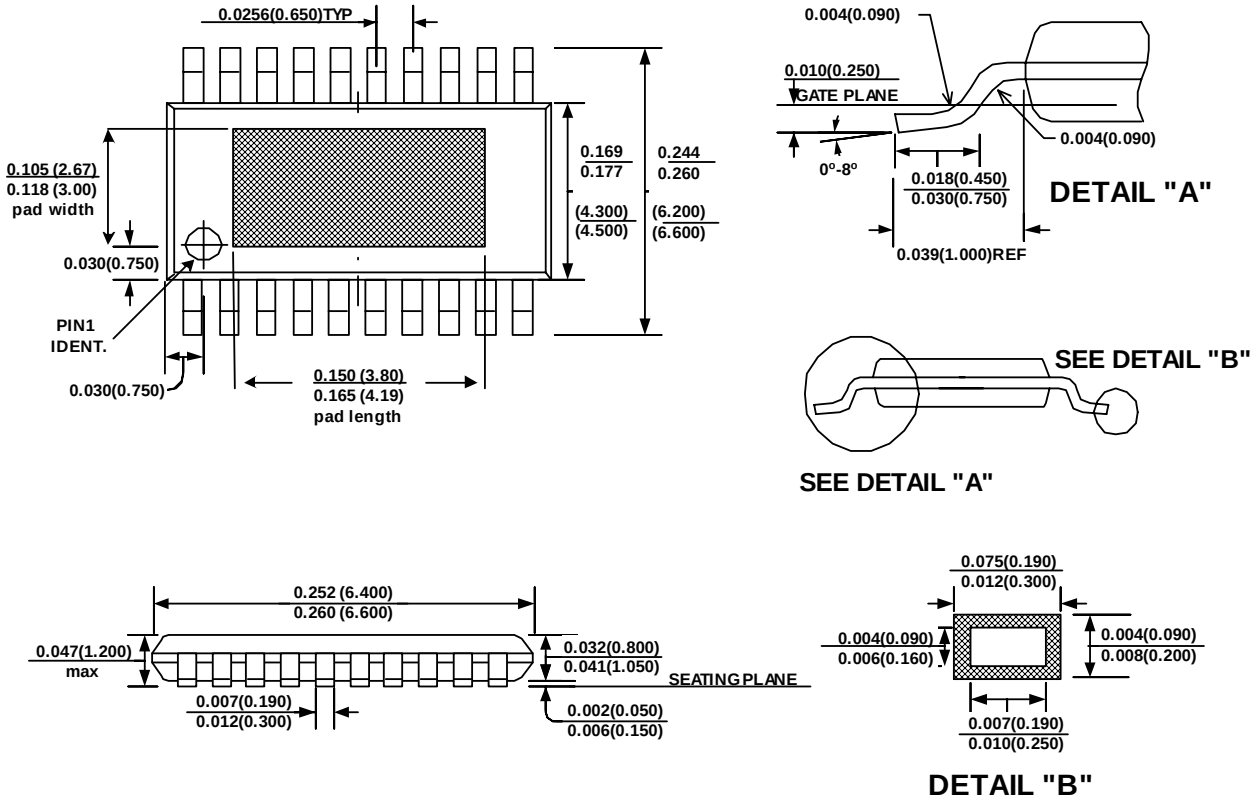


Figure 1—Functional Block Diagram

PACKAGE INFORMATION

TSSOP20F



NOTE:
1) Control dimension is in inches. Dimension in bracket is millimeters.