

# 5-V Low Drop Fixed Voltage Regulator

TLE 4270-2



### Features

- Output voltage tolerance  $\leq \pm 2\%$
- 650 mA output current capability
- Low-drop voltage
- Reset functionality
- Adjustable reset time
- Suitable for use in automotive electronics
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Wide temperature range
- ESD protection: ±2kV HBM<sup>1)</sup>
- Green Product (RoHS compliant)
- AEC Qualified

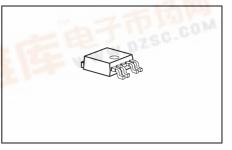


This device is a 5-V low drop fixed-voltage regulator. The maximum input voltage is 42 V (65 V,  $\leq$  400 ms). Up to an input voltage of 26 V and for an output current up to 650 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA. The device incorporates overvoltage protection and a temperature protection which turns off the device at high temperatures.

1) ESD susceptibility, Human Body Model (HBM) according to EIA/JESD 22-A114B

Туре	Package
TLE 4270-2 G	PG-TO263-5-1
TLE 4270-2 D	PG-TO252-5-11







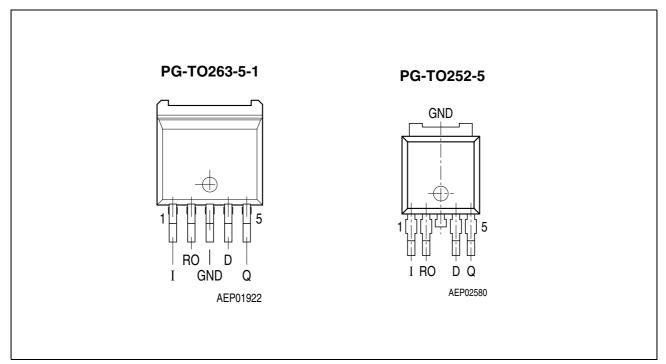


Figure 1	Pin Configuration	(top view)
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## Table 1Pin Definitions and Functions

Pin	Symbol	Function
1	1	Input; block to ground directly at the IC with a ceramic capacitor.
2	RO	<b>Reset Output;</b> the open collector output is connected to the 5-V output via an integrated resistor of 30 k $\Omega$ .
3	GND	Ground; internally connected to heatsink.
4	D	<b>Reset Delay;</b> connect a capacitor to ground for delay time adjustment.
5	Q	<b>5-V Output;</b> block to ground with 22 $\mu$ F capacitor, ESR < 3 $\Omega$ .



### **Circuit Description**

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

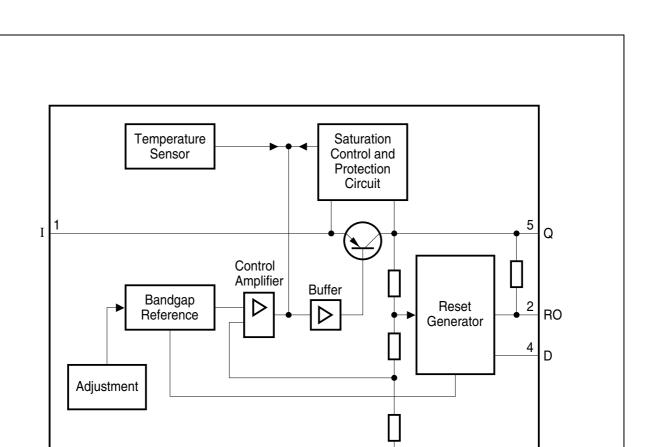
The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

### **Application Description**

The IC regulates an input voltage in the range of 5.5 V <  $V_1$  < 36 V to  $V_{Q,nom}$  = 5.0 V. Up to 26 V it produces a regulated output current of more than 650 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. A reset signal is generated for an output voltage of  $V_Q$  < 4.5 V. The delay for power-on reset can be set externally with a capacitor.





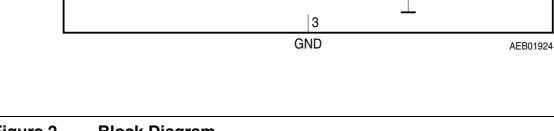


Figure 2 Block Diagram



## Table 2Absolute Maximum Ratings

 $T_{\rm j}$  = -40 to 150 °C

Parameter	Symbol	Lim	it Values	Unit	Notes
		Min.	Max.		
Input I					
Voltage	$V_{\rm I}$	-42	42	V	-
Voltage	$V_1$	-	65	V	<i>t</i> ≤ 400 ms
Current	$I_{\rm I}$	-	-	-	internally limited
Reset Output RO		-		·	
Voltage	$V_{\sf RO}$	-0.3	7	V	-
Current	I <sub>RO</sub>	-	-	-	Internally limited
Reset Delay D		•		•	
Voltage	$V_{D}$	-0.3	7	V	_
Current	ID	-	-	-	Internally limited
Output Q		·	·		·
Voltage	$V_{Q}$	-1.0	16	V	_
Current	IQ	-	-	-	Internally limited
Ground GND					
Current	I <sub>GND</sub>	-0.5	-	A	-
Temperatures		•	•	•	
Junction temperature	T <sub>i</sub>	_	150	°C	_
Storage temperature	$\vec{T}_{stg}$	-50	150	°C	-
		1	1		

### Table 3Operating Range

Parameter	Symbol	Limit Values		Limit Values		Unit	Notes
		Min.	Max.	-			
Input voltage	VI	6	42	V	-		
Junction temperature	Tj	-40	150	°C	-		

### **Thermal Resistance**

Junction ambient	R <sub>thj-a</sub>	_	65 79	K/W K/W	– TO263, TO252 <sup>1)</sup>
Junction case	R <sub>thj-c</sub>	_	3	K/W	TO-263 Packages

1) Mounted on PCB,  $80 \times 80 \times 1.5 \text{ mm}^3$ ;  $35\mu$  Cu;  $5\mu$  Sn; Footprint only; zero airflow.



## Table 4Characteristics

Parameter	Symbol Limit Values			Unit	Test Condition		
		Min.	Тур.	Max.	_		
Output voltage	V <sub>Q</sub>	4.90	5.00	5.10	V	5 mA $\leq I_Q \leq$ 550 mA; 6 V $\leq V_I \leq$ 26 V	
Output voltage	V <sub>Q</sub>	4.90	5.00	5.10	V	$26 \text{ V} \le V_{\text{I}} \le 36 \text{ V};$ $I_{\text{Q}} \le 300 \text{ mA}$	
Output current limiting	I <sub>Qmax</sub>	650	850	-	mA	$V_{\rm Q} = 0 \ {\rm V}$	
Current consumption $I_q = I_1 - I_Q$	Iq	_	1	1.5	mA	I <sub>Q</sub> = 5 mA	
Current consumption $I_q = I_l - I_Q$	Iq	_	55	75	mA	I <sub>Q</sub> = 550 mA	
Current consumption $I_q = I_1 - I_Q$	Iq	_	70	90	mA	$I_{\rm Q} = 550 \text{ mA}; V_{\rm I} = 5 \text{ V}$	
Drop voltage	$V_{DR}$	-	350	700	mV	$I_{\rm Q} = 550 \ {\rm mA}^{1)}$	
Load regulation	$\Delta V_{\rm Q,Lo}$	-	25	50	mV	$I_{\rm Q}$ = 5 to 550 mA; $V_{\rm I}$ = 6 V	
Line regulation	$\Delta V_{Q,Li}$	-	12	25	mV	$V_{\rm I}$ = 6 to 26 V $I_{\rm Q}$ = 5 mA	
Power supply Ripple rejection	PSRR	-	54	-	dB	$f_{\rm r}$ = 100 Hz; $V_{\rm r}$ = 0.5 Vpp	
Reset Generator			·	L			
Switching threshold	$V_{RT}$	4.5	4.65	4.8	V	-	
Reset High voltage	$V_{ROH}$	4.5	-	-	V	-	
Reset low voltage	$V_{ROL}$	-	60	-	mV	$R_{\rm int} = 30 \text{ k}\Omega^{2};$ 1.0 V $\leq V_{\rm Q} \leq 4.5 \text{ V}$	
Reset low voltage	$V_{ROL}$	_	200	400	mV	$I_{\rm R} = 3 \text{ mA}, V_{\rm Q} = 4.4 \text{ V}$	
Reset pull-up	R <sub>int</sub>	18	30	46	kΩ	internally connected to Q	
Charge current	I <sub>D,c</sub>	8	14	25	μA	$V_{\rm D} = 1.0  \rm V$	



### Table 4Characteristics (cont'd)

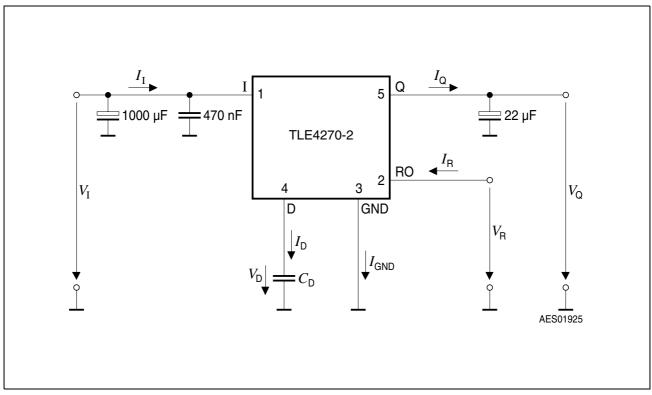
# $V_{\rm I}$ = 13.5 V; -40 °C $\leq$ $T_{\rm j}$ $\leq$ 125 °C (unless otherwise specified)

Parameter	Symbol Limit Values				Unit	<b>Test Condition</b>
		Min.	Тур.	Max.		
Upper reset timing threshold	V <sub>DU</sub>	1.4	1.8	2.3	V	-
Lower reset timing threshold	V <sub>DL</sub>	0.2	0.45	0.8	V	$V_{\rm Q} < V_{\rm RT}$
Delay time	t <sub>rd</sub>	_	13	-	ms	$C_{\rm D} = 100  \rm nF$
Reset reaction time	t <sub>rr</sub>	_	-	3	μs	C <sub>D</sub> = 100 nF
Overvoltage Protec	tion			·		•
Turn-Off voltage	$V_{\rm Lov}$	42	44	46	V	-

I uni-On voltage $V_{I, ov}$ 424446V-1) Drop voltage =  $V_I - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

2) Reset peak is always lower than 1.0 V.







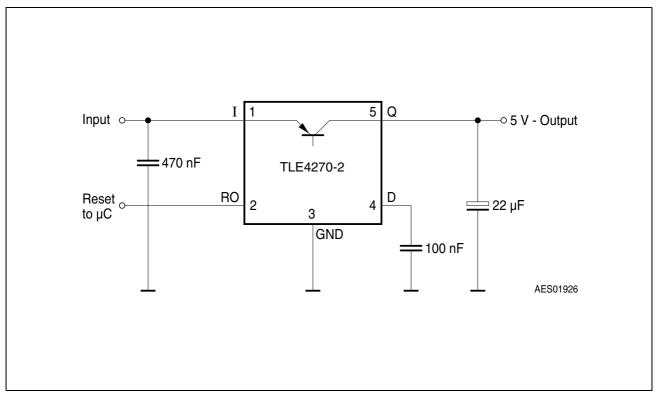


Figure 4 Application Circuit



### **Design Notes for External Components**

An input capacitor  $C_1$  is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1  $\Omega$  in series with  $C_1$ . An output capacitor  $C_{\Omega}$  is necessary for the stability of the regulating circuit. Stability is guaranteed at values of  $C_0 \ge 22 \ \mu\text{F}$  and an ESR of < 3 Ω.

### **Reset Circuitry**

If the output voltage decreases below 4.5 V, an external capacitor  $C_{\rm D}$  on pin 4 (D) will be discharged by the reset generator. If the voltage on this capacitor drops below  $V_{\text{DL}}$ , a reset signal is generated on pin 2 (RO), i.e. reset output is set low. If the output voltage rises above the reset threshold,  $C_{\rm D}$  will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches  $V_{DU}$  and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of  $C_{\rm D}$ .

### Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor  $C_{\rm D}$  which can be calculated as follows:

$$C_{\rm D} = (\Delta t \times I_{\rm D,c}) / \Delta V$$

**Definitions:** 

- $C_{\rm D}$  = delay capacitors
- $\Delta t = \text{reset delay time } t_{\text{rd}}$
- $I_{D,c}$  = charge current, typical 14 µA
- $\Delta V = V_{\rm DU}$ , typical 1.8 V

 $V_{\rm DU}$  = upper reset timing threshold at  $C_{\rm D}$  for reset delay time

$$t_{\rm rd} = \Delta V \times C_{\rm D} / I_{\rm D,c} \tag{2}$$

The reset reaction time  $t_{rr}$  is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1  $\mu$ s for delay capacitor of 47 nF. For other values for  $C_{\rm D}$  the reaction time can be estimated using the following equation:

$$t_{\rm rr} \approx 20 \ {\rm s/F} \times C_{\rm D}$$
 (3)

(1)



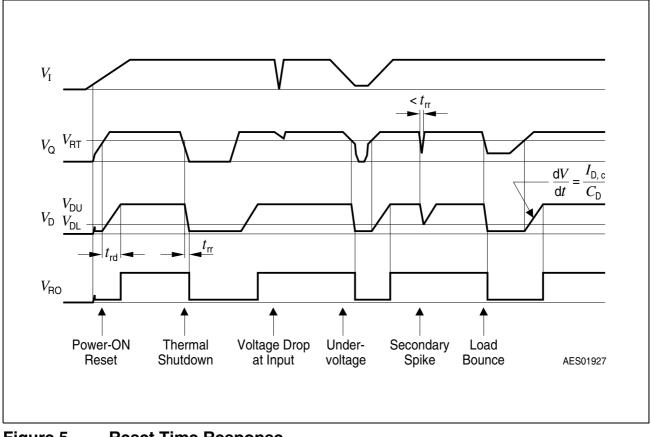
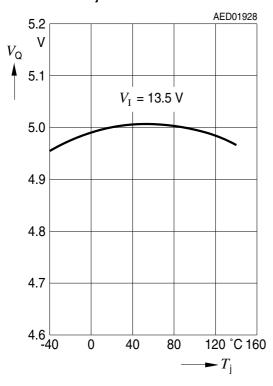


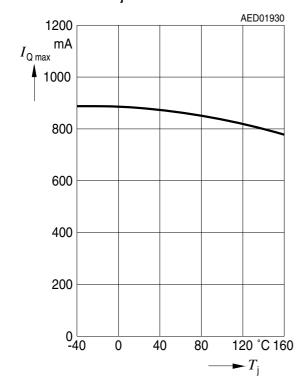
Figure 5 **Reset Time Response** 



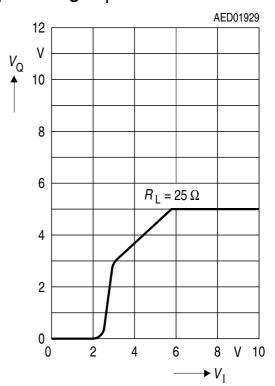
Output Voltage  $V_{Q}$  versus Temperature  $T_{j}$ 



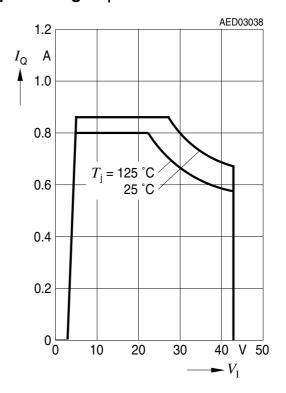
Output Current  $I_Q$  versus Temperature  $T_i$ 



Output Voltage  $V_{\rm Q}$  versus Input Voltage  $V_{\rm I}$ 

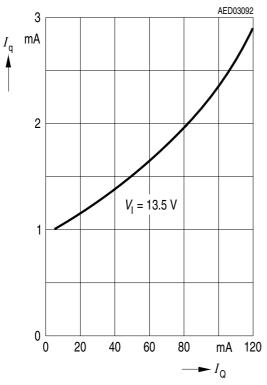


# Output Current $I_Q$ versus Input Voltage $V_I$

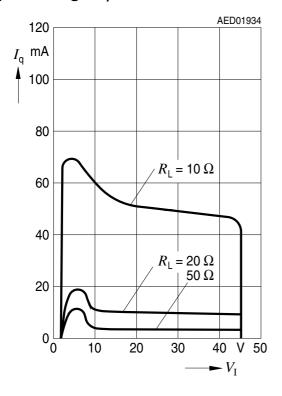




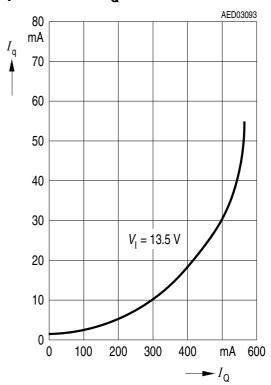
Current Consumption  $I_q$  versus Output Current  $I_Q$ 



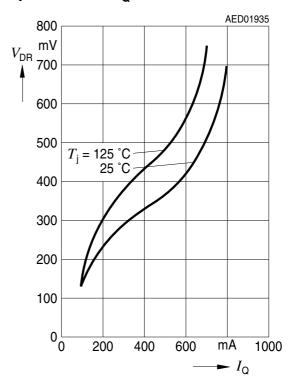
### Current Consumption $I_q$ versus Input Voltage $V_l$



Current Consumption  $I_q$  versus Output Current  $I_o$ 

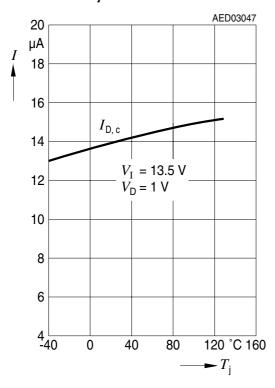


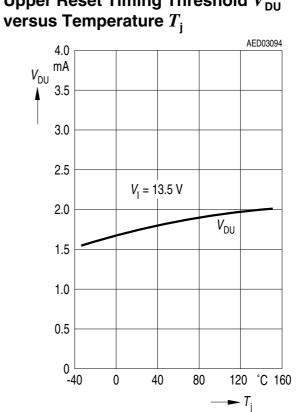
### Drop Voltage $V_{\text{DR}}$ versus Output Current $I_{\text{O}}$





Charge Current  $I_{\rm D,c}$  versus Temperature  $T_{\rm j}$ 

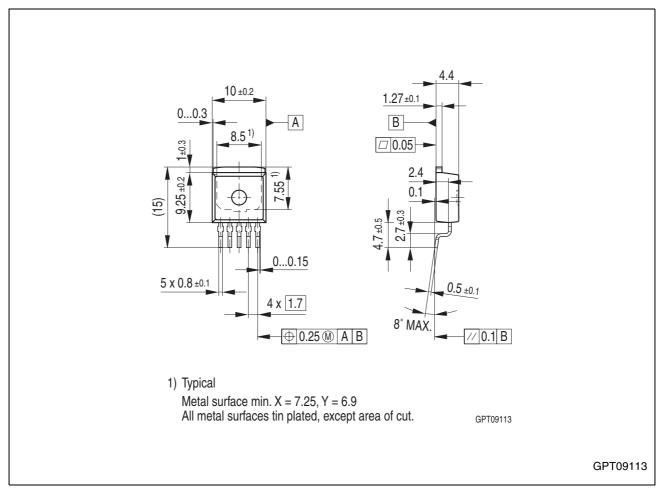




Upper Reset Timing Threshold  $V_{\rm DU}$ 



### **Package Outlines**





### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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SMD = Surface Mounted Device

Dimensions in mm



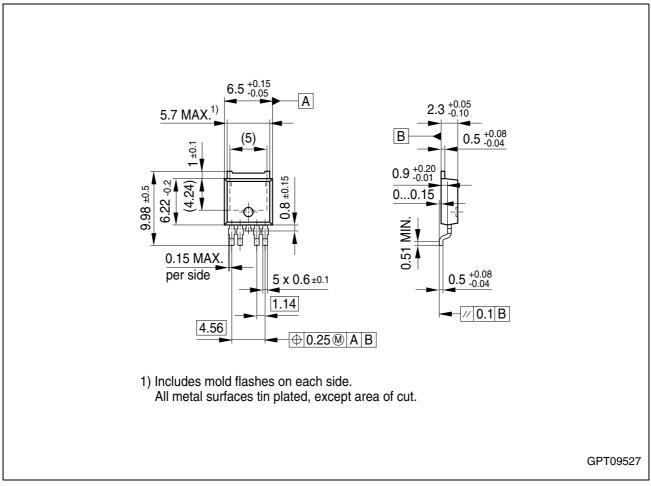


Figure 7 PG-TO252-5-11 (Plastic Transistor Single Outline)

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# **Revision History**

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Version	Date	Changes
Rev. 1.8	2007-11-09	Page 1: Changed ESD specification from ">4000V" to "±2kV HBM" according to PCN No. 2007-089
Rev. 1.7	2007-03-20	Initial version of RoHS-compliant derivate of TLE 4270 Change of product name to TLE 4270-2 due to modified chip layout and size. Page 1: AEC certified statement added Page 1 and Page 14: RoHS compliance statement and Green product feature added Page 1 and Page 14: Package changed to RoHS compliant version Legal Disclaimer updated

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