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JEITA Guideline Compatible Stand-Alone Synchronous Switch-Mode Li-Ion or Li-Polymer Battery Charger with System Power Selector and Low I_q

Check for Samples: bq24616

FEATURES

- Battery Thermistor Sense for JEITA Guideline Compatible Charger
- 600 kHz NMOS-NMOS Synchronous Buck Converter
- Stand-alone Charger Support for Li-Ion or Li-Polymer
- 5 V–28 V VCC Input Operating Range and Supports 1-6 Battery Cells
- Up to 10A Charge Current and Adapter Current
- High-Accuracy Voltage and Current Regulation
  - ±0.5% Charge Voltage Accuracy
  - ±3% Charge Current Accuracy
  - ±3% Adapter Current Accuracy
- Integration
  - Automatic System Power Selection from Adapter or Battery
  - Internal Loop Compensation
  - Internal Soft Start
  - Dynamic Power Management
- Safety Protection
  - Input Over-Voltage Protection
  - Battery Detection
  - Reverse Protection Input FET
  - Programmable Safety Timer
  - Charge Over-Current Protection
  - Battery Short Protection
  - Battery Over-Voltage Protection
  - Thermal Shutdown
- Status Outputs
  - Adapter Present
  - Charger Operation Status
- Charge Enable Pin
- 6 V Gate Drive for Synchronous Buck Converter
- 30 ns Driver Dead-time and 99.5% Max Effective Duty Cycle
- 24-pin, 4×4-mm^2 QFN Package
- Energy Star Low Quiescent Current I_q
  - < 15 µA Off-State Battery Discharge current
  - < 1.5 mA Off-State Input Quiescent Current

APPLICATIONS

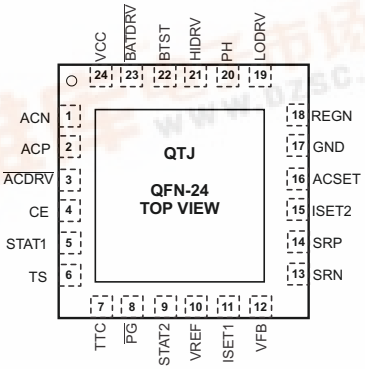
- Netbook, Mobile Internet Device and Ultra-Mobile PC
- Industrial and Medical Equipment
- Personal Digital Assistants
- Handheld Terminals
- Portable Equipment

DESCRIPTION

The bq24616 is highly integrated, JEITA (Japan Electronic Information Technology Association) guideline compatible, Li-ion or Li-polymer switch-mode battery charge controller. It offers a constant-frequency synchronous switching PWM controller with high accuracy charge current and voltage regulation, charge preconditioning, termination, adapter current regulation, and charge status monitoring.

The bq24616 charges the battery in three phases: preconditioning, constant current, and constant voltage. Charge is terminated when the current reaches a minimum user-selectable level. A programmable charge timer provides a safety backup. The bq24616 automatically restarts the charge cycle if the battery voltage falls below an internal threshold, and enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage.

PACKAGE AND PIN-OUT



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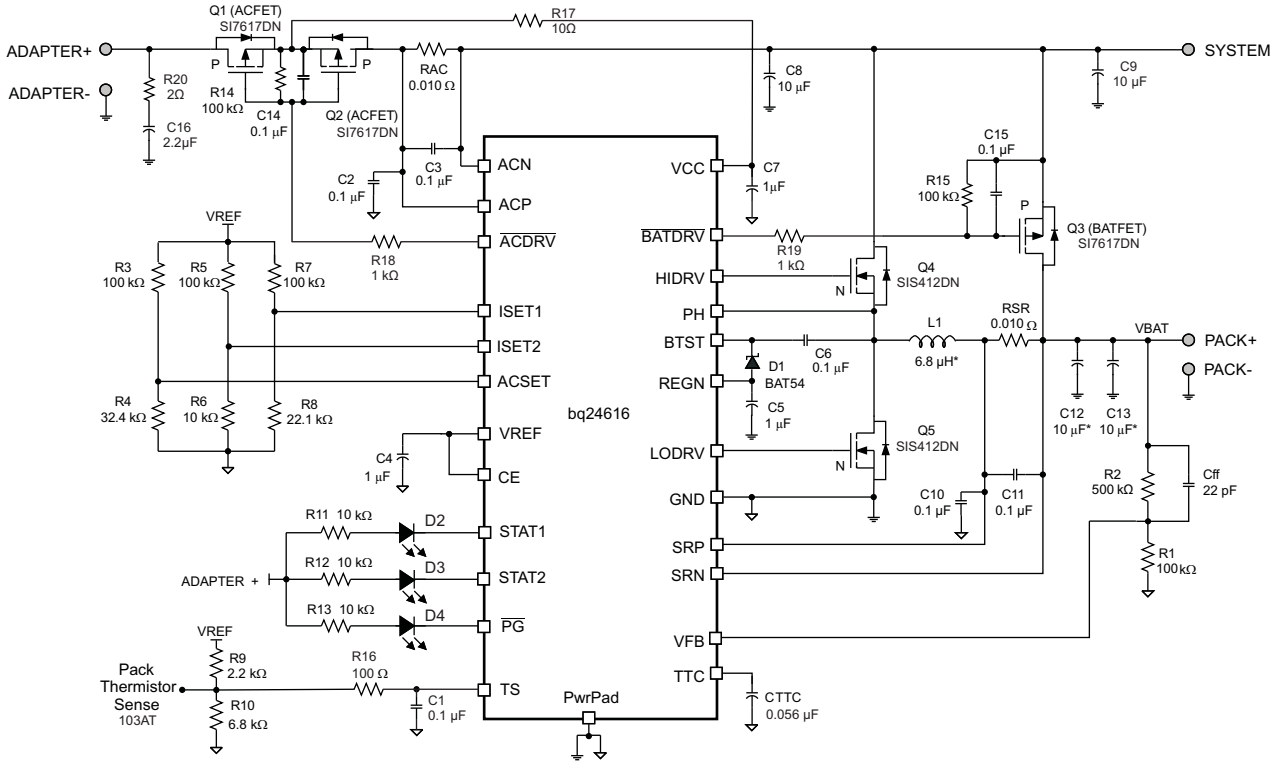
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The bq24616 controls external switches to prevent battery discharge back to the input and to connect the battery to the system using 6-V gate drives for system efficiency. The bq24616 features Dynamic Power Management (DPM). The DPM reduces battery charge current when the input power limit is reached to avoid overloading the AC adapter while supplying the load and the battery charger simultaneously. A highly-accurate current-sense amplifier enables precise measurement of input current from the AC adapter to monitor the overall system power.

TYPICAL APPLICATION



VIN=19V; 3-cell; $I_{adapter\_limit}$=4A; $I_{pre\text{-}charge}$= I_{term}=0.3A; 5 hour safety timer; I_{charge}=1.5A (0-10°C), 3A (10-60°C); V_{BAT}=12.6V (0-45°C), 12.3V (45-50°C), 12.15V (50-60°C).

Figure 1. Typical System Schematic

ORDERING INFORMATION

PART NUMBER	IC MARKING	PACKAGE	ORDERING NUMBER (Tape and Reel)	QUANTITY
bq24616	QTJ	24-PIN 4×4 mm^2 QFN	bq24616RGER	3000
			bq24616RGET	250

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PACKAGE THERMAL DATA

PACKAGE	θ_{JP}	θ_{JA}	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
QFN – RGE (1)(2)	4°C/W	43°C/W	2.3 W	0.023 W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2×2 via matrix. θ_{JA} has 5% improvement by 3x3 via matrix.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			VALUE		UNIT
			MIN	MAX	
	Voltage range	VCC, ACP, ACN, SRP, SRN, $\overline{\text{BATDRV}}$, $\overline{\text{ACDRV}}$, CE, STAT1, STAT2, $\overline{\text{PG}}$	–0.3	33	V
		PH	–2	36	V
		VFB	–0.3	16	V
		REGN, LODRV, ACSET, TS, TTC	–0.3	7	V
		BTST, HIDRV with respect to GND	–0.3	39	V
		VREF, ISET1, ISET2	–0.3	3.6	V
	Maximum difference voltage	ACP–ACN, SRP–SRN	–0.5	0.5	V
T_J	Junction temperature range		–40	155	°C
T_{stg}	Storage temperature range		–55	155	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.
(3) Must have a series resistor between battery pack to VFB if Battery Pack voltage is expected to be greater than 16V. Usually the resistor divider top resistor will take care of this.

RECOMMENDED OPERATING CONDITIONS

			VALUE		UNIT
			MIN	MAX	
	Voltage range	VCC, ACP, ACN, SRP, SRN, $\overline{\text{BATDRV}}$, $\overline{\text{ACDRV}}$, CE, STAT1, STAT2, $\overline{\text{PG}}$	–0.3	28	V
		PH	–2	30	V
		VFB	–0.3	14	V
		REGN, LODRV, ACSET, TS, TTC	–0.3	6.5	V
		BTST, HIDRV with respect to GND	–0.3	34	V
		ISET1, ISET2	–0.3	3.3	V
		VREF	0	3.3	V
	Maximum difference voltage	ACP–ACN, SRP–SRN	–0.2	0.2	V
T_J	Junction temperature range		0	125	°C
T_{stg}	Storage temperature range		–55	155	°C

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ELECTRICAL CHARACTERISTICS

5.0V ≤ V(VCC) ≤ 28V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{VCC_OP}	VCC input voltage operating range		5.0		28.0	V
QUIESCENT CURRENTS						
I_{BAT}	Total battery discharge current (sum of currents into VCC, BTST, PH, ACP, ACN, SRP, SRN, VFB), $V_{FB} \le V_{FB\_REG}$	$V_{VCC} < V_{SRN}$, $V_{VCC} > V_{UVLO}$ (SLEEP)			15	µA
	Battery discharge current (sum of currents into BTST, PH, SRP, SRN, VFB), $V_{FB} \le V_{FB\_REG}$	$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{UVLO}$ CE = LOW			5	µA
		$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{VCCLOW}$ CE = HIGH, Charge done			5	µA
I_{AC}	Adapter supply current (current into VCC,ACP,ACN pin)	$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{UVLO}$ CE = LOW (IC quiescent current)		1	1.5	mA
		$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{VCCLOW}$, CE = HIGH, charge done		2	5	
		$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{VCCLOW}$, CE = HIGH, Charging, Qg_total = 20 nC		25		
CHARGE VOLTAGE REGULATION						
V_{FB_REG}	Feedback Regulation Voltage	$V_{T3} < V_{TS} < V_{T1}$		2.1		V
		$V_{T4} < V_{TS} < V_{T3}$		2.05		
		$V_{T5} < V_{TS} < V_{T4}$		2.025		
	Charge Voltage Regulation Accuracy	T_J = 0 to 85°C	–0.5%		–0.5%	
		T_J = –40 to 125°C	–0.7%		–0.7%	
I_{VFB}	Leakage Current into V_{FB} pin	V_{FB} = 2.1V, 2.05V, 2.025V			100	nA
CURRENT REGULATION – FAST CHARGE						
V_{ISET1}	ISET1 voltage range				2	V
V_{IREG_CHG}	SRP-SRN current sense voltage range	$V_{IREG\_CHG} = V_{SRP} - V_{SRN}$			100	mV
K_{ISET1}	Charge current set factor (amps of charge current per volt on ISET1 pin)	R_{SENSE} = 10 mΩ		5		A/V
	Charge current regulation accuracy	V_{IREG_CHG} = 40 mV	–3%		3%	
		V_{IREG_CHG} = 20 mV	–4%		4%	
		V_{IREG_CHG} = 5 mV	–25%		25%	
		V_{IREG_CHG} = 1.5 mV (V_{SRN} > 3.1V)	–40%		40%	
I_{ISET1}	Leakage current into ISET1 pin	V_{ISET1} = 2 V			100	nA
CURRENT REGULATION – PRECHARGE						
V_{ISET2}	ISET2 voltage range				2	V
K_{ISET2}	Precharge current set factor (amps of precharge current per volt on ISET2 pin)	R_{SENSE} = 10 mΩ		1		A/V
	Precharge current regulation accuracy	V_{IREG_PRECH} = 20 mV	–4%		4%	
		V_{IREG_PRECH} = 5 mV	–25%		25%	
		V_{IREG_PRECH} = 1.5 mV (V_{SRN} < 3.1V)	–55%		55%	
I_{ISET2}	Leakage current into ISET2 pin	V_{ISET2} = 2V			100	nA

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE TERMINATION						
K_{TERM}	Termination current set factor (Amps of termination current per volt on ISET2 pin)	R_{SENSE} = 10 mΩ		1		A/V
	Termination current accuracy	V_{ITERM} = 20 mV	–4%		4%	
		V_{ITERM} = 5 mV	–25%		25%	
		V_{ITERM} = 1.5 mV	–45%		45%	
	Deglitch time for termination (both edge)			100		ms
t_{QUAL}	Termination qualification time	V_{BAT}>V_{RECH} and I_{CHG}<I_{TERM}		250		ms
I_{QUAL}	Termination qualification current	Discharge current once termination is detected		2		mA
INPUT CURRENT REGULATION						
V_{ACSET}	ACSET Voltage Range				2	V
V_{IREG_DPM}	ACP-ACN Current Sense Voltage Range	V_{IREG_DPM} = V_{ACP} – V_{ACN}			100	mV
K_{ACSET}	Input current set factor (amps of input current per volt on ACSET pin)	R_{SENSE} = 10 mΩ		5		A/V
I_{ACSET}	Input current regulation accuracy leakage current in to ACSET pin	V_{IREG_DPM} = 40 mV	–3%		3%	
		V_{IREG_DPM} = 20 mV	–4%		4%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
I_{ISET1}	Leakage current in to ACSET pin	V_{ACSET} = 2 V			100	nA
INPUT UNDER-VOLTAGE LOCK-OUT COMPARATOR (UVLO)						
V_{UVLO}	AC Under-voltage rising threshold	Measure on VCC	3.65	3.85	4	V
V_{UVLO_HYS}	AC Under-voltage hysteresis, falling			350		mV
VCC LOWV COMPARATOR						
	Falling threshold, disable charge	Measure on VCC		4.1		V
	Rising threshold, resume charge			4.35	4.5	V
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
V_{SLEEP_FALL}	SLEEP falling threshold	V_{VCC} – V_{SRN} to enter SLEEP	40	100	150	mV
V_{SLEEP_HYS}	SLEEP hysteresis			500		mV
	SLEEP rising delay	VCC falling below SRN, Delay to turn off ACFET		1		µs
	SLEEP falling delay	VCC rising above SRN, Delay to turn on ACFET		30		ms
	SLEEP rising shutdown deglitch	VCC falling below SRN, Delay to enter SLEEP mode		100		ms
	SLEEP falling powerup deglitch	VCC rising above SRN, Delay to exit SLEEP mode		30		ms
ACN / SRN COMPARATOR						
$V_{ACN\text{-}SRN\_FALL}$	ACN to SRN falling threshold	V_{ACN} – V_{SRN} to turn on BATFET	100	200	310	mV
$V_{ACN\text{-}SRN\_HYS}$	ACN to SRN rising hysteresis			100		mV
	ACN to SRN rising deglitch	V_{ACN} – V_{SRN} > $V_{ACN\text{-}SRN\_RISE}$		2		ms
	ACN to SRN falling deglitch	V_{ACN} – V_{SRN} < $V_{ACN\text{-}SRN\_FALL}$		50		µs
BAT LOWV COMPARATOR						
V_{LOWV}	Precharge to fastcharge transition (LOWV threshold)	Measured on VFB pin, Rising	1.534	1.55	1.566	V
V_{LOWV_HYS}	LOWV hysteresis			100		mV
	LOWV rising deglitch	VFB falling below V_{LOWV}		25		ms
	LOWV falling deglitch	VFB rising above V_{LOWV} + V_{LOWV_HYS}		25		ms
RECHARGE COMPARATOR						
V_{RECHG}	Recharge threshold (with-respect-to V_{REG})	Measured on VFB pin, Falling	35	50	65	mV
	Recharge rising deglitch	VFB decreasing below V_{RECHG}		10		ms
	Recharge falling deglitch	VFB decreasing above V_{RECHG}		10		ms

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ELECTRICAL CHARACTERISTICS (continued)

5.0V ≤ V(VCC) ≤ 28V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BAT OVER-VOLTAGE COMPARATOR						
V_{OV_RISE}	Over-voltage rising threshold	As percentage of V_{FB} ,T1 – T5		104%		
V_{OV_FALL}	Over-voltage falling threshold	As percentage of V_{FB},T1 – T5		102%		
INPUT OVER-VOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC over-voltage rising threshold on VCC		31.04	32	32.96	V
V_{ACOV_HYS}	AC over-voltage falling hysteresis			1		V
	AC over-voltage deglitch (both edge)	Delay to changing the STAT pins		1		ms
	AC over-voltage rising deglitch	Delay to turn-off ACFET, disable charge		1		ms
	AC over-voltage falling deglitch	Delay to turn on ACFET, resume charge		20		ms
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		145		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			15		°C
	Thermal shutdown rising deglitch	Temperature increasing		100		µs
	Thermal shutdown falling deglitch	Temperature decreasing		10		ms
THERMISTOR COMPARATOR						
V_{T1}	T1 (0 °C) threshold, Charge suspended below this temperature.	V_{TS} rising, As Percentage to V_{VREF}	70.2%	70.8%	71.4%	
V_{T1-HYS}	Charge back to I_{CHARGE}/2 and V_{FB}=2.1 V above this temperature.	Hysteresis, V_{TS} falling		0.6%		
V_{T2}	T2 (10 °C) threshold, Charge back to I_{CHARGE}/2 and V_{FB}=2.1 V below this temperature.	V_{TS} rising, As Percentage to V_{VREF}	68.0%	68.6%	69.2%	
V_{T2-HYS}	Charge back to I_{CHARGE} and V_{FB}=2.1 V above this temperature.	Hysteresis, V_{TS} falling		0.8%		
V_{T3}	T3 (45 °C) threshold, Charge back to I_{CHARGE} and V_{FB}=2.05 V above this temperature.	V_{TS} falling, As Percentage to V_{VREF}	55.5%	56.1%	56.7%	
V_{T3-HYS}	Charge back to I_{CHARGE} and V_{FB}=2.1 V below this temperature.	Hysteresis, V_{TS} rising		0.8%		
V_{T4}	T4 (50 °C) threshold, Charge back to I_{CHARGE} and V_{FB}=2.025 V above this temperature.	V_{TS} falling, As Percentage to V_{VREF}	53.2%	53.7%	54.2%	
V_{T4-HYS}	Charge back to I_{CHARGE} and V_{FB}=2.05 V below this temperature.	Hysteresis, V_{TS} rising		0.8%		
V_{T5}	T5 (60 °C) threshold, Charge suspended above this temperature.	V_{TS} falling, As Percentage to V_{VREF}	47.6%	48.1%	48.6%	
V_{T5-HYS}	Charge back to I_{CHARGE} and V_{FB}=2.025 V below this temperature.	Hysteresis, V_{TS} rising		1.2%		
	Deglitch time for Temperature Out of Valid Charge Range Detection	V_{TS} < V_{T5} or V_{TS} > V_{T1}		400		ms
	Deglitch time for Temperature In Valid Range Detection	V_{TS} > V_{T5} + V_{T5_HYS} or V_{TS} < V_{T1} - V_{T1_HYS}		20		
	Deglitch time for Temperature Detection above/below T2, T3, T4 threshold			25		ms
	Charge Current when V_{TS} between V_{T1} and V_{T2} range			I_{CHARGE} /2		
CHARGE OVER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{OC}	Charge over-current falling threshold	Current rising, in non-synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} < 2 V		45.5		mV
		Current rising, as percentage of $V_{(IREG\_CHG)}$, in synchronous mode, V_{SRP} > 2.2V		160%		
	Charge over-current threshold floor	Minimum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2V		50		mV
	Charge over-current threshold ceiling	Maximum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2V		180		mV

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ELECTRICAL CHARACTERISTICS (continued)

5.0V ≤ V(VCC) ≤ 28V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
$V_{ISYNSET}$	Charge under-current falling threshold	Switch from SYNCH to NON-SYNCH, V_{SRP} > 2.2V	1	5	9	mV
BATTERY SHORTED COMPARATOR (BATSHORT)						
V_{BATSHT}	BAT Short falling threshold, forced non-syn mode	V_{SRP} falling		2		V
V_{BATSHT_HYS}	BAT short rising hysteresis			200		mV
V_{BATSHT_DEG}	Deglitch on both edge			1		µs
LOW CHARGE CURRENT COMPARATOR						
V_{LC}	Low charge current (average) falling threshold to force into non-synchronous mode	Measure on $V_{(SRP-SRN)}$		1.25		mV
V_{LC_HYS}	Low charge current rising hysteresis			1.25		mV
V_{LC_DEG}	Deglitch on both edge			1		µs
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{VCC} > V_{UVLO}, (0-35mA load)	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0V, V_{VCC} > V_{UVLO}	35			mA
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{VCC} > 10V, CE = HIGH, (0-40mA load)	5.7	6.0	6.3	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0V, V_{VCC} > V_{UVLO}, CE = HIGH	40			mA
TTC INPUT AND SAFETY TIMER						
T_{PRECHG}	Precharge safety timer range(1)	Precharge time before fault occurs	1440	1800	2160	sec
T_{CHARGE}	Fast charge safety timer range, with +/- 10% accuracy(1)	Tchg = C_{TTC} × K_{TTC}	1		10	Hr
	Fast charge timer accuracy(1)	0.01 µF ≤ C_{TTC} ≤ 0.11 µF	–10%		10%	
K_{TTC}	Timer multiplier			5.6		min/nF
	TTC low threshold	V_{TTC} below this threshold disables the safety timer and termination			0.4	V
	TTC oscillator high threshold			1.5		V
	TTC oscillator low threshold			1		V
	TTC source/sink current		45	50	55	µA
BATTERY SWITCH (BATFET) DRIVER						
$R_{DS\_BAT\_OFF}$	BATFET turn-off resistance	V_{ACN} > 5V			150	Ω
$R_{DS\_BAT\_ON}$	BATFET turn-on resistance	V_{ACN} > 5V			20	kΩ
V_{BATDRV_REG}	BATFET drive voltage	V_{BATDRV_REG} = V_{ACN} – V_{BATDRV} when V_{ACN} > 5V and BATFET is on	4.2		7	V
AC SWITCH (ACFET) DRIVER						
$R_{DS\_AC\_OFF}$	ACFET turn-off resistance	V_{VCC} > 5V			30	Ω
$R_{DS\_AC\_ON}$	ACFET turn-on resistance	V_{VCC} > 5V			20	kΩ
V_{ACDRV_REG}	ACFET drive voltage	V_{ACDRV_REG} = V_{VCC} – V_{ACDRV} when V_{VCC} > 5V and ACFET is on	4.2		7	V
AC / BAT MOSFET DRIVERS TIMING						
	Driver dead time	Dead time when switching between AC and BAT		10		µs

(1) Verified by design

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ELECTRICAL CHARACTERISTICS (continued)

5.0V ≤ V(VCC) ≤ 28V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY DETECTION						
t_{WAKE}	Wake time	Max time charge is enabled		500		ms
I_{WAKE}	Wake current	R_{SENSE} = 10mΩ	50	125	200	mA
$t_{DISCHARGE}$	Discharge time	Max time discharge current is applied		1		sec
$I_{DISCHARGE}$	Discharge current			8		mA
I_{FAULT}	Fault current after a timeout fault			2		mA
V_{WAKE}	Wake threshold (with-respect-to V_{REG})	Voltage on VFB to detect battery absent during Wake		50		mV
V_{DISCH}	Discharge threshold	Voltage on VFB to detect battery absent during discharge		1.55		V
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS\_HI\_ON}$	High side driver (HSD) turn-on resistance	$V_{BTST} – V_{PH}$ = 5.5 V		3.3	6	Ω
$R_{DS\_HI\_OFF}$	High side driver turn-off resistance	$V_{BTST} – V_{PH}$ = 5.5 V		1	1.3	Ω
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold voltage	$V_{BTST} – V_{PH}$ when low side refresh pulse is requested	4.0	4.2		V
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS\_LO\_ON}$	Low side driver (LSD) turn-on resistance			4.1	7	Ω
$R_{DS\_LO\_OFF}$	Low side driver turn-off resistance			1	1.4	Ω
PWM DRIVERS TIMING						
	Driver dead time	Dead time when switching between LSD and HSD, no load at LSD and HSD		30		ns
PWM OSCILLATOR						
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of VCC		7		%
	PWM switching frequency		510	600	690	kHz
INTERNAL SOFT START (8 steps to regulation current ICHG)						
	Soft start steps			8		step
	Soft start step time			1.6		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power-up	Delay from CE=1 to charger is allowed to turn on		1.5		s
LOGIC IO PIN CHARACTERISTICS (CE, STAT1, STAT2, $\overline{PG}$)						
V_{IN_LO}	CE input low threshold voltage				0.8	V
V_{IN_HI}	CE input high threshold voltage		2.1			
V_{BIAS_CE}	CE input bias current	V = 3.3V (CE has internal 1MΩ pulldown resistor)			6	µA
V_{OUT_LO}	STAT1, STAT2, $\overline{PG}$ output low saturation voltage	Sink Current = 5 mA			0.5	V
I_{OUT_HI}	Leakage current	V = 32 V			1.2	µA

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TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

	Figure
REF REGN and $\overline{PG}$ Power Up (CE=1)	Figure 2
Charge Enable	Figure 3
Current Soft-Start (CE=1)	Figure 4
Charge Disable	Figure 5
Continuous Conduction Mode Switching Waveforms	Figure 6
Cycle-by-Cycle Synchronous to Nonsynchronous	Figure 7
Transient System Load (DPM)	Figure 8
Battery Insertion	Figure 9
Battery to Ground Short Protection	Figure 10
Battery to ground Short Transition	Figure 11
Efficiency vs Output Current	Figure 12

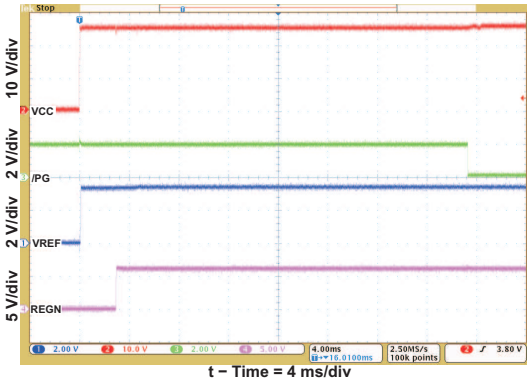

Figure 2. REF REGN and $\overline{PG}$ Power Up (CE=1)

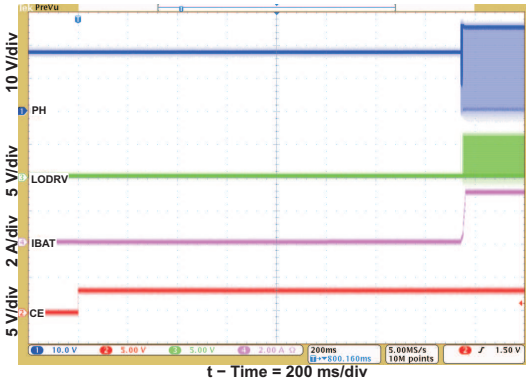

Figure 3. Charge Enable

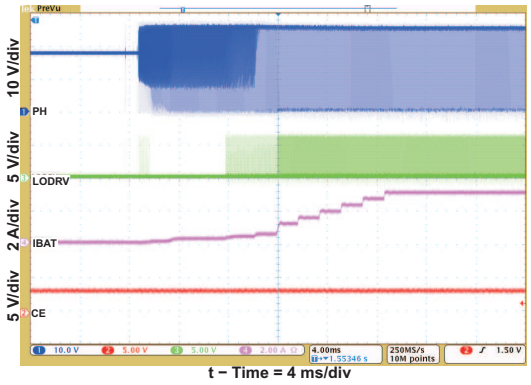

Figure 4. Current Soft-Start (CE=1)

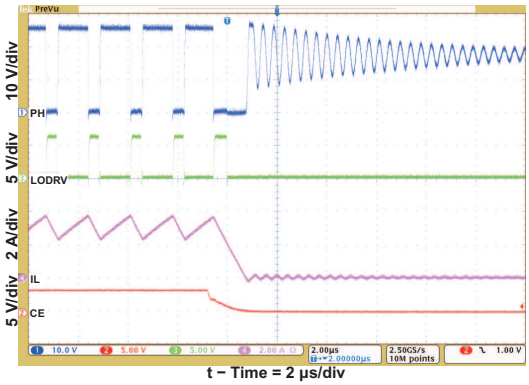

Figure 5. Charge Disable

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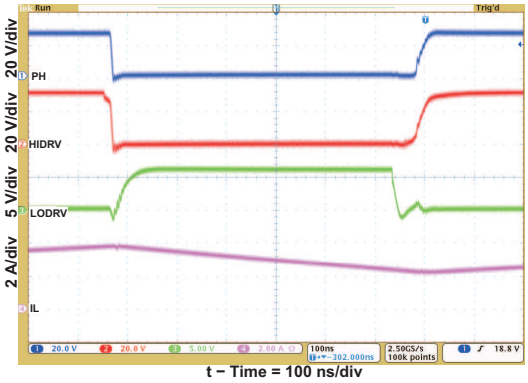

Figure 6. Continuous Conduction Mode Switching Waveform

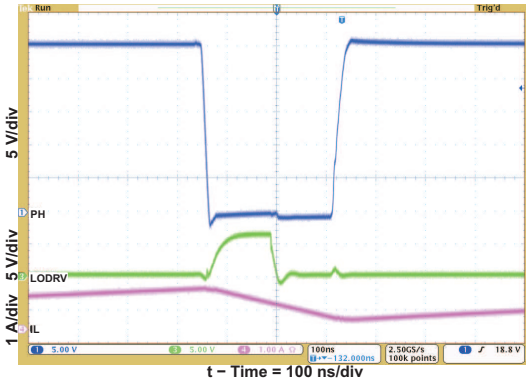

Figure 7. Cycle-by-Cycle Synchronous to Nonsynchronous

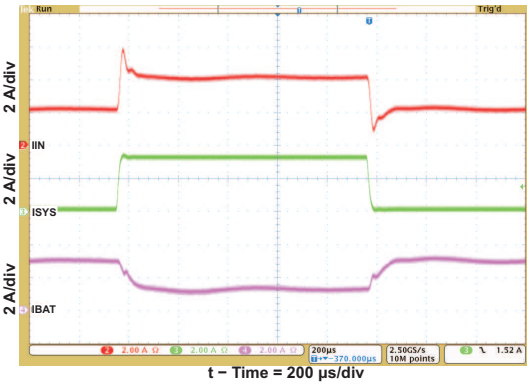

Figure 8. Transient System Load (DPM)

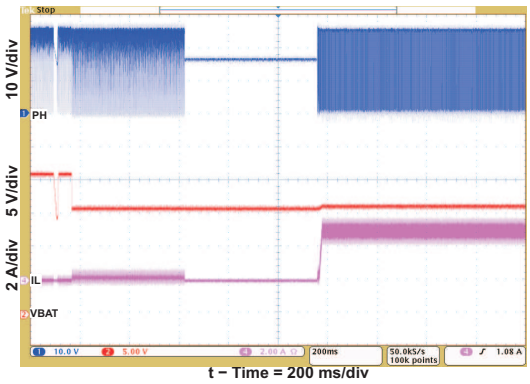

Figure 9. Battery Insertion

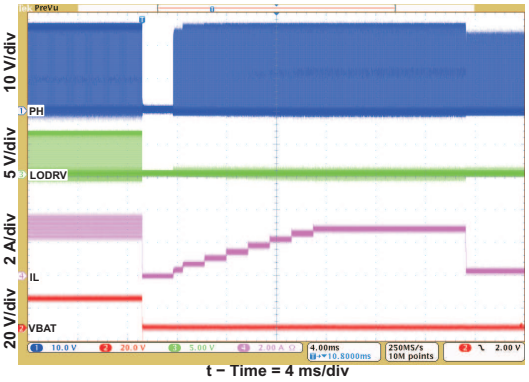

Figure 10. Battery to GND Short Protection

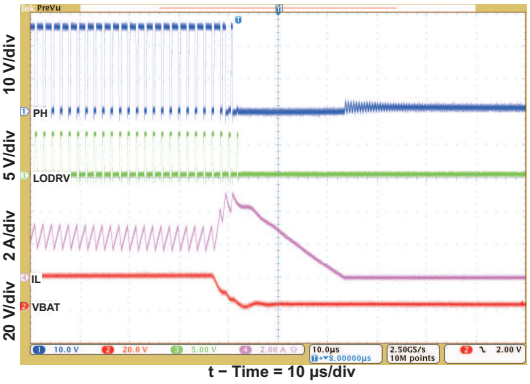

Figure 11. Battery to GND Short Transition

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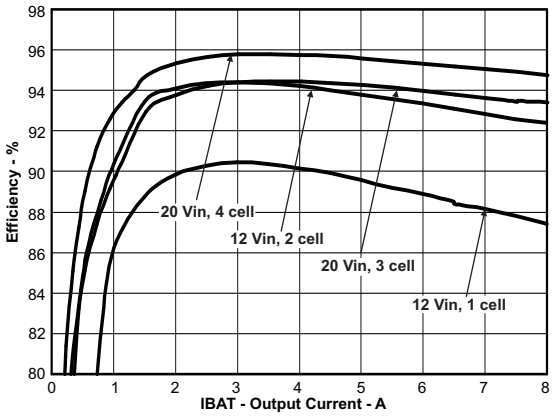

Figure 12. Efficiency vs Output Current

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Pin Functions – 24-Pin QFN

PIN			FUNCTION DESCRIPTION
NO.	NAME	I/O	
1	ACN	I	Adapter current sense resistor, negative input. A 0.1-μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-μF ceramic capacitor is placed from ACN pin to GND for common-mode filtering.
2	ACP	I	Adapter current sense resistor, positive input. A 0.1-μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from ACP pin to GND for common-mode filtering.
3	$\overline{\text{ACDRV}}$	O	AC adapter to system MOSFET driver output. Connect through a 1-kΩ resistor to the gate of the ACFET P-channel power MOSFET and the reverse conduction blocking P-channel power MOSFET. The internal gate drive is asymmetrical, allowing a quick turn-off and slow turn-on, in addition to the internal break-before-make logic with respect to $\overline{\text{BATDRV}}$. If needed, an optional capacitor from gate to source of the ACFET is used to slow down the ON and OFF times.
4	CE	I	Charge-enable active-HIGH logic input. HI enables charge. LO disables charge. It has an internal 1MΩ pull-down resistor.
5	STAT1	O	Open-drain charge status pin to indicate various charger operation (See Table 3)
6	TS	I	Temperature qualification voltage input for battery pack negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to GND. (See Figure 17)
7	TTC	I	Fast-charge safety timer and termination control. Connect a capacitor from this node to GND to set the timer. When this input is LOW, the fast-charge timer and termination are disabled. When this input is HIGH, the fast-charge timer is disabled but termination is allowed.
8	$\overline{\text{PG}}$	O	Open-drain power-good status output. Active LOW when IC has a valid VCC (not in UVLO or ACOV or SLEEP mode). Active HIGH when IC has an invalid VCC. $\overline{\text{PG}}$can be used to drive a LED or communicate with a host processor.
9	STAT2	O	Open-drain charge status pin to indicate various charger operation (See Table 3)
10	VREF	O	3.3V regulated voltage output. Place a 1-μF ceramic capacitor from VREF to GND pin close to the IC. This voltage could be used for programming of voltage and current regulation and for programming the TS threshold.
11	ISET1	I	Fast Charge current set input. The voltage of ISET1 pin programs the fast charge current regulation set-point. To avoid early termination during V_{T1} and V_{T2} range, fast charge current need to be bigger than 2 times of termination current.
12	VFB	I	Output voltage analog feedback adjustment. Connect the output of a resistive voltage divider from the battery terminals to this node to adjust the output battery regulation voltage.
13	SRN	I/O	Charge current sense resistor, negative input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-μF ceramic capacitor is placed from SRN pin to GND for common-mode filtering.
14	SRP	I/O	Charge current sense resistor, positive input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from SRP pin to GND for common-mode filtering.
15	ISET2	I	Pre-charge and termination current set input. The voltage of ISET2 pin programs the pre-charge current regulation set-point and termination current trigger point.
16	ACSET	I	Adapter current set input. The voltage of ACSET pin programs the input current regulation set-point during Dynamic Power Management (DPM)
17	GND		Low-current sensitive analog/digital ground. On PCB layout, connect with PowerPad underneath the IC.
18	REGN	O	PWM low side driver positive 6V supply output. Connect a 1-μF ceramic capacitor from REGN to GND pin, close to the IC. Use for low side driver and high-side driver bootstrap voltage by connecting a small signal Schottky diode from REGN to BTST.
19	LODRV	O	PWM low side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
20	PH	I	PWM high side driver negative supply. Connect to the Phase switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1-μF bootstrap capacitor from PH to BTST.
21	HIDRV	O	PWM high side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
22	BTST	I	PWM high side driver positive supply. Connect to the Phase switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1-μF bootstrap capacitor from SW to BTST.
23	$\overline{\text{BATDRV}}$	O	Battery to system MOSFET driver output. Gate drive for the battery to system load BAT PMOS power FET to isolate the system from the battery to prevent current flow from the system to the battery, while allowing a low impedance path from battery to system. Connect this pin through a 1-kΩ resistor to the gate of the input BAT P-channel MOSFET. Connect the source of the FET to the system load voltage node. Connect the drain of the FET to the battery pack positive terminal. The internal gate drive is asymmetrical to allow a quick turn-off and slow turn-on, in addition to the internal break-before-make logic with respect to $\overline{\text{ACDRV}}$. If needed, an optional capacitor from gate to source of the BATFET is used to slow down the ON and OFF times.
24	VCC	I	IC power positive supply. Connect through a 10-Ω to the common-source (diode-OR) point: source of high-side P-channel MOSFET and source of reverse-blocking power P-channel MOSFET. Place a 1-μF ceramic capacitor from VCC to GND pin close to the IC.
	PowerPAD		Exposed pad beneath the IC. Always solder PowerPAD to the board, and have vias on the PowerPAD plane star-connecting to GND and ground plane for high-current power converter. It also serves as a thermal pad to dissipate the heat.

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BLOCK DIAGRAM

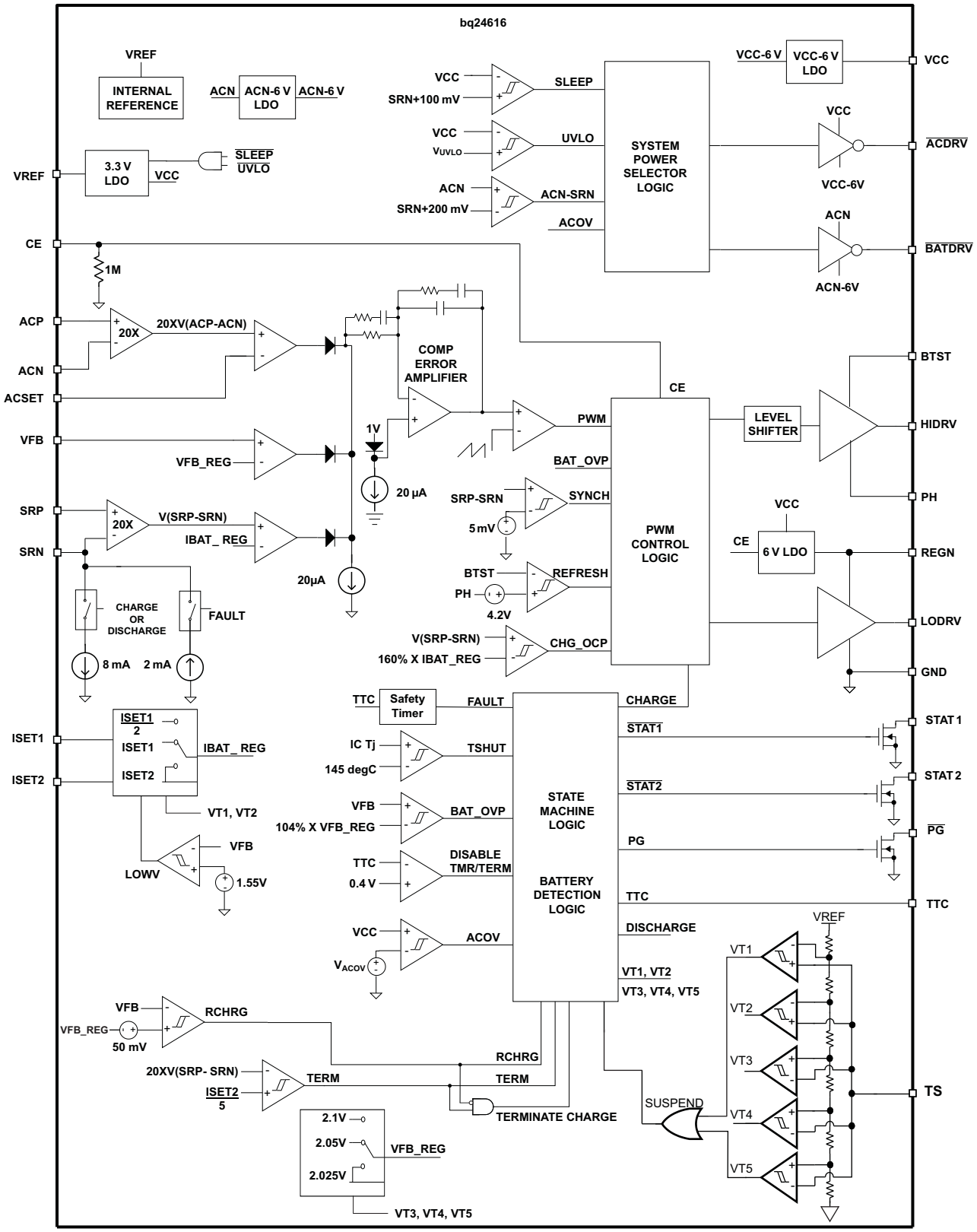

Figure 13. Functional Block Diagram for bq24616

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OPERATIONAL FLOWCHART

Figure 14. Operational Flowchart

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DETAILED DESCRIPTION

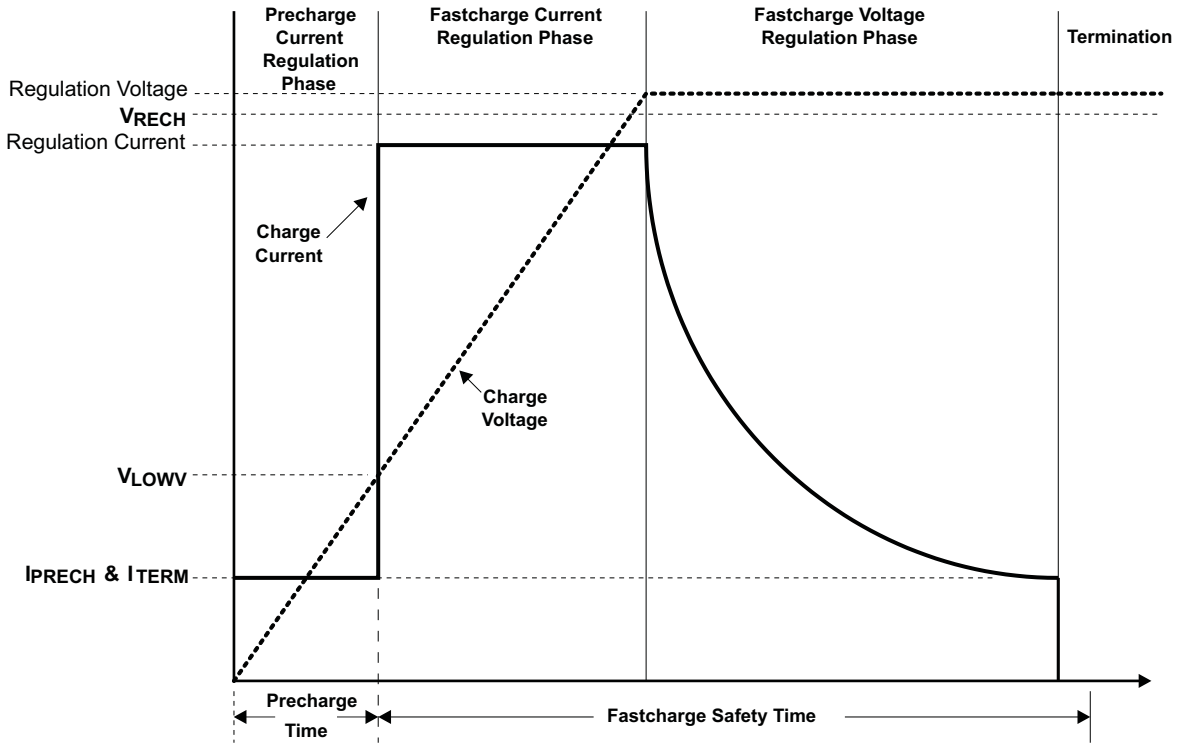

Figure 15. Typical Charging Profile

Battery Voltage Regulation

The bq24616 uses a high accuracy voltage bandgap and regulator for the high charging voltage accuracy. The charge voltage is programmed via a resistor divider from the battery to ground, with the midpoint tied to the VFB pin. The voltage at the VFB pin is regulated to 2.1V in 0 – 45°C range, giving the following equation for the regulation voltage:

$$V_{BAT} = 2.1\ V \times \left[1 + \frac{R2}{R1}\right], \quad (1)$$

where R2 is connected from VFB to the battery and R1 is connected from VFB to GND.

Battery Current Regulation

The ISET1 input sets the maximum fast charging current in 10 – 60°C range. Battery charge current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 100mV. Thus, for a 10mΩ sense resistor, the maximum charging current is 10A. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET1}}{20 \times R_{SR}} \quad (2)$$

V_{ISET1}, the input voltage range of ISET1, is between 0V and 2V. The SRP and SRN pins are used to sense voltage across R_{SR} with default value of 10mΩ; however, resistors of other values can also be used. A larger sense resistor will give a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

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Input Adapter Current Regulation

The total input from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the battery charger reduces the charging current when the input current exceeds the input current limit set by ACSET. The current capability of the AC adaptor can be lowered, reducing system cost.

Similar to setting battery regulation current, adaptor current is sensed by resistor R_{AC} connected between ACP and ACN. Its maximum value is set by ACSET using Equation 3:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}} \quad (3)$$

V_{ACSET}, the input voltage range of ACSET, is between 0 and 2V. The ACP and ACN pins are used to sense voltage across R_{AC} with default value of 10mΩ; however, resistors of other values can also be used. A larger sense resistor will give a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

Precharge

On power-up, if the battery voltage is below the V_{LOWV} threshold, the bq24616 applies the precharge current to the battery. This feature is intended to revive deeply discharged cells. If the V_{LOWV} threshold is not reached within 30 minutes of initiating precharge, the charger turns off and a FAULT is indicated on the status pins.

The precharge current ($I_{PRECHARGE}$) is determined by the voltage on the ISET2 pin (V_{ISET2}) according to Equation 4.

$$I_{PRECHARGE} = \frac{V_{ISET2}}{100 \times R_{SR}} \quad (4)$$

Charge Termination, Recharge, and Safety Timer

The bq24616 monitors the charging current during the voltage regulation phase. When V_{TTC} is valid, termination is detected while the voltage on the VFB pin is higher than the V_{RECH} threshold AND the charge current is less than the I_{TERM} threshold, as calculated in Equation 5:

$$I_{TERM} = \frac{V_{ISET2}}{100 \times R_{SR}} \quad (5)$$

V_{ISET2}, the input voltage of ISET2, is between 0 and 2V. The minimum precharge/termination current is clamped to be around 125mA with default 10mΩ sensing resistor. As a safety backup, the bq24616 also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TTC pin and GND, and is given by Equation 6

$$t_{CHARGE} = C_{TTC} \times K_{TTC} \quad (6)$$

where C_{TTC} (range from 0.01µF to 0.11 µF to give 1-10hr safety time) is the capacitor connected from TTC pin to GND, and K_{TTC} is the constant multiplier (5.6min/nF).

A new charge cycle is initiated and fast-charge safety timer is reset when one of the following conditions occur:

- The battery voltage falls below the recharge threshold
- A power-on-reset (POR) event occurs
- CE is toggled

The TTC pin may be taken LOW to disable termination and to disable the safety timer. If TTC is pulled to VREF, the bq24616 will continue to allow termination but disable safety timer. TTC taken low will reset the safety timer. When ACOV, VCCLOWV and SLEEP mode resume normal, the safety timer will also be reset.

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Power Up

The bq24616 uses a SLEEP comparator to determine the source of power on the VCC pin, since VCC can be supplied either from the battery or the adapter. If the VCC voltage is greater than the SRN voltage, bq24616 will enable the ACFET and disable BATFET. If all other conditions are met for charging, bq24616 will then attempt to charge the battery (See *Enabling and Disabling Charging*). If the SRN voltage is greater than VCC, indicating that the battery is the power source, bq24616 enables the BATFET, and enters a low quiescent current (<15μA) SLEEP mode to minimize current drain from the battery.

If VCC is below the UVLO threshold, the device is disabled, ACFET turns off and BATFET turns on.

Enable and Disable Charging

The following conditions have to be valid before charge is enabled:

- CE is HIGH
- The device is not in UVCCLOWV mode
- The device is not in SLEEP mode
- The VCC voltage is lower than the AC over-voltage threshold (VCC < V_{ACOV})
- 30ms delay is complete after initial power-up
- The REGN LDO and VREF LDO voltages are at the correct levels
- Thermal Shut (TSHUT) is not valid
- TS fault is not detected

One of the following conditions will stop on-going charging:

- CE is LOW;
- Adapter is removed, causing the device to enter VCCLOWV or SLEEP mode;
- Adapter is over voltage;
- The REGN or VREF LDOs are overloaded;
- TSHUT IC temperature threshold is reached (145°C on rising-edge with 15°C hysteresis).
- TS voltage goes out of range indicating the battery temperature is too hot or too cold.
- TTC safety timer out

System Power Selector

The bq24616 automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or during SLEEP mode. The battery is disconnected from the system and then the adapter is connected to the system 30ms after exiting SLEEP. An automatic break-before-make logic prevents shoot-through currents when the selectors switch.

The $\overline{\text{ACDRV}}$ is used to drive a pair of back-to-back p-channel power MOSFETs between adapter and ACP with sources connected together and to VCC. The FET connected to adapter prevents reverse discharge from the battery to the adapter when turned off. The p-channel FET with the drain connected to the adapter input provides reverse battery discharge protection when off; and also minimizes system power dissipation, with its low-R_{DSON}, compared to a Schottky diode. The other p-channel FET connected to ACP separates battery from adapter, and provides a limited dI/dt when connecting the adapter to the system by controlling the FET turn-on time. The $\overline{\text{BATDRV}}$ controls a p-channel power MOSFET placed between BAT and system.

When adapter is not detected, the $\overline{\text{ACDRV}}$ is pulled to VCC to keep ACFET off, disconnecting the adapter from system. $\overline{\text{BATDRV}}$ stays at ACN-6V to connect battery to system.

Approximately 30ms after the device comes out of SLEEP mode, the system begins to switch from battery to adapter. The break-before-make logic keeps both ACFET and BATFET off for 10us before ACFET turns on. This prevents shoot-through current or any large discharging current from going into the battery. The $\overline{\text{BATDRV}}$ is pulled up to ACN and the $\overline{\text{ACDRV}}$ pin is set to VCC-6V by an internal regulator to turn on p-channel ACFET, connecting the adapter to the system.

When the adapter is removed, the system waits until VCC drops back to within 200mV above SRN to switch from adapter back to battery. The break-before-make logic still keeps 10μs dead time. The $\overline{\text{ACDRV}}$ is pulled up to VCC and the $\overline{\text{BATDRV}}$ pin is set to ACN-6V by an internal regulator to turn on p-channel BATFET, connecting the battery to the system.

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Asymmetrical gate drive (fast turn-off and slow turn-on) for the $\overline{ACDRV}$ and $\overline{BATDRV}$ drivers provides fast turn-off and slow turn-on of the ACFET and BATFET to help the break-before-make logic and to allow a soft-start at turn-on of either FET. The soft-start time can be further increased, by putting a capacitor from gate to source of the p-channel power MOSFETs.

Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger goes into fast-charge to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts around 1.6ms, for a typical rise time of 12.8ms. No external components are needed for this function.

Converter Operation

The synchronous buck PWM converter uses a fixed frequency voltage mode with feed-forward control scheme. A type III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter is selected to give a resonant frequency of 12kHz–17kHz for bq24616, where resonant frequency, f_o, is given by:

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} \quad (7)$$

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the duty-cycle of the converter. The ramp height is 7% of the input adapter voltage making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 300mV in order to allow zero percent duty-cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.5% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4.2V for more than 3 cycles, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-PH) voltage is detected to fall low again due to leakage current discharging the BTST capacitor below the 4.2 V, and the reset pulse is reissued.

The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. Also see *Application Information* for how to select inductor, capacitor and MOSFET.

Synchronous and Non-Synchronous Operation

The charger operates in synchronous mode when the SRP-SRN voltage is above 5mV (0.5A inductor current for a 10mΩ sense resistor). During synchronous mode, the internal gate drive logic ensures there is break-before-make complimentary switching to prevent shoot-through currents. During the 30ns dead time where both FETs are off, the body-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn-on keeps the power dissipation low, and allows safely charging at high currents. During synchronous mode the inductor current is always flowing and converter operates in continuous conduction mode (CCM), creating a fixed two-pole system.

The charger operates in non-synchronous mode when the SRP-SRN voltage is below 5mV (0.5A inductor current for a 10mΩ sense resistor). The charger is forced into non-synchronous mode when battery voltage is lower than 2V or when the average SRP-SRN voltage is lower than 1.25mV.

During non-synchronous operation, the body-diode of lower-side MOSFET can conduct the positive inductor current after the high-side n-channel power MOSFET turns off. When the load current decreases and the inductor current drops to zero, the body diode will be naturally turned off and the inductor current will become discontinuous. This mode is called Discontinuous Conduction Mode (DCM). During DCM, the low-side n-channel power MOSFET will turn-on for around 80ns when the bootstrap capacitor voltage drops below 4.2V, then the low-side power MOSFET will turn-off and stay off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The 80ns low-side MOSFET on-time is required to ensure the bootstrap capacitor is

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always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The 80ns low-side pulse pulls the PH node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring.

At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance. Whenever the converter goes into zero percent duty-cycle, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (only 80ns recharge pulse) either, and there is almost no discharge from the battery.

During the DCM mode the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage.

Cycle-by-Cycle Charge Under Current Protection

If the SRP-SRN voltage decreases below 5mV (The charger is also forced into non-synchronous mode when the average SRP-SRN voltage is lower than 1.25mV), the low side FET will be turned off for the remainder of the switching cycle to prevent negative inductor current. During DCM, the low-side FET will only turn on for at around 80ns when the bootstrap capacitor voltage drops below 4.2V to provide refresh charge for the bootstrap capacitor. This is important to prevent negative inductor current from causing a boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors and lead to an over-voltage stress on the VCC node and potentially cause damage to the system.

Input Over Voltage Protection (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. Once the adapter voltage reaches the ACOV threshold, charge is disabled and the system is switched to battery instead of adapter.

Input Under Voltage Lock Out (UVLO)

The system must have a minimum VCC voltage to allow proper operation. This VCC voltage could come from either input adapter or battery, since a conduction path exists from the battery to VCC through the high side NMOS body diode. When VCC is below the UVLO threshold, all circuits on the IC are disabled, and the gate drive bias to ACFET and BATFET are disabled. ACFET is OFF and BATEFET is ON.

Battery Over-Voltage Protection

The converter will not allow the high-side FET to turn-on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. An 8mA current sink from SRP/SRN to GND is on only during charge and allows discharging the stored output inductor energy that is transferred to the output capacitors. BATOVP will also suspend the safety timer.

Cycle-by-Cycle Charge Over-Current Protection

The charger has a secondary cycle-to-cycle over-current protection. It monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when the over-current is detected, and automatically resumes when the current falls below the over-current threshold.

Thermal Shutdown Protection

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 145°C. The charger stays off until the junction temperature falls below 130°C, then the charger will soft-start again if all other enable charge conditions are valid. Thermal shutdown will also suspend the safety timer.

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Temperature Qualification AND JEITA Guideline

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and GND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the voltage on TS pin must be within the V_{T1} to V_{T5} thresholds. If V_{TS} is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{T1} to V_{T5} range. During the charge cycle the battery temperature must be within the V_{T1} to V_{T5} thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{T1} to V_{T5} range. The controller suspends charge by turning off the PWM charge FETs. If V_{TS} is within the range of V_{T1} and V_{T2}, charge voltage regulation on V_{FB} pin is 2.1 V and the charge current is reduced to $I_{CHARGE}/2$ (To avoid early termination during V_{T1} and V_{T2} range, fast charge current need to be bigger than 2 times of termination current); if V_{TS} is within the range of V_{T2} and V_{T3}, the charge voltage regulation on V_{FB} pin is 2.1 V; if V_{TS} is within V_{T3} and V_{T4}, the charge voltage regulation on V_{FB} pin is reduced back to 2.05 V; and if V_{TS} is within V_{T4} and V_{T5}, the charge voltage regulation on V_{FB} pin is further reduced to 2.025 V. Figure 16 below summarizes the operation. Refer to Li-ion battery-charger solutions for JEITA compliance, SLYT365

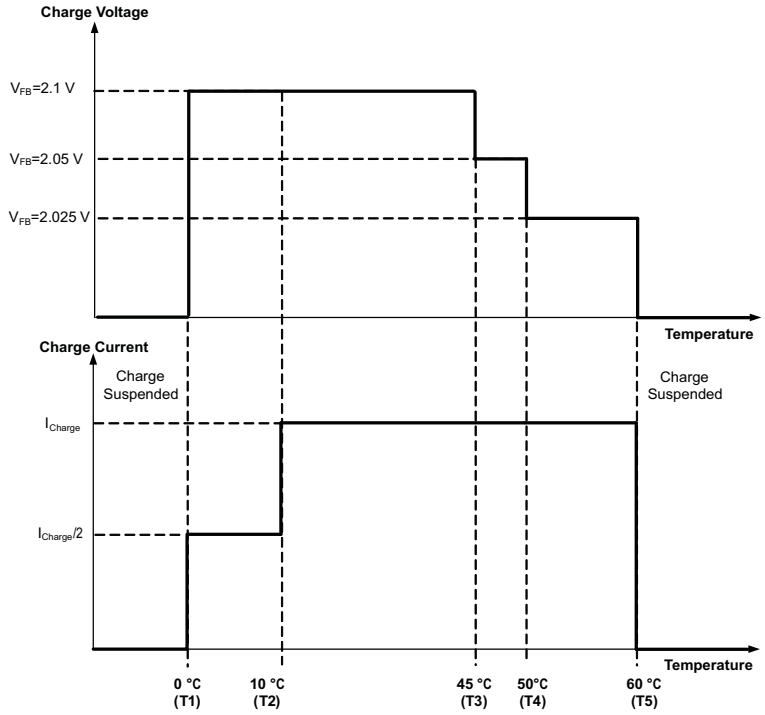

Figure 16. Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 1, the value RT1 and RT2 can be determined by using the following equations:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{VT1} - 1\right)} \quad (8)$$

$$RT1 = \frac{\frac{V_{VREF}}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (9)$$

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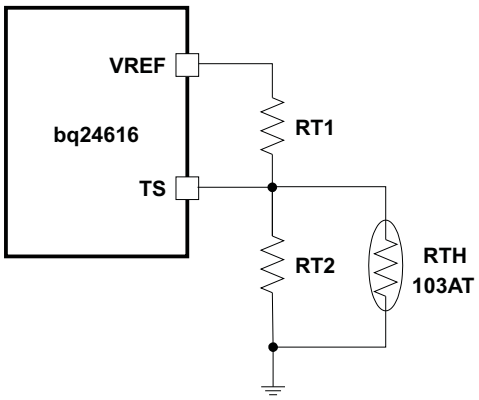

Figure 17. TS Resistor Network

For example, 103AT NTC thermistors are used to monitor the battery pack temperature. Select T1 = 0ºC for COLD and T5 = 60ºC for HOT, then we get R_{T2} = 6.8kΩ and R_{T1} = 2.2kΩ as in the design tool. A small RC filter is suggested to use for system-level ESD protection.

Timer Fault Recovery

The bq24616 provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: The battery voltage is above the recharge threshold and a timeout fault occurs.

Recovery Method: The timer fault will clear when the battery voltage falls below the recharge threshold, and battery detection will begin. Taking CE low or a POR condition will also clear the fault.

Condition 2: The battery voltage is below the recharge threshold and a timeout fault occurs.

Recovery Method: Under this scenario, the bq24616 applies the I_{FAULT} current to the battery. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the bq24616 disables the fault current and executes the recovery method described in Condition 1. Taking CE low or a POR condition will also clear the fault.

$\overline{PG}$ Output

The open drain $\overline{PG}$(power good) output indicates whether the VCC voltage is valid or not. The open drain FET turns on whenever bq24616 has a valid VCC input (not in UVLO or ACOV or SLEEP mode). The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor.

CE (Charge Enable)

The CE digital input is used to disable or enable the charge process. A high-level signal on this pin enables charge, provided all the other conditions for charge are met (see *Enabling and Disabling Charge*). A high to low transition on this pin also resets all timers and fault conditions. There is an internal 1MΩ pulldown resistor on the CE pin, so if CE is floated the charge will not turn on.

Inductor, Capacitor, and Sense Resistor Selection Guidelines

The bq24616 provides internal loop compensation. With this scheme, best stability occurs when the LC resonant frequency, f_o, is approximately 12kHz–17kHz for bq24616.

The following table provides a summary of typical LC components for various charge currents:

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Table 2. Typical Inductor, Capacitor, and Sense Resistor Values as a Function of Charge Current for bq24616 (600 kHz Switching Frequency)

CHARGE CURRENT	2A	4A	6A	8A	10A
Output Inductor Lo	6.8 μH	6.8 μH	4.7 μH	3.3 μH	3.3 μH
Output Capacitor Co	20 μF	20 μF	30 μF	40 μF	40 μF
Sense Resistor	10 mΩ	10 mΩ	10 mΩ	10 mΩ	10 mΩ

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in the table below. These status pins can be used to drive LEDs or communicate with the host processor. Note that OFF indicates that the open-drain transistor is turned off.

Table 3. STAT Pin Definition for bq24616

CHARGE STATE	STAT1	STAT2
Charge in progress	ON	OFF
Charge complete	OFF	ON
Charge suspend, timer fault, AC over-voltage, sleep mode, battery absent	OFF	OFF

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Battery Detection

For applications with removable battery packs, bq24616 provides a battery absent detection scheme to reliably detect insertion or removal of battery packs.

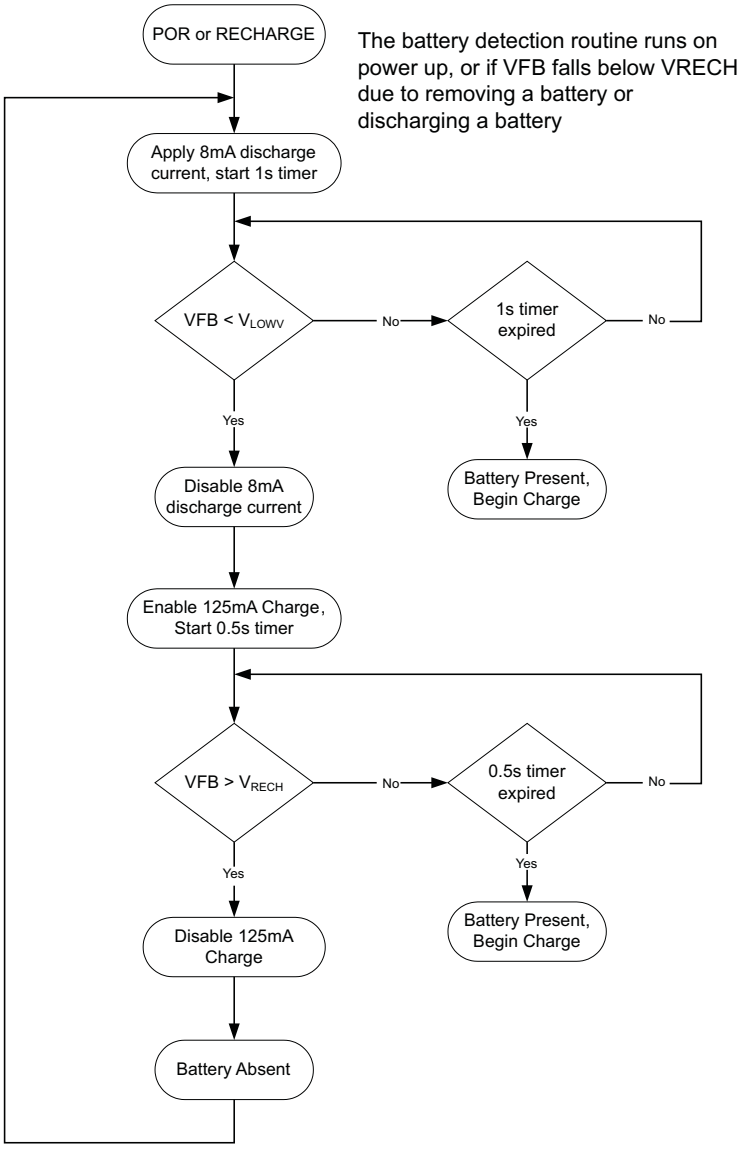

Figure 18. Battery Detection Flowchart

Once the device has powered up, an 8mA discharge current will be applied to the SRN terminal. If the battery voltage falls below the LOWV threshold within 1 second, the discharge source is turned off, and the charger is turned on at low charge current (125mA). If the battery voltage gets up above the recharge threshold within 500ms, there is no battery present and the cycle restarts. If either the 500ms or 1 second timer time out before the respective thresholds are hit, a battery is detected and a charge cycle is initiated.

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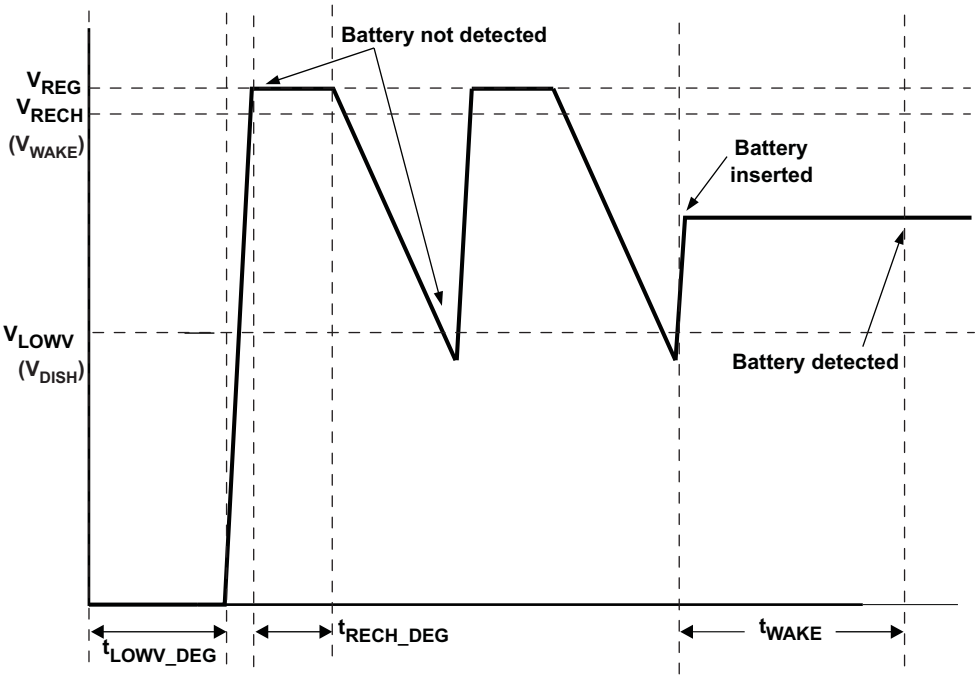

Figure 19. Battery Detect Timing Diagram

Care must be taken that the total output capacitance at the battery node is not so large that the discharge current source cannot pull the voltage below the LOWV threshold during the 1 second discharge time. The maximum output capacitance can be calculated as follows:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{0.5 \times \left[1 + \frac{R_2}{R_1}\right]} \quad (10)$$

Where C_{MAX} is the maximum output capacitance, I_{DISCH} is the discharge current, t_{DISCH} is the discharge time, and R_2 and R_1 are the voltage feedback resistors from the battery to the VFB pin. The 0.5 factor is the difference between the RECHARGE and the LOWV thresholds at the VFB pin.

Example

For a 3-cell Li+ charger, with R2 = 500k, R1 = 100k (giving 12.6V for voltage regulation), I_{DISCH} = 8mA, t_{DISCH} = 1 second,

$$C_{MAX} = \frac{8mA \times 1sec}{0.5 \times \left[1 + \frac{500k}{100k}\right]} = 2.7\ mF \quad (11)$$

Based on these calculations, no more than 2.7 mF should be allowed on the battery node for proper operation of the battery detection circuit.

Component List for Typical System Circuit of Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	3	P-channel MOSFET, –30 V,–35 A, PowerPAK 1212-8, Vishay-Siliconix, Si7617DN
Q4, Q5	2	N-channel MOSFET, 30 V, 12 A, PowerPAK 1212-8, Vishay-Siliconix, Sis412DN
D1	1	Diode, Dual Schottky, 30 V, 200 mA, SOT23, Fairchild, BAT54C
D2, D3, D4	3	LED Diode, Green, 2.1V, 20mA, LTST-C190GKT
R_{AC}, R_{SR}	2	Sense Resistor, 10 mΩ, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 6.8 µH, 5.5A, Vishay-Dale IHLP2525CZ

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PART DESIGNATOR	QTY	DESCRIPTION
C8, C9, C12, C13	4	Capacitor, Ceramic, 10 µF, 35 V, 20%, X7R
C4, C5	2	Capacitor, Ceramic, 1 µF, 16 V, 10%, X7R
C1, C3, C6, C11	4	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R
C2, C10	2	Capacitor, Ceramic, 0.1 µF, 50 V, 10%, X7R
C7	1	Capacitor, Ceramic, 1 µF, 50 V, 10%, X7R
C14, C15 (Optional)	2	Capacitor, Ceramic, 0.1 µF, 50 V, 10%, X7R
C16	1	Capacitor, Ceramic, 2.2 µF, 35V, 10%, X7R
C_{ff}	1	Capacitor, Ceramic, 22 pF, 25V, 10%, X7R
C_{TTC}	1	Capacitor, Ceramic, 0.056 µF, 16V, 5%, X7R
R1, R3, R5, R7	4	Resistor, Chip, 100 kΩ, 1/16W, 0.5%
R2	1	Resistor, Chip, 500 kΩ, 1/16W, 0.5%
R4	1	Resistor, Chip, 32.4 kΩ, 1/16W, 0.5%
R6	1	Resistor, Chip, 10 kΩ, 1/16W, 0.5%
R8	1	Resistor, Chip, 22.1 kΩ, 1/16W, 0.5%
R9	1	Resistor, Chip, 2.2 kΩ, 1/16W, 1%
R10	1	Resistor, Chip, 6.8 kΩ, 1/16W, 1%
R11, R12, R13, R18, R19	5	Resistor, Chip, 10 kΩ, 1/16W, 5%
R14, R15 (optional)	2	Resistor, Chip, 100 kΩ, 1/16W, 5%
R16	1	Resistor, Chip, 100 Ω, 1/16W, 5%
R17	1	Resistor, Chip, 10 Ω, 1/4W, 5%
R20	1	Resistor, Chip, 2 Ω, 1W, 5%

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APPLICATION INFORMATION

Inductor Selection

The bq24616 has 600kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (12)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D=V_{OUT}/V_{IN}$), switching frequency (f_s) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (13)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9V to 12.6V for 3-cell battery pack. For 20V adapter voltage, 10V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12V to 16.8V, and 12V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

The bq24616 has cycle-by-cycle charge under current protection (UCP) by monitoring charging current sensing resistor to prevent negative inductor current. The Typical UCP threshold is 5mV falling edge corresponding to 0.5A falling edge for a 10mΩ charging current sensing resistor.

Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (14)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 20V input voltage. 10-20µF capacitance is suggested for typical of 3-4A charging current.

Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (15)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_o = \frac{V_{OUT}}{8LCf_s^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (16)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The bq24616 has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 12 kHz and 17 kHz. The preferred ceramic capacitor is 25V or higher rating, X7R or X5R for 4-cell application.

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Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6V of gate drive voltage. 30V or higher voltage rating MOSFETs are preferred for 20V input voltage and 40V or higher rating MOSFETs are perfered for 20-28V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD} \qquad FOM_{bottom} = R_{DS(on)} \times Q_G \tag{17}$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance $R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (F), turn on time (t_{on}) and turn off time (t_{toff}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times \left(t_{on} + t_{off}\right) \times f_S \tag{18}$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100ºC junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, t_{off} = \frac{Q_{SW}}{I_{off}} \tag{19}$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and Ioff is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \tag{20}$$

Gate driving current total can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (Ron) and turn-off gate resistance R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, I_{off} = \frac{V_{plt}}{R_{off}} \tag{21}$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \tag{22}$$

If the SRP-SRN voltage decreases below 5mV (The charger is also forced into non-synchronous mode when the average SRP-SRN voltage is lower than 1.25mV), the low side FET will be turned off for the remainder of the switching cycle to prevent negative inductor current.

As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The maximum charging current in non-synchronous mode can be up to 0.9A (0.5A typ) for a 10mΩ charging current sensing resistor considering IC tolerance. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

MOSFET gate driver power loss contributes to the dominant losses on controller IC, when the buck converter is switching. Choosing the MOSFET with a small Q_{g_total} will reduce the IC power loss to avoid thermal shutdown.

$$P_{ICLoss\_driver} = V_{IN} \cdot Q_{g\_total} \cdot f_s \tag{23}$$

Where Q_{g_total} is the total gate charge for both upper and lower MOSFET at 6V V_{REGN}

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Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on VCC pin. ACP/ACN pin needs to be placed after the input ACFET in order to avoid the over-voltage stress on these pins during hot-plug-in.

There are several methods to damping or limit the over voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However these two solutions may not have low cost or small size.

A cost effective and small size solution is shown in Figure 20. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for VCC pin (it can be the body diode of input ACFET). C2 is VCC pin decoupling capacitor and it should be place to VCC pin as close as possible. The R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high voltage spike. C2 value should be less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect for hot plug-in. R1 and R2 package must be sized enough to handle inrush current power loss according to resistor manufacturer's datasheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

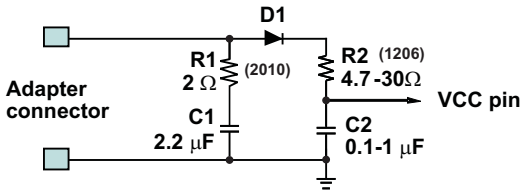

Figure 20. Input Filter

PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 21) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
3. Place inductor input terminal to switching MOSFET's output terminal as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 22 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.
5. Place output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Route analog ground separately from power ground and use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling. Connect analog ground to GND. Connect analog ground and power ground together using PowerPAD as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (PowerPAD should tie to analog ground in this case). A star-connection

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under PowerPAD is highly recommended.

8. It is critical that the exposed PowerPAD on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
10. All via size and number should be enough for a given current path.

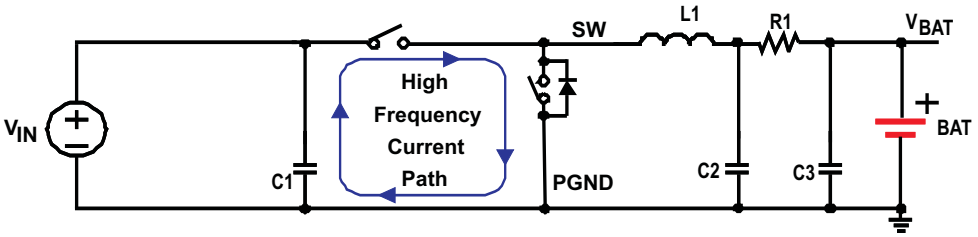

Figure 21. High Frequency Current Path

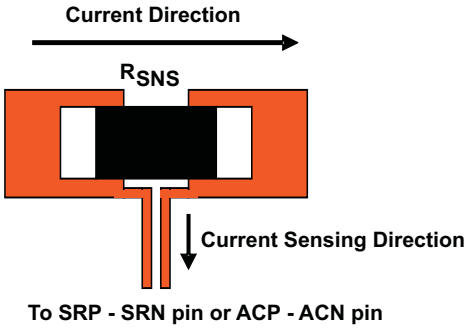

Figure 22. Sensing Resistor PCB Layout

Refer to the EVM design (SLUU396) for the recommended component placement with trace and via locations.

For the QFN information, refer to SCBA017 and SLUA271.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
BQ24616RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
BQ24616RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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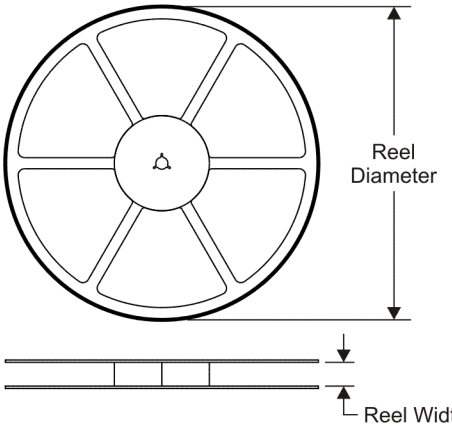
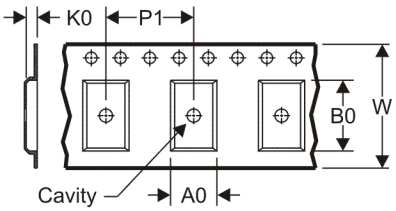
TAPE AND REEL INFORMATION

REEL DIMENSIONS

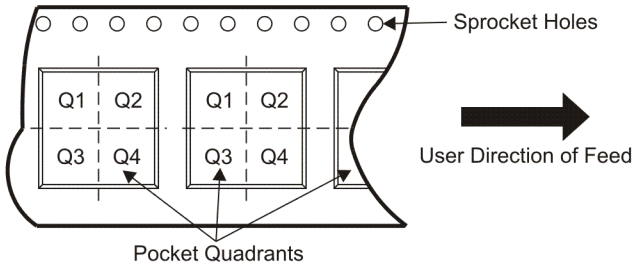


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24616RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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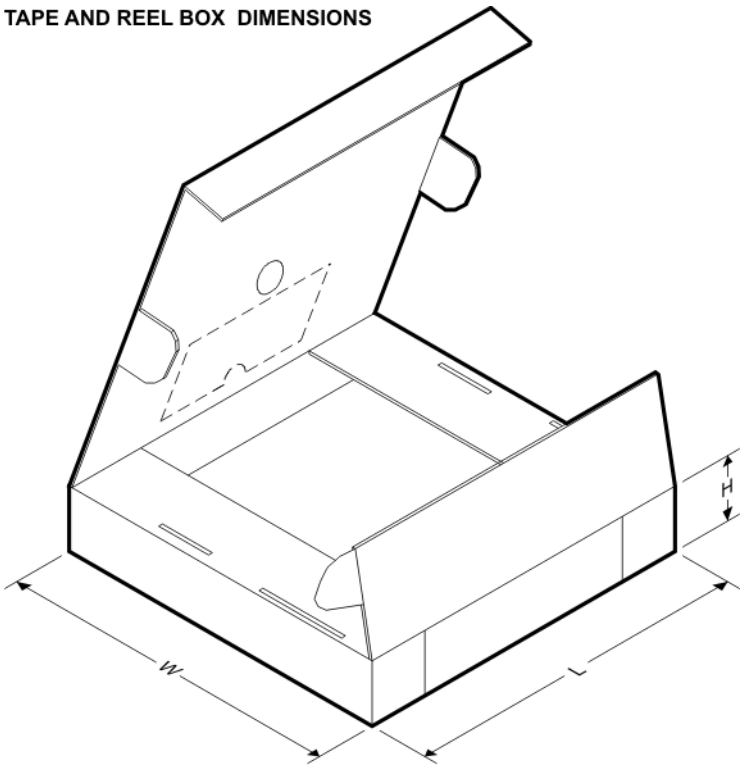
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24616RGET	VQFN	RGE	24	250	190.5	212.7	31.8

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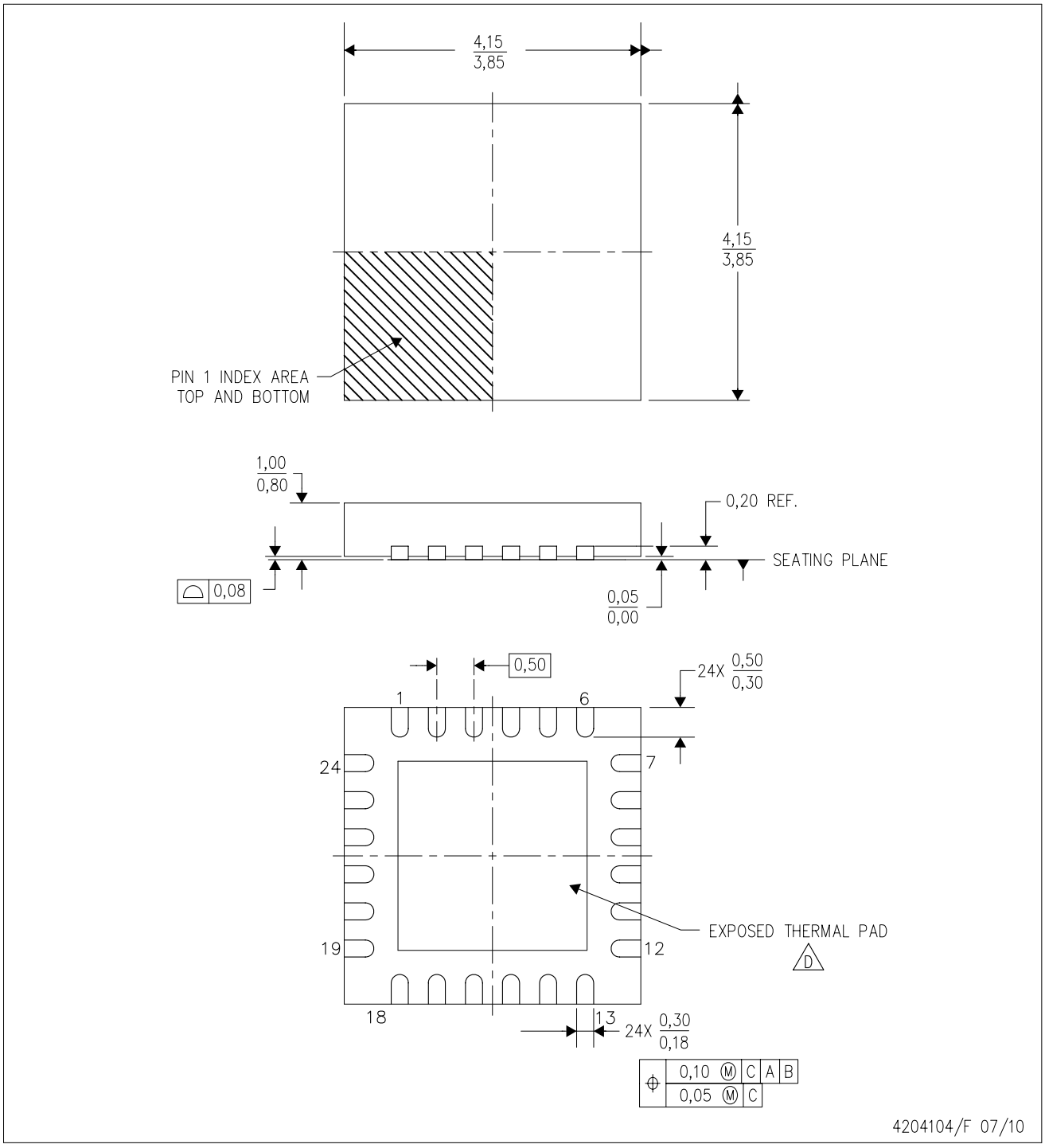
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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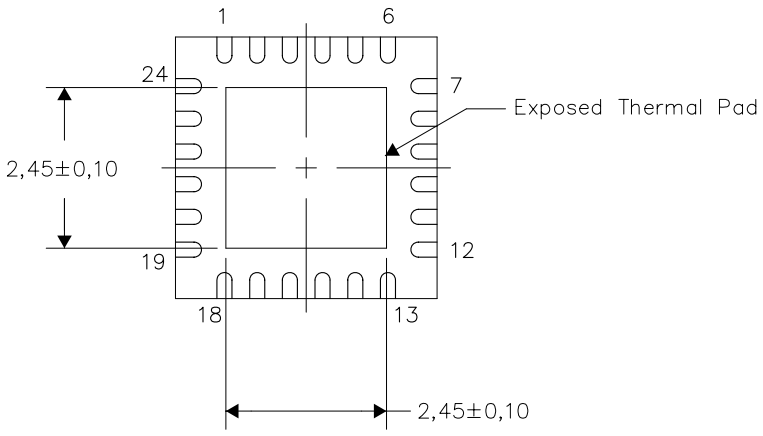
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206344–3/V 11/10

NOTES: A. All linear dimensions are in millimeters

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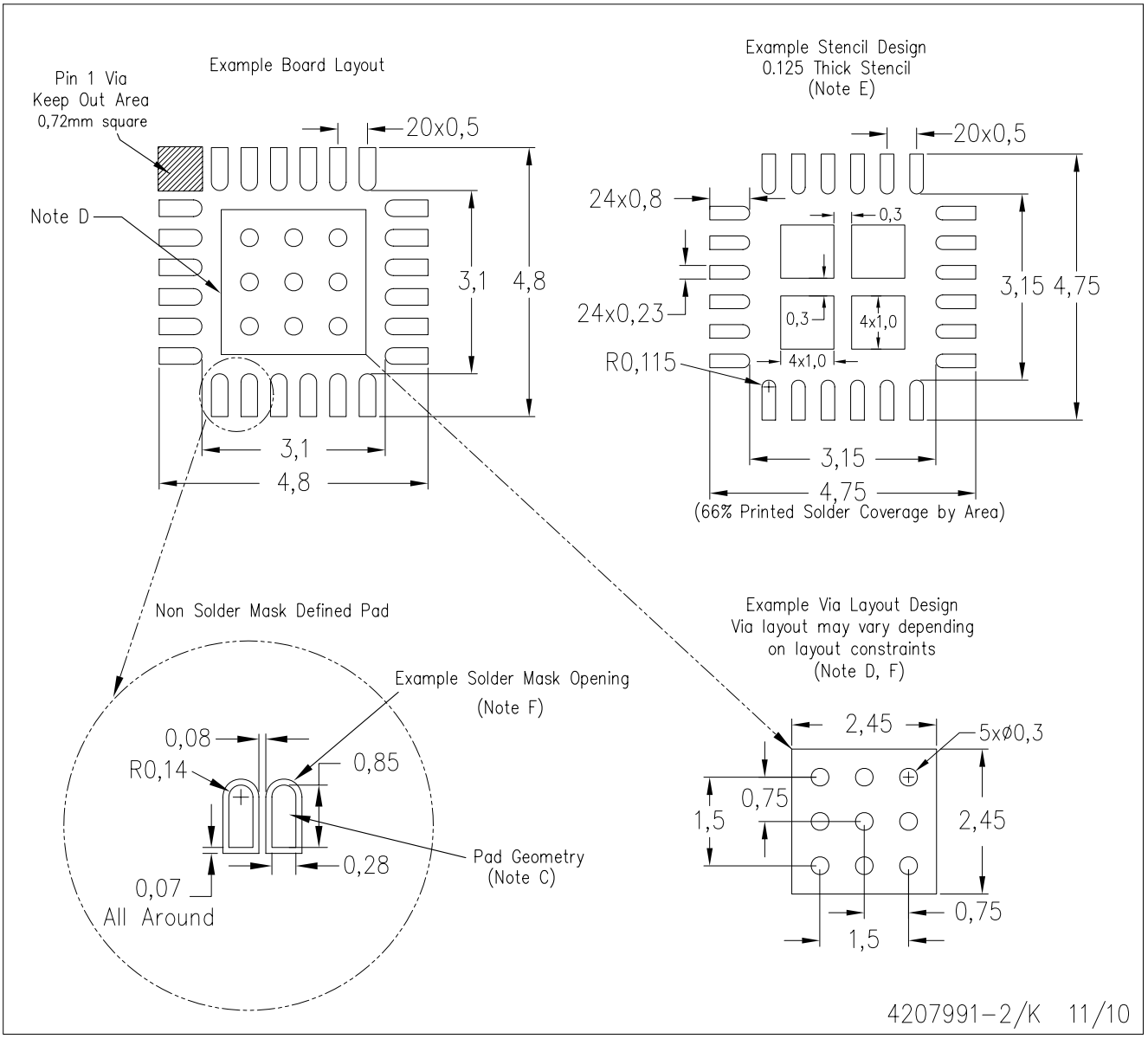
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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