LMH2191

Dual Channel 52 MHz Clock Tree Driver

General Description

The LMH2191 is a dual-channel clock tree driver that supplies a digital system clock to peripherals in mobile handsets or other applications. It provides a solution to clocking issues such as limited drive capability for fanout or longer traces. It also provides protection of the master clock from varying loads and frequency pulling effects, isolation from noisy modules, and crosstalk isolation. It has very low phase noise which enables it to drive sensitive modules such as Wireless LAN and Bluetooth.

The LMH2191 can be clocked up to 52 MHz and has an independent clock request pin for each clock output which allows the peripheral to control the clock. It features an integrated LDO which provides an ultra low-noise voltage supply with 10 mA external load current which can be used to supply the TCXO or other clock source. The LMH2191 dual clock distributor is offered in a tiny 1.615 mm x 1.070 mm 8-bump micro SMD package. Its small size and low supply current make it ideal for portable applications.

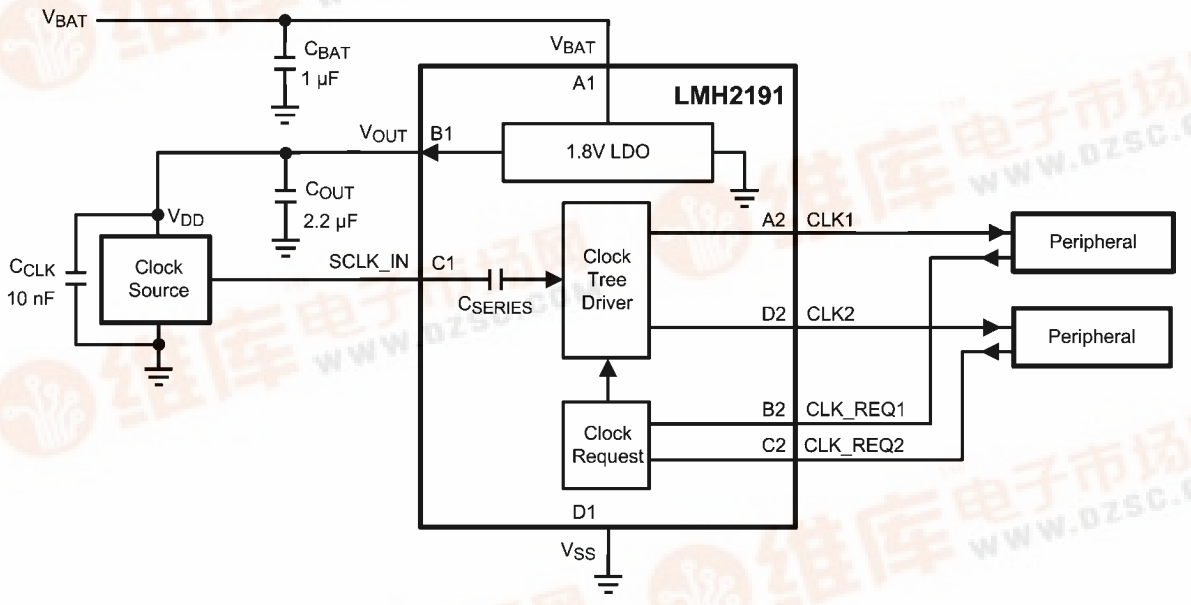
Features

- One input clock, two output clocks
- 1.8V square wave clock outputs
- Inverted clock outputs
- Independent clock requests
- High isolation of supply noise to clock input
- High output-to-output isolation
- Integrated 1.8V Low-Dropout Regulator
  - — Low output-noise voltage
  - — 10 mA load current
- EMI filtering
- Ultra low standby current
- V_{BAT} range = 2.5V to 5.5V
- micro SMD 8-Bump Package

Applications

- Mobile handsets
- Portable Equipment

Typical Application



Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{BAT} - V_{SS}	-0.3V to 6V
LVCMOS port IO voltage	-0.3V to (V_{OUT} + 0.3V)
ESD Tolerance (*Note 2*)	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
Output Short Circuit Duration (*Note 4*)	
LDO	infinite
Clock Output	infinite

For Soldering Information see:
http://www.national.com/ms/MS/MS-SOLDERING.pdf

Storage Temperature Range	−65°C to 150°C
Junction Temperature (*Note 3*)	150°C

Operating Ratings (*Note 1*)

Supply Voltage (V_{BAT} - V_{SS})	2.5V to 5.5V
Input Clock, SCLK_IN	
Frequency	10 MHz to 52 MHz
Duty Cycle	45% to 55%
Temperature Range	-40°C to +85°C
Package Thermal Resistance θ_{JA} (*Note 3*)	Board specification: 4LCELLPHONE
Package TMP08	153 °C/W

3.5 V Electrical Characteristics (*Note 5*)

Unless otherwise specified, all limits are guaranteed at T_J = 25°C, V_{BAT} = 3.5V, C_{BAT} = 1µF, C_{OUT} = 2.2 µF (*Note 11*), f_{SCLK_IN} = 26 MHz, I_{OUT} = 1mA, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (*Note 7*)	Typ (*Note 6*)	Max (*Note 7*)	Units
Supply Current (*Note 9*, *Note 10*)						
I_{DD}	Supply Current	Active Mode SCLK_IN = 19.2 MHz; both clock outputs toggling; C_{LOAD} CLK1/2 = 0pF; I_{OUT} = 0mA		1.4	1.65 **1.7**	mA
		Active Mode SCLK_IN = 19.2 MHz; both clock outputs toggling; C_{LOAD} for CLK1/2 = 33.5pF; I_{OUT} = 0mA		3.7	4.45 **4.50**	mA
		Active Mode SCLK_IN = 26 MHz, both clock outputs toggling, C_{LOAD} for CLK1/2 = 0pF, I_{OUT}=0mA		1.9	2.15 **2.25**	mA
		Active Mode SCLK_IN = 26 MHz, both clock outputs toggling, C_{LOAD} for CLK1/2 = 33.5 pF, I_{OUT}=0mA		5	5.80 **5.95**	mA
		In shutdown. Input clock not active. CLK_REQ1/2=Low		0.1	**1**	µA
		In shutdown. Input clock toggling. CLK_REQ1/2=Low		0.1	**1**	uA
C_{PD}	Power Dissipation Capacitance per CLK output	C_{LOAD} for CLK1,2 = 0pF, Defined with respect to V_{OUT} = 1.8V		20	23.0 **24.0**	pF
Clock Outputs (CLK1/2) *Figure 1*, *Figure 2*						
t_{PD_LH}	Propagation Delay - Low to High	50% to 50%; C_{LOAD} = 33 pF; measured on CLK1		6.1	**10.5**	ns
t_{PD_HL}	Propagation Delay - High to Low	50% to 50%; C_{LOAD} = 33 pF; measured on CLK1		6.1	**10.5**	
t_{SKEW}	Skew Between Outputs (Either Edge)	CLK1 to CLK2. 50% to 50%		1.5	**3.1**	
t_{RISE}	Rise Time (*Note 8*)	For C_L between 33.5 pF - 50 pF, 20% to 80%; typical value based on 40 pF load	**2.1**	3.7	**5.9**	ns
t_{FALL}	Fall Time (*Note 8*)	For C_L between 33.5 pF - 50 pF, 20% to 80%; typical value based on 40pF load	**2**	3.5	**5**	
CLK_DC	Output Clock Duty Cycle	For C_L between 33.5 pF - 50 pF	**42**	50	**58**	%

Symbol	Parameter	Condition		Min (*Note 7*)	Typ (*Note 6*)	Max (*Note 7*)	Units
$Jitter_{RMS}$	Additive RMS period Jitter	$f_{SCLK-IN}$= 26 MHz, BW = 100 Hz to 1MHz	CLK1		95		fs
			CLK2		110		
CLK1 Phase Noise	Additive Phase Noise	All outputs enabled at 26 MHz	f = 100 Hz		-128		dBc/Hz
			f = 1 kHz		-144		
			f = 10 kHz		-150		
			f = 100 kHz		-160		
			f = 1 MHz		-163		
		All outputs enabled at 19.2 MHz	f = 100 Hz		-127		
			f = 1 kHz		-146		
			f = 10 kHz		-153		
			f = 100 kHz		-161		
			f = 1 MHz		-163		
CLK2 Phase Noise	Additive Phase Noise	All outputs enabled at 26 MHz	f = 100 Hz		-127		
			f = 1 kHz		-142		
			f = 10 kHz		-148		
			f = 100 kHz		-160		
			f = 1 MHz		-162		
		All outputs enabled at 19.2 MHz	f = 100 Hz		-129		
			f = 1 kHz		-144		
			f = 10 kHz		-151		
			f = 100 kHz		-163		
			f = 1 MHz		-164		
V_{OH}	CLK1/2 Output Voltage High Level	I_{OH} = -2mA (equivalent output load 800Ω)		**1.6**			V
V_{OL}	CLK1/2 Output Voltage Low Level	I_{OL} = 2mA				**0.2**	
System Clock Input (SCLK_IN)							
V_{I-pp}	SCLK_IN peak- to- peak input level (*Note 8*)	For duty cycle variation < 1%		**0.6**	1	**1.8**	V
I_{IH}	Current into SCLK_IN pin (Input HIGH)	SCLK_IN = 1.8V, CLK_REQ1/2=Low			0	**0.1**	µA
I_{IL}	Current into SCLK_IN pin (Input LOW)	SCLK_IN = 0V, CLK_REQ1/2=Low		**–0.1**	0		
C_{IN}	Input Capacitance (*Note 8*)	CLK_REQ1/2=High			7.5	**13**	pF
R_{IN}	Input Resistance (*Note 8*)	CLK_REQ1/2=High see Application Note: Input Impedance			14	**20**	kΩ
Switching Characteristics: System Clock Input							
f_{SCLK_IN}	System Clock			**10**	26	**52**	MHz
CLK_DC	Input Clock Duty Cycle			45	50	55	%
Clock Request Inputs (CLK_REQ1/2)							
t_{SET}	Setup Time from CLK_REQx to SCLK_IN, to enable CLKx (*Figure 3*)			**12**	6.2		ns
V_{IH}	CLK_REQ1/2 logic HIGH input level. (clock output = ON)(*Note 15*)	V_{BAT} = 2.5V		**1.4**			V
		V_{BAT} = 3.5V		**1.4**			
		V_{BAT} = 5.5V		**1.4**			
V_{IL}	CLK_REQ1/2 logic LOW input level. (clock output = OFF)	V_{BAT} = 2.5V				**0.4**	V
		V_{BAT} = 3.5V				**0.4**	
		V_{BAT} = 5.5V				**0.4**	

Symbol	Parameter	Condition		Min (*Note 7*)	Typ (*Note 6*)	Max (*Note 7*)	Units
I_{IH}	Current into CLK_REQ pin	V_{IH} = 1.8V, 200 kΩ pull down resistor (Input HIGH)			8.5	**14**	µA
I_{IL}	Current into CLK_REQ pin	$V_{IL} = V_{SS}$, (Input LOW)		**-0.2**	0		µA
LDO							
V_{OUT}	Output Voltage	I_{OUT} = 1mA		**1.73**	1.8	**1.88**	V
I_{LOAD}	Load Current(*Note 12*)	V_{OUT} > 1.7V		0		10	mA
V_{DO}	Dropout Voltage (*Note 14*)	I_{OUT} = 10 mA Vout=1.7V			125		mV
I_{SC}	Short Circuit Current Limit				300		mA
PSRR	Power Supply Rejection Ratio	V_{BAT} ripple = 200 mV_{PP}, I_{OUT} = 10 mA	f = 100 Hz		92		dB
			f = 217.5 Hz		90		
			f = 1 kHz		78		
			f = 10 kHz		60		
			f = 100 kHz		50		
			f = 1 MHz		50		
			f = 3.25 MHz		42		
E_N	Output Noise Voltage (*Note 13*)	BW = 10 Hz to 100 kHz, CLK_REQ1/2=High, Input clock not active			18		$µV_{RMS}$
T_{SHTDWN}	Thermal Shutdown	Temperature			160		°C
		Hysteresis			20		
$ΔV_{OUT}$	Line Transient	V_{BAT} = 2.8V to 3.4V in 30 µs, I_{OUT} = 1mA		**-1**			mV
		V_{BAT} = 3.4V to 2.8V in 30 µs, I_{OUT} = 1mA				**1**	
	Load Transient	I_{OUT} = 0mA to 10 mA in 10 µs		**-15**			mV
		I_{OUT} = 10 mA to 0mA in 10 µs				**10**	
	Overshoot on Startup					**20**	mV
R_{OUT}	DC Output Resistance				5		Ω
T_{ON}	Turn on Time	From rising edge of CLK_REQ1 to 95% of V_{OUT}(NOM)			200	260 **350**	µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human body model, applicable std. MIL-STD-883, Method 3015.7. Machine model, applicable std. JESD22–A115–A (ESD MM std of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22–C101–C. (ESD FICDM std. of JEDEC)

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 5: Electrical Table values apply only for factory testing (ATE) conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 6: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 7: Limits are 100% production tested at 25°C. Limits over temperature range are guaranteed through correlations using statistical quality control (SQC) method.

Note 8: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 9: Supply current depends on switching frequency and load.

Note 10: Positive current is current flowing into the device.

Note 11: C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 12: The device maintains stable, regulated output voltage without a load.

Note 13: The noise figure is the noise of the LDO only; harmonics of the output clocks are excluded.

Note 14: Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Note 15: Clock Request Inputs can tolerate logic high input levels up to V_{BAT}.

Timing Diagrams

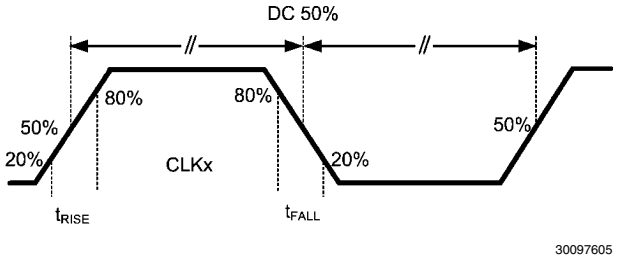


FIGURE 1. Rise / Fall time and Duty Cycle Waveform for Clock Outputs

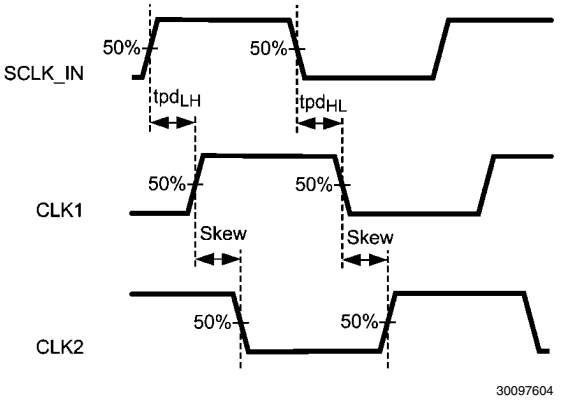


FIGURE 2. Clock Output Timing Waveforms

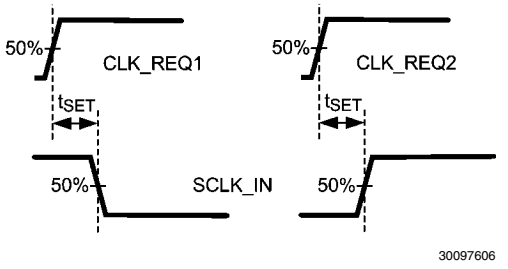
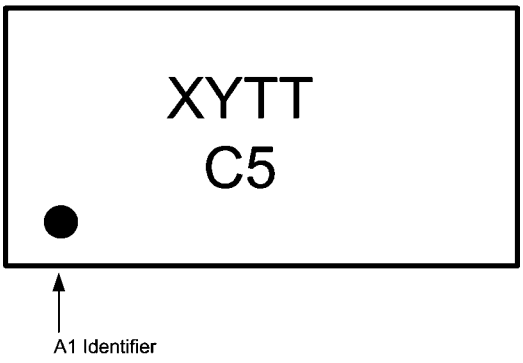


FIGURE 3. Clock Request Timing Waveforms

Connection Diagrams

Top view



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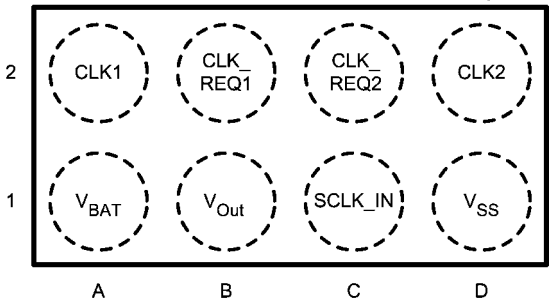
Text Marking

Top View



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Connections

Pin Descriptions

Pin	Pin Name	Port / Direction	Type	Description
C1	SCLK_IN	Host	Input	Source Clock Input
A2	CLK1	Peripheral	Output	Clock Output 1
B2	CLK_REQ1	Peripheral	Input	Clock Request Input 1 Clock1 = ON at high level
D2	CLK2	Peripheral	Output	Clock Output 2
C2	CLK_REQ2	Peripheral	Input	Clock Request Input 2 Clock2 = ON at high level
A1	V_{BAT}	Battery / Input	Power	Power Supply
B1	Vout	LDO / Output	Power	Power Supply to Clock Source and clock outputs
D1	V_{SS}	Ground	Ground	Ground Pin

I = Input, O = Output, I/O = Input / Output

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Bump microSMD	LMH2191TME	XYTT C5	250 Units Tape and Reel	TMP0008LAA
	LMH2191TMX		3K Units Tape and Reel	

Block Diagram

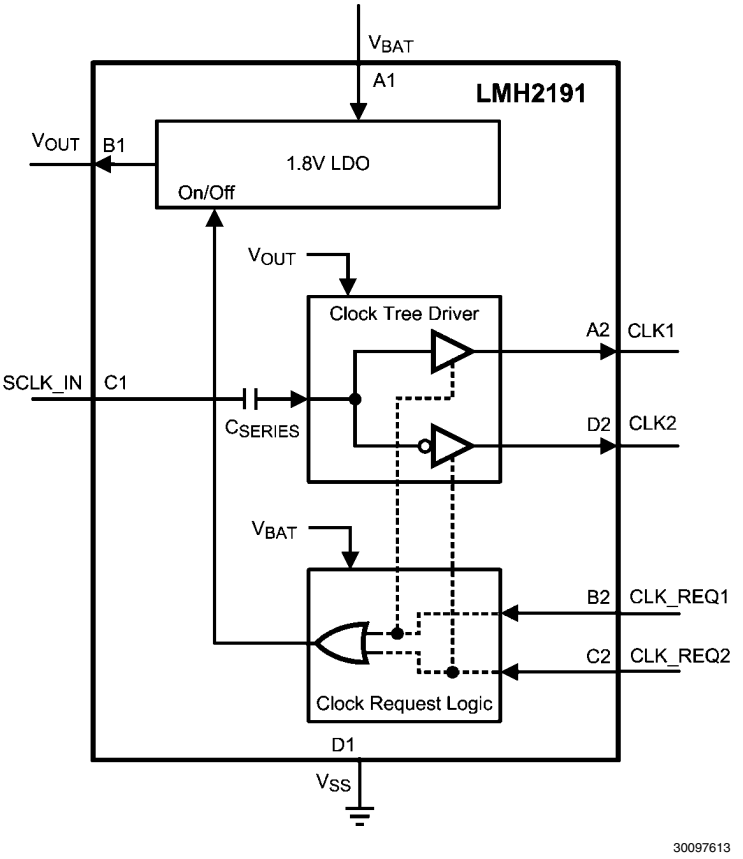
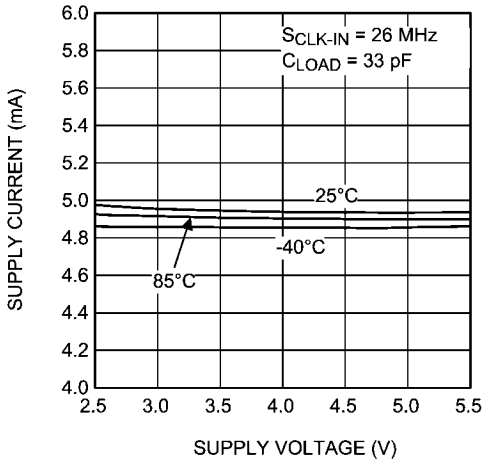


FIGURE 4. Block Diagram

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, I_{LOAD} = 2.5 mA.

Supply Current vs. Supply Voltage



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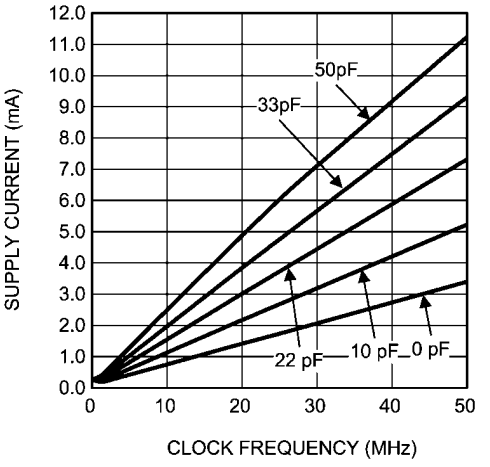
Supply Current vs. Input Clock Frequency



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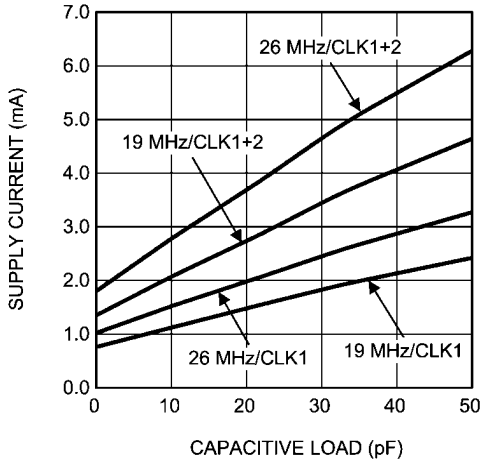
Supply Current vs. Capacitive Load



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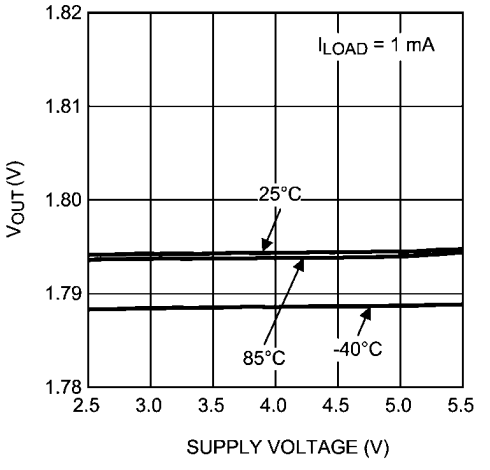
LDO output Voltage vs. Supply Voltage



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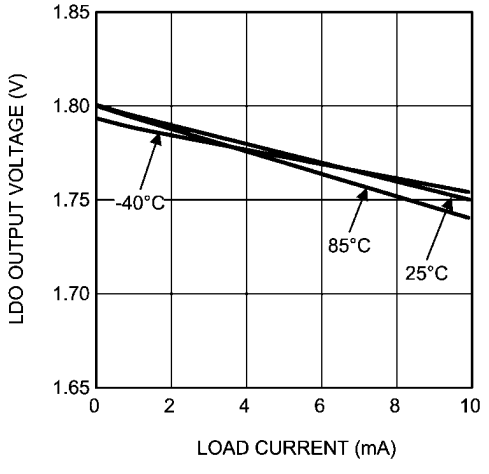
LDO output Voltage vs. LDO output current



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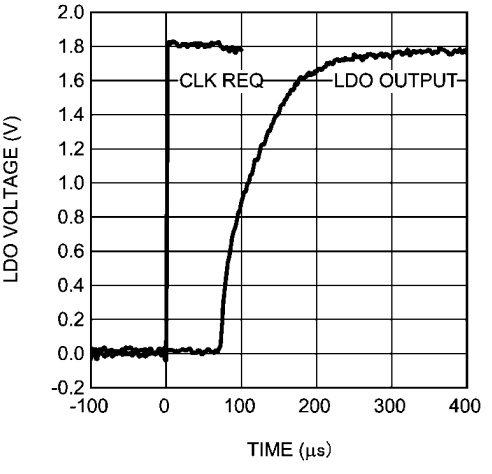
LDO output voltage ON timing



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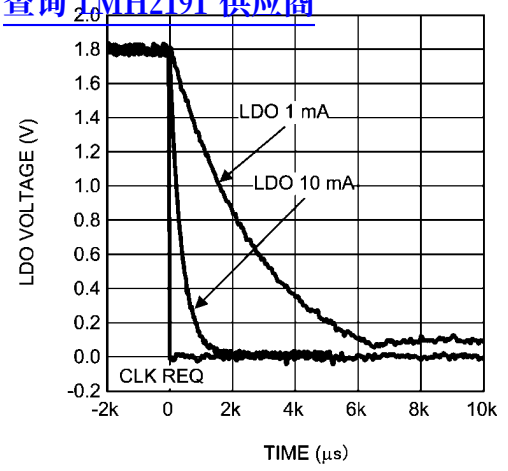
LDO output voltage OFF timing



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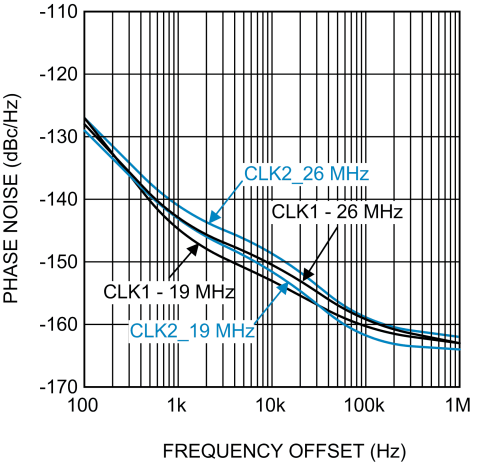
Additive Phase Noise vs. Frequency Offset



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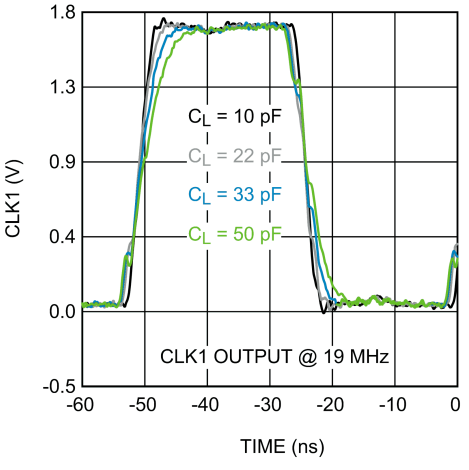
CLK1 Pulse Response 10-50pF @ 19MHz



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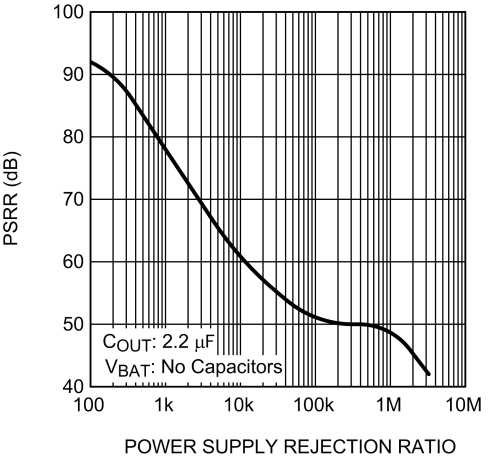
Power Supply Rejection Ratio vs. Frequency



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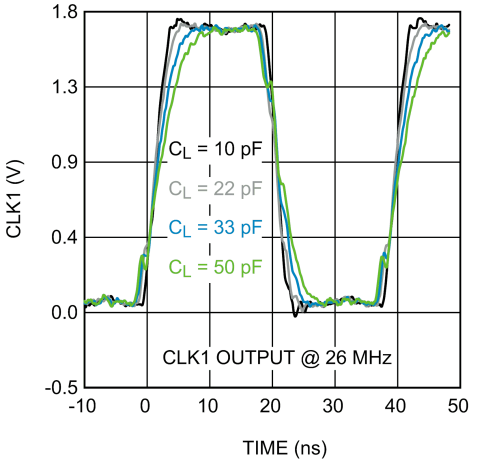
CLK1 Pulse Response 10-50pF @ 26MHz



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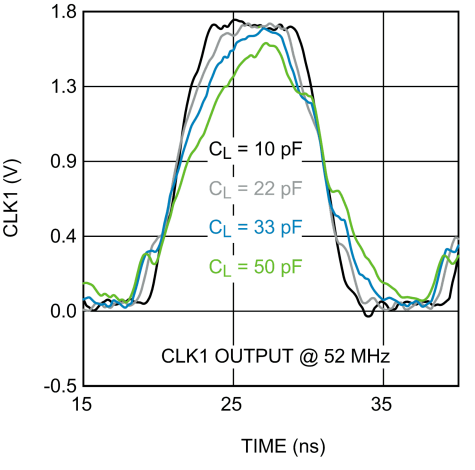
CLK1 Pulse Response 10-50pF @ 52MHz



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Application Information

The LMH2191 is a complete 52 MHz clocking conditioner and clock tree driver. The LMH2191 is used to supply a common clock to mobile phone peripherals such as Bluetooth, Wireless LAN, and/or Digital Video Broadcast-H (DVB-H). The high isolation between the clock outputs ensures that the peripherals don't disrupt each other. Its excellent phase noise characteristics prevent the clock quality from deteriorating. A typical LMH2191 setup is depicted in *Figure 5*.

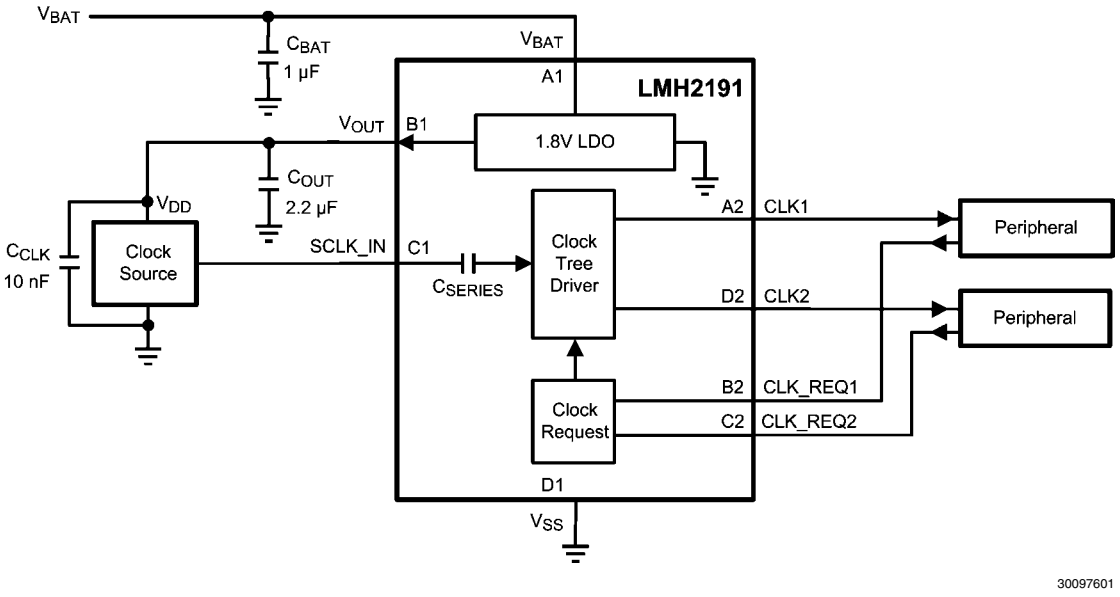


FIGURE 5. LMH2191 Typical Application Schematic

The internal structure of the LMH2191 is depicted in the block diagram of *Figure 6*.

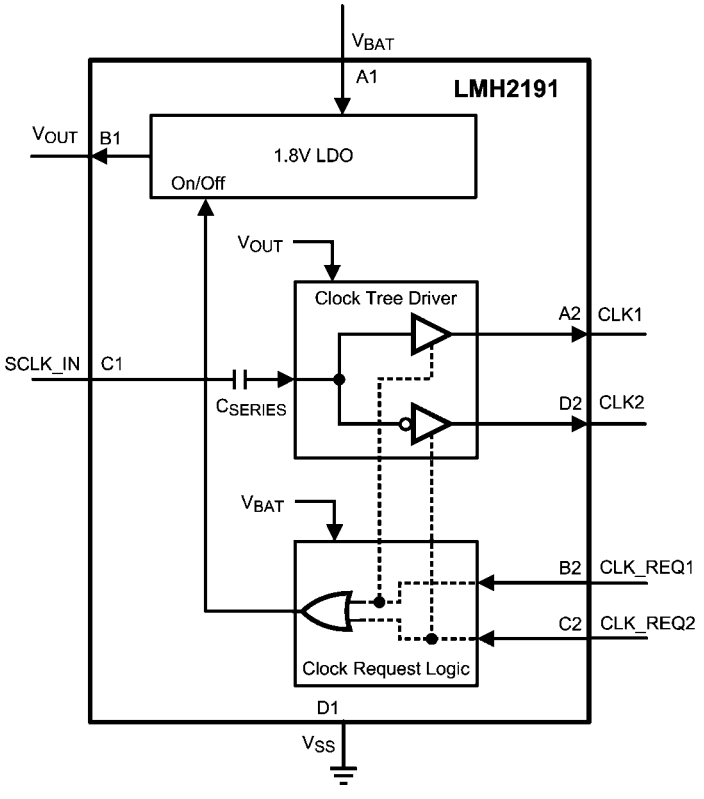


FIGURE 6. Block Diagram

The LMH2191 clock distribution circuit is comprised of 3 blocks:

- Clock tree driver
- Clock request logic
- Low Dropout Regulator (LDO)

The clock tree driver provides a clean clock to 2 separately connected peripheral devices. Independent clock request inputs allow the peripheral to control when the particular clock should be enabled. Furthermore, both clock request inputs control the LDO output voltage, e.g., when both request inputs are low (no CLK1 and no CLK2 output required), the LDO voltage is disabled. The LDO provides a low-noise, high-PSRR supply voltage that enables low phase noise on the clock outputs, and low quiescent current for portable applications. It can also be used to supply the TCXO. The following sections provide a detailed description of each block.

CLOCK TREE DRIVER

The clock tree driver consists of one input that drives 2 outputs. It is supplied by a high-precision voltage regulator of 1.8V, the LDO. The Clock outputs are enabled when the appropriate Clock Request inputs are logic high.

Clock Tree Driver Input

The source clock input (SCLK_IN) is the input for the clock tree driver. This input has an internally connected coupling capacitor (C_{SERIES}). In shutdown mode (when both CLK_REQ inputs are low), the input stage is completely switched off to prevent unnecessary power consumption when the source clock is still present.

Due to the internal coupling capacitor, the clock signal is DC biased, since the coupling capacitor prevents the internal biasing of the input circuitry to be affected by the external DC voltage. Because of the coupling capacitor, the minimum clock frequency is 10 MHz. It is assumed that the input signal is a sine wave or a typical TCXO waveform (the signal from a TCXO has slow edges), enabling the control loop to adjust to a duty cycle of 50% if the input signal differs slightly from 50% duty cycle. The duty cycle is an important timing parameter for the peripheral equipment. The circuit that adjust the duty cycle is shown in *Figure 7*.

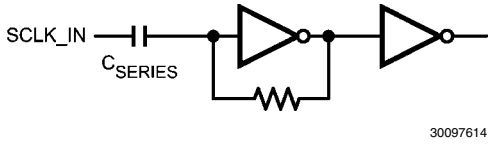


FIGURE 7. Clock Duty Cycle Regulation

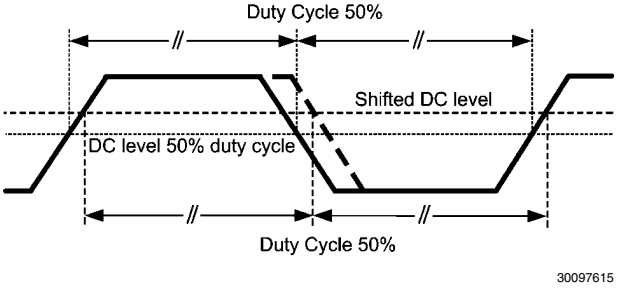


FIGURE 8. Duty Cycle adjust levels

In order to achieve a duty cycle of 50%, the edges of the incoming clock signal (SCLK_IN) are used to move the switching point to the level that is needed to create the 50% duty cycle. The simplified input circuit consists of an inverter and a feedback resistor. Together with the input series capacitor of about 30 pF, the circuit creates a DC level depending on the duty cycle of the incoming clock signal. When the duty cycle is exactly 50%, the DC level is in the middle of the upper and lower pulse level. When the duty cycle differs from 50%, the DC level shifts slightly to maintain the duty cycle level at 50%. (See Duty Cycle adjust levels of *Figure 8*.) As explained above, the slow edges of the SCLK_IN signal are important to make the control loop work.

Input Impedance

The input impedance can be split up into two parts: the DC input resistance and the AC input impedance. Due to the used series capacitor in the input signal path the DC resistance is infinite. The AC input impedance is formed by the circuit drawn in *Figure 7*. This circuit consists of an inverter and a feedback resistor. A signal fed to the input pin is connected to the inverter input which has a high input impedance and is in parallel to the feedback resistor of 30 kΩ. The other pin of the feedback resistor is connected to the output of the inverter which means that the input current is higher than it would be if it were connected to a decoupled supply connection. For this reason the AC input resistance can be much lower than the connected feedback resistor of 30 kΩ. The input resistance is dependant on the amplitude of the input signal. When an input amplitude of 1.8V is used (the same amplitude as the output of the inverter), the input impedance is theoretical half the value of the feedback resistor. When the amplitude of the input signal lowers, the input resistance becomes lower too. With an input signal of $1V_{PP}$, the input impedance will be about 10 kΩ.

Clock Tree Driver Outputs

The LMH2191's clock tree driver outputs have a drive strength that make each output capable of driving a capacitive load up to 50 pF, together with a minimum of EMI. Further reduction of EMI is achieved by the inversion of the CLK2 output. (See *Figure 9*.) Both the drive strength and the capacitive load make the edges of the output pulse relative slow which is favorable for EMI reduction.

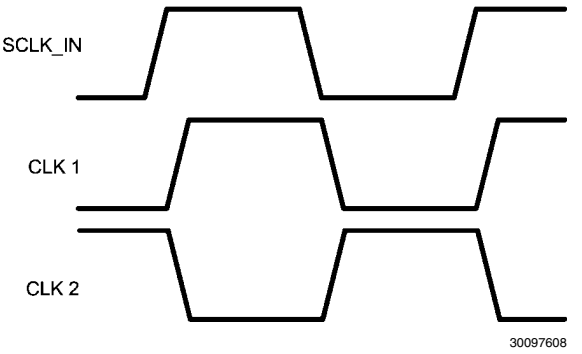


FIGURE 9. Clock Outputs

CLOCK REQUEST LOGIC

A clock request input is provided for each clock output. This allows the peripheral device to control when it wants to receive a clock. In case the application does not have clock request functionality, the CLKx_REQ can be hard wired to a logic high level to enable the clock output continuously. The clock request inputs have logic levels compatible with 1.8V logic, but can tolerate logic high levels up to V_{BAT}.

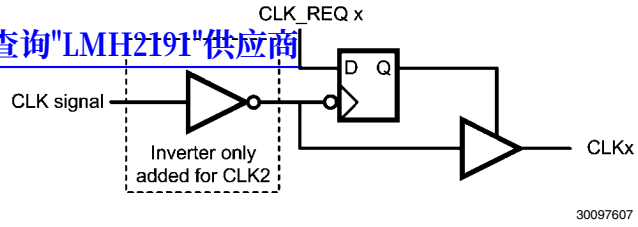


FIGURE 10. Enabling the output

The clock request logic enables an independent control of the clock tree driver outputs, CLK1 and CLK2, as well as an LDO disable when both request inputs are low.

The on and off switching of the clock output drivers is done synchronously with the clock input in order to prevent glitches at the clock output. For this the clock request signal is connected to the D input of a latch. The Q output of this latch enables the clock output driver (see *Figure 10*). For the CLK1 output the CLK input signal is connected via an inverter to the clock input of the latch. In this way the latch enables and disables the CLK1 output buffer on the falling edge of the clock signal. For the CLK2 output an extra inverter is inserted prior to the latch circuit, and the CLK2 output buffer is enabled and disabled on the rising edge of the clock input signal (equal to the falling edge of the CLK2 output signal).

LOW DROPOUT REGULATOR

The linear and Low-Dropout regulator (LDO) is used to regulate the input voltage, V_{BAT}, thus generating a well-defined ultra low noise 1.8V supply voltage. This allows the LMH2191 to suppress V_{BAT} supply voltage ripple and noise for the TCXO and the internal Clock Path. Voltage ripple and noise would distort clock edges causing extra phase noise on the distributed clock signal.

The LDO is powered up whenever a Clock Request is active; it supports overheating detection and will switch off in case overheating occurs. The recommended sequence for powering up the LDO is to raise a clock request to a high level with the supply already powered up. Thus the LDO stays in shutdown mode with sub µA current consumption until an output clock is actually needed. The LDO will power up within the turn-on time of about 200 µs (as specified in the data sheet tables). Alternatively, the clock request input can be hard wired to V_{BAT} which powers up the LDO simultaneously with V_{BAT}. A drawback is that the LDO and clock path (and if connected, the TCXO) will always draw current when V_{BAT} is powered up. Also, in this setup, care should be taken with supplies with an excessive long startup time of more than about 25 ms. Under this condition the LDO could exhibit excessive long turn-on delay (order of seconds.)

LAYOUT RECOMMENDATIONS

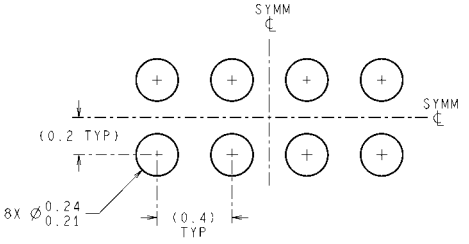
As with any other device, careful attention must be paid to the board layout. If the board isn't properly designed, the performance of the device can be less than desired. Care should be taken that the SCLK_IN input trace and the output traces of CLK1 and CLK2 are as short as possible to reduce extra capacitive load observed by the clock outputs. Also proper de-coupling close to the device is necessary. *Table 1* depicts the advised component values. NSC suggests to use the evaluation board, available from the National Semiconductor web site www.National.com, as a guide for layout and as an aid in device testing and characterization.

TABLE 1. Recommended Component Values

Symbol	Parameter	Min	Typ	Max	Units
C_{BAT}	Capacitor on V_{BAT}	0.47	1		µF
C_{OUT}	Capacitor on V_{OUT}	1	2.2		
ESR	Equivalent Series Resistance	5		500	mΩ

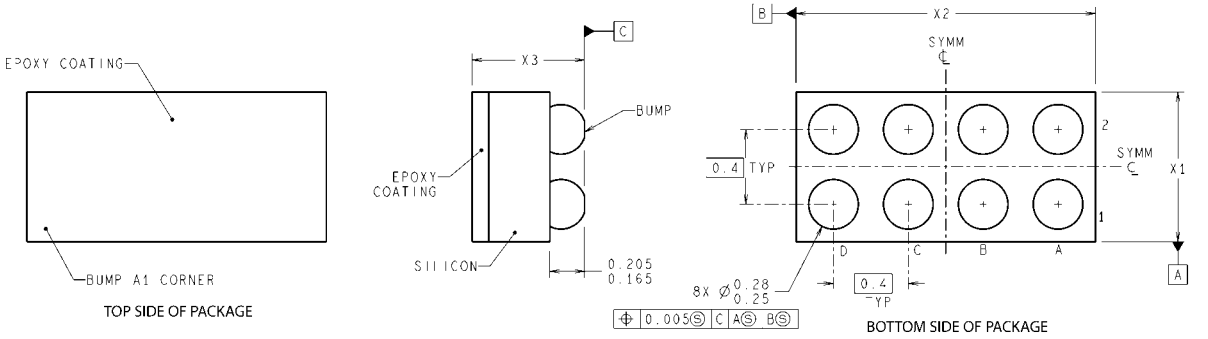
C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCC's) used in setting electrical characteristics.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TMP08XXX (Rev A)

8 bump Thin Micro SMD
NS Package Number TMP0008LAA
X1=1.070mm; X2=1.615mm; X3=0.600mm

Notes

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Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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