MirrorBit™ and MirrorFlash™ Status Bits and Erase Suspend Timing

Application Note

Introduction

As new microprocessors achieve faster and faster speeds, the response time of flash memory has become increasingly important. When working with MirrorBit/ MirrorFlash devices, which are typically used with high-end microprocessors, knowing how to address the response time limitations is even more important. Two of the most common instances that engineers are faced with response time issues are when checking the status of a program operation or when performing multiple erase/suspend operations.

Checking Status Bits during Program Operations

With the addition of write buffers in MirrorBit/MirrorFlash devices, the response time of the DQ Status Bits has changed slightly. When checking the program status, the DQ Status Bits are not guaranteed to be valid until 4 µs after the program command (see Figure 1) is issued. Note that all program operations on MirrorBit/ MirrorFlash parts take more than 4 µs to complete. In other words, the only status information expected within the first 4 µs would be “Program in Progress” or “Write to Buffer Operation Aborted”.

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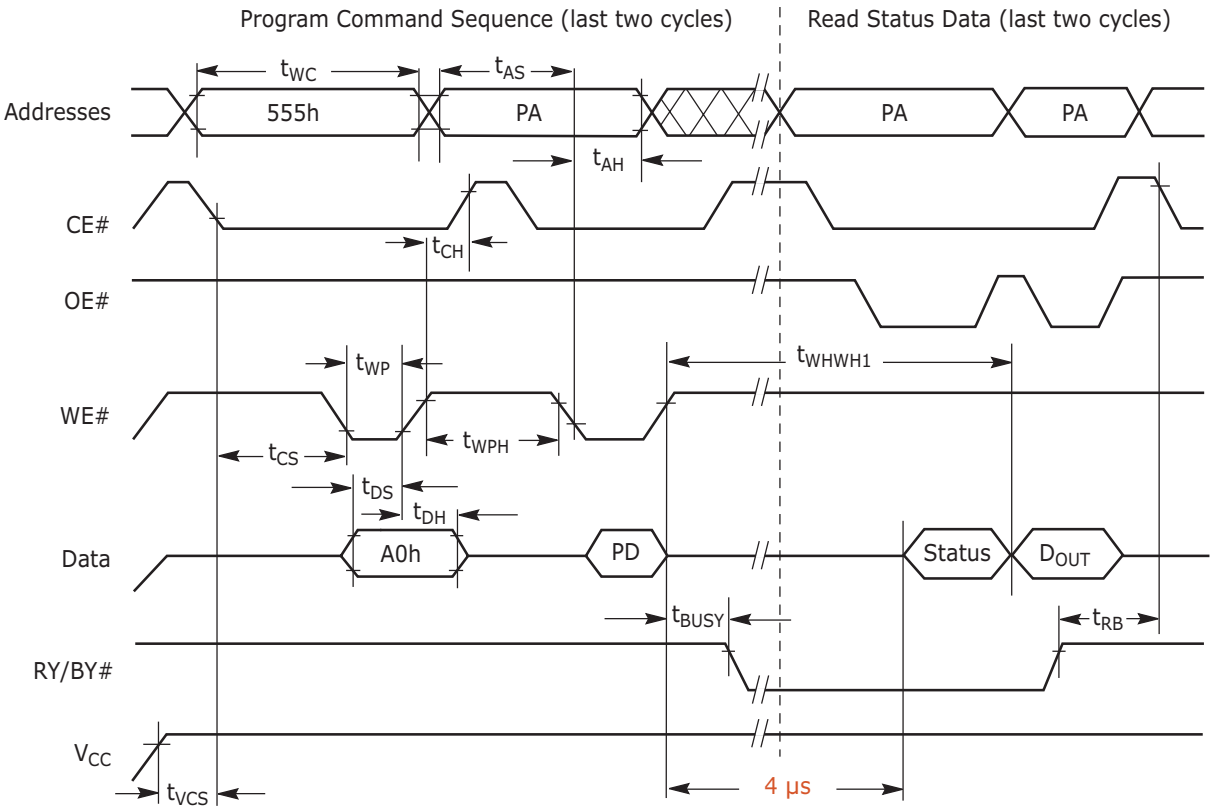

Figure I. Program Operation

If the write-buffer page boundary is crossed while programming the write buffer, MirrorBit/MirrorFlash devices will return the abort condition status (DQ1 = 1, DQ7 = data for the last address loaded, DQ6 = toggle, and DQ5 = 0) on the next read and will NOT be affected by the 4 µs status bit delay.

Program status can be checked using the DQ6 toggle-bit for “busy/programming in progress”, independent of the address being read; however, polling for “done/successful operation” should be performed on the address being programmed or on the last word in the program buffer.

Reading Status Bits Without Waiting 4 µs

To read the program status without waiting 4 µs, the output enable (OE#) control must be permanently tied low. In some systems, this may cause interference on the data bus; however, no issue should be present in systems that use the CE# signal to control access to the flash. In addition, if a Write Buffer operation is aborted, there is no 4 µs delay in reading the status bits.

Reading Status Bit When Using Program Suspend/Resume

If the suspend command is issued less then 4 µs after the program command, the system must wait 4 µs after programming is resumed before the status bits are valid. If the suspend command is issued more than 4 µs after the program command, there will be no delay when reading the status bits after programming is resumed.

Sector Erase/Suspend/Resume Timing

Spansion devices allow the user to suspend an erase and resume at a later time. During an erase operation, the flash device performs multiple internal operations, which are invisible to the system. When an erase operation is suspended, any of the internal operations that were not fully completed must be restarted. As such, if a flash device is continually issued suspend/resume commands in rapid succession, erase progress will be impeded as a function of the number of suspends. The result will be a longer overall erase time than without suspends. Note that the additional suspends will not affect device reliability or future performance.

In most systems rapid erase/suspend activity occurs only briefly. In this example, erase performance will not be significantly impacted.

Revision Summary

Revision A (September 10, 2003)

Initial release.