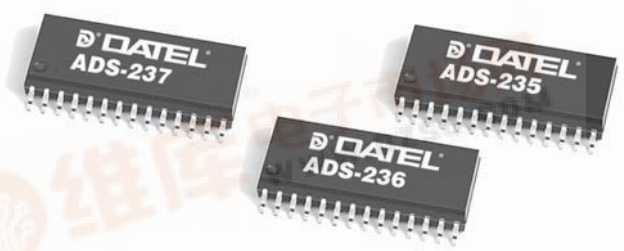
ADS-235, ADS-236, ADS-237

12-Bit, 5MHz and 9MHz Sampling A/D Converters

FEATURES

- 5MHz (ADS-235/236) and 9MHz (ADS-237) sampling rates
- Low power
- Outstanding dynamic performance
- Fully differential or single-ended analog input
- 100MHz full power input bandwidth
- Integral sample-and-hold
- Single +5V supply operation
- Internally generated DC bias Voltage
- 3.0/5.0V CMOS compatible digital output
- TTL/CMOS compatible digital inputs/outputs



GENERAL DESCRIPTION

The ADS-235, ADS-236 and ADS-237 are monolithic, 12-bit, sampling analog-to-digital converters fabricated in a CMOS process. The converters are designed for applications where high speed, wide bandwidth and low power dissipation are essential. These characteristics are provided through the use of a fully differential sampling pipeline A/D architecture with digital error correction logic.

The ADS-235, ADS-236 and ADS-237 offer excellent dynamic performance while consuming only 300mW. The digital output circuit is separate and can be powered from either a 3V or 5V supply allowing the user to interface with 3V logic, if desired.

The ADS-235, ADS-236 and ADS-237 provide the user with an internally generated DC bias voltage output. This DC bias voltage is ideal for AC coupled analog input applications. The units are available in a 28-lead plastic SOIC package and operate over the 0°C to 70°C and –40 to +85°C temperature ranges.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CLK, CLOCK	28	BIT 12
2	+DVS1, +5V DIG. SUP.	27	BIT 11
3	DGND1	26	BIT 10
4	+DVS1, +5V DIG. SUP.	25	BIT 9
5	DGND1	24	BIT 8
6	+AVS, +5V ANALOG SUP.	23	BIT 7
7	AGND	22	+DVS2, DIG. OUTPUT SUP.
8	VIN+, ANALOG INPUT	21	DGND2
9	VIN–, ANALOG INPUT	20	BIT 6
10	VDC, DC BIAS OUTPUT	19	BIT 5
11	VROUT, REF. OUT	18	BIT 4
12	VRIN, REF. IN	17	BIT 3
13	AGND	16	BIT 2
14	+AVS, +5V ANALOG SUP.	15	BIT 1 (MSB)

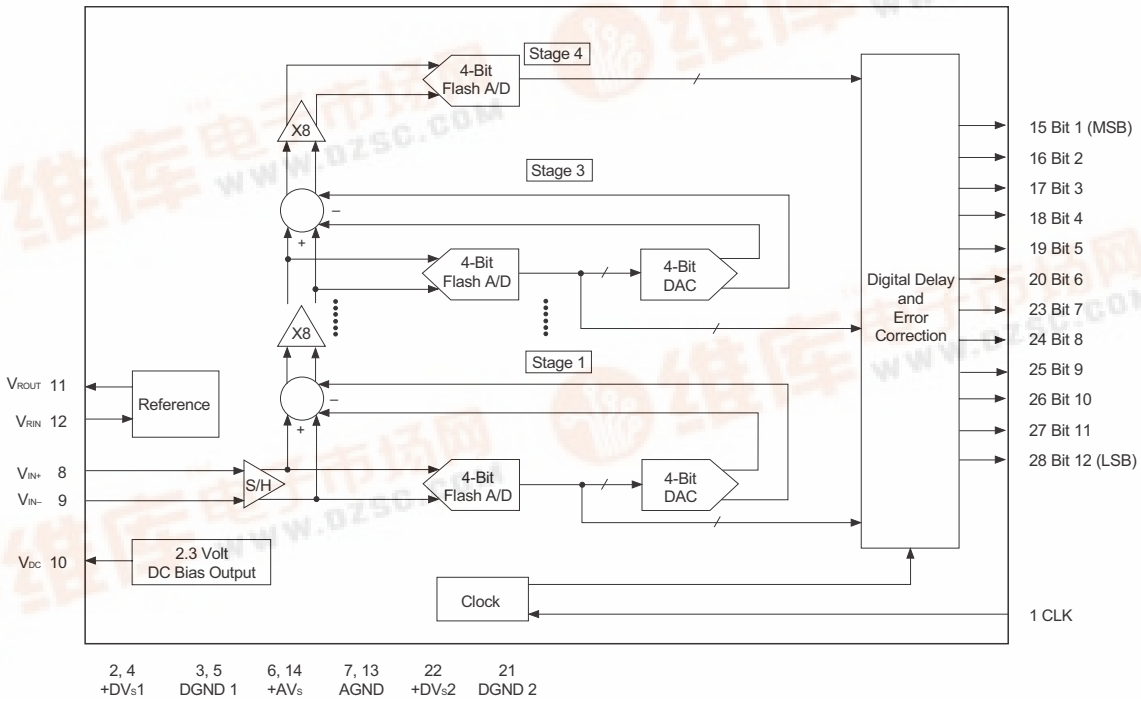


Figure 1. ADS-235, ADS-236 and ADS-237 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+AVs, +DVs1 and +DVs2 Supplies	+6.0	Volts
DGND to AGND	0.3	Volts
Analog I/O Pins	AGND to +AVs Supply	Volts
Digital I/O Pins	DGND to +DVs Supply	Volts
Lead Temperature (10 seconds, Pin Tips Only)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temperature Range				
ADS-235S	0	—	70	°C
ADS-236S/ADS-237S	–40	—	85	°C
Storage Temperature Range	–65	—	150	°C
Thermal Resistance, θja ①	—	75		°C/W
Junction Temperature	—	—	150	°C
Package Type	28-Pin Plastic SOIC			

① Measured mounted on PC board in free air.

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, (ADS-235), TMIN to TMAX (ADS-236/237), +DVs1 = +DVs2 = +AVs = +5V, V_{RIN} = 3.5V, F_S = 5MHz (ADS-235/236) and 9MHz (ADS-237) at a 50% duty cycle, CL =10pF, and differential analog input unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Max. Peak-to-Peak Diff. Voltage Input Range (V_{IN+} - V_{IN-})	—	±2.0	—	Volts
Max. Peak-to-Peak Single-Ended Voltage Input Range	—	4.0	—	Volts
Analog Input Common Mode Voltage Range (V_{IN+} + V_{IN-})/2 ①	1.0	2.3	4.0	Volts
Input Bias Current, IB+ or IB– ②	–10	—	10	µA
Differential Input Current, (IB+ - IB–)	—	±0.5	—	µA
Input Impedance ②	1.0	—	—	MΩ
Input Capacitance	—	10	—	pF
INTERNAL VOLTAGE REFERENCE				
Reference Output Voltage, V_{ROUT}	—	3.5	—	Volts
Reference Output Current	—	—	1	mA
Reference Temperature Coefficient				
ADS-235 ③	—	—	—	ppm/°C
ADS-236	—	200	—	ppm/°C
ADS-237	—	50	—	ppm/°C
REFERENCE VOLTAGE INPUT				
Reference Voltage Input, V_{RIN}	—	3.5	—	Volts
Total Reference Resistance, R_L	—	7.8	—	kΩ
Reference Current	—	450	—	µA
PERFORMANCE				
Resolution	12	—	—	Bits
Maximum Sample Rate, F_{CLK}				
ADS-235	—	5	—	MHz
ADS-236	5	—	—	MHz
ADS-237	9	—	—	MHz
Minimum Sample Rate	—	0.5	—	MHz
Integral Nonlinearity, F_{IN}=DC				
ADS-235	—	±2.0	—	LSB
ADS-236, ADS-237	—	±1.0	±2.0	LSB
Differential Nonlinearity, F_{IN}=DC ④	—	±0.5	±1.0	LSB
Input Offset Error, F_{IN}=DC				
ADS-235	—	12	—	LSB
ADS-236, ADS-237	—	19	—	LSB
Full Scale Error, F_{IN}=DC				
ADS-235	—	24	—	LSB
ADS-236, ADS-237	—	32	—	LSB
Aperture Delay, t_{AP}	—	5	—	ns
Aperture Uncertainty, t_{AJ}	—	5	—	ps(RMS)
Full Power Input Bandwidth	—	100	—	MHz
Spurious Free Dynamic Range, SFDR, F_{IN}=1MHz				
ADS-235	—	73	—	dB
ADS-236	—	83	—	dB
ADS-237	—	77	—	dB
Total Harmonic Distortion, THD, F_{IN}=1MHz				
ADS-235	—	–70	—	dB
ADS-236	—	–80	—	dB
ADS-237	—	–75	—	dB

PERFORMANCE (cont.)	MIN.	TYP.	MAX.	UNITS
Second Harmonic, F_{IN}=1MHz				
ADS-235	—	–73	—	dB
ADS-236	—	–86	—	dB
ADS-237	—	–80	—	dB
Third Harmonic, F_{IN}=1MHz				
ADS-235	—	–73	—	dB
ADS-236	—	–83	—	dB
ADS-237	—	–77	—	dB
Effective Number Of Bits, ENOB, F_{IN}=1MHz				
ADS-235	—	10.3	—	Bits
ADS-236	—	11	—	Bits
ADS-237	—	10.8	—	Bits
Signal to Noise Ratio and Distortion, SINAD, F_{IN}=1MHz				
ADS-235	—	64	—	dB
ADS-236	—	68	—	dB
ADS-237	—	66.5	—	dB
Signal to Noise Ratio, SNR, F_{IN}=1MHz				
ADS-235	—	65	—	dB
ADS-236	—	68	—	dB
ADS-237	—	67.3	—	dB
Intermodulation Distortion, IMD, F1=1MHz F2=1.02MHz				
ADS-235	—	–66	—	dB
ADS-236	—	–68	—	dB
ADS-237	—	–65	—	dB
Transient Response ⑤	—	1	—	Cycle
Over-Voltage Recovery, 0.2V Overdrive	—	2	—	Cycle
TIMING CHARACTERISTICS				
Data Output Hold, t_H	—	8	—	ns
Data Output Delay, t_{OD}	—	8	—	ns
Clock Pulse Width, TPWO, TPW1				
ADS-235, ADS-236	90	100	110	ns
ADS-237	106	111	116	ns
Data Latency, t_{LAT}	—	—	3	Cycles
DC BIAS VOLTAGE OUTPUT				
DC Bias Voltage Output, V_{DC}	—	2.3	—	volts
DC Bias Voltage Current	—	—	1.0	mA
DIGITAL OUTPUTS				
Logic Levels				
Logic "1", +DVs2=5V, V_{OH}=2.4V	–0.2	—	—	mA
Logic "0", +DVs2=5V, V_{OL}=0.4V	1.6	—	—	mA
Logic "1", +DVs2=3V, V_{OH}=2.4V	—	–0.2	—	mA
Logic "0", +DVs2=3V, V_{OL}=0.4V	—	1.6	—	mA
Output Capacitance	—	5	—	pF

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Ranges				
+5V Analog Supply, +AVs	+4.75	5	+5.25	Volts
+5V Digital Supply, +DVs1	+4.75	5	+5.25	Volts
+3V Digital Supply, +DVs2	+2.7	3	+3.3	Volts
+5V Digital Supply, +DVs2	+4.75	5	+5.25	Volts
Power Supply Currents				
ADS-235, ADS-236				
+AIs	—	46	—	mA
+DIs1	—	13	—	mA
+DIs2	—	1	—	mA
ADS-237				
+AIs	—	46	—	mA
+DIs1	—	17	—	mA
+DIs2	—	2	—	mA
Power Dissipation				
ADS-235	—	300	—	mW
ADS-236	—	300	350	mW
ADS-237	—	325	365	mW
Offset Error Sensitivity, 5V±5%				
ADS-235	—	±16	—	LSB
ADS-236, ADS-237	—	2	—	LSB
Gain Error Sensitivity, 5V±5%				
ADS-235	—	±16	—	LSB
ADS-236, ADS-237	—	30	—	LSB

Footnotes: ① Differential Mode ② CLK off and Low
③ Not specified ④ No missing codes
⑤ For Fs step to settle to 12-bits accuracy

FUNCTIONAL DESCRIPTION

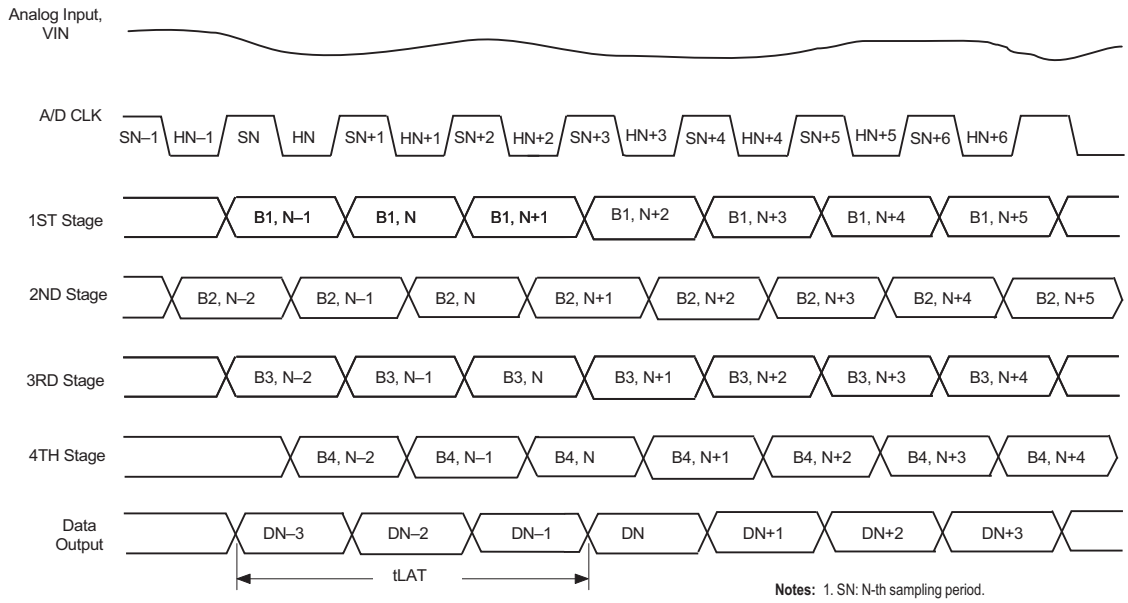
The ADS-235, ADS-236 and ADS-237 are 12-bit fully differential pipeline sampling A/D converters with digital error correction. Referring to the Functional Block Diagram shown in figure 1, figure 3.1 shows the circuit for the front end differential in and out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Ø1 and Ø2, derived from the master sampling clock. During the sampling phase, Ø1, the input signal is applied to the sampling capacitors, C_S. At the same time the hold capacitors, C_H, are discharged to analog ground. At the falling edge of Ø1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Ø2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample and hold cycle.

The sample and hold output is a fully differential representation of the sampled analog input. The circuit not only performs the sample-hold function but will also convert a single-ended input to a fully differential output. During the sampling phase, the V_{IN} pins see only the on resistance of a switch and C_S. The small values of these components result in a typical full power input bandwidth of 100MHz for the converters.

As illustrated in the Functional Block Diagram, figure 1, and the Internal Timing Diagram, figure 2A, three identical pipeline sub-converter stages, each containing a four-bit flash converter and a four-bit multiplying digital-to-analog converter, follow the S/H with the fourth stage being a four-bit flash converter. Each converter stage in the pipeline will be sampling in one clock phase and amplifying in the other clock phase. Each sub-converter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The four-bit output of each of the sub-converter stages is used by the error correction logic. The output of each stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the delay line is to align the digital outputs in time of the three identical stages with the output of the fourth stage flash converter before applying the sixteen bit result to the error correction logic. The error correction logic uses the supplementary bits to correct any error that may exist before generating the final twelve-bit digital data output.

Due to the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital



Notes: 1. SN: N-th sampling period.
2. HN: N-th holding period.
3. BM, N: M-th stage digital output corresponding to N-th sampled input.
4. DN: Final data output corresponding to N-th sampled input.

Figure 2A. Internal Timing Diagram

data bus on the third cycle of the clock after the analog sample is taken. After this latency delay, the digital data representing each successive sample of the analog input is output during the following clock cycle. The digital output data is synchronized to the external sampling clock through a double buffered latching circuit. The output of the digital error correction circuit is available in offset binary format.

Differential Analog Input

The analog input is a differential input that can be configured in various ways depending on the signal source and the level of performance desired. A fully differential connection as shown in figures 3.2 and 3.3 will give the best performance.

The ADS-235, ADS-236 and ADS-237 are powered by a single +5V analog power supply which limits the analog input to between ground and +5V. For the differential input connection this implies that the analog input common mode voltage can range from 1.0V to 4.0V, see figure 3.6. Performance for the converter does not change significantly with the value of the analog input common mode voltage. A DC voltage source, V_{DC}, equal to 2.3V, typical, is provided to help simplify circuit design when using an AC coupled differential input. This low impedance voltage source is not designed to be a reference voltage but makes an excellent DC bias source. This bias voltage source stays well within the analog input common mode voltage range over temperature.

The difference between the converter's two internal reference voltages is 2V. For the AC coupled differential input, figure 3.2, if V_{IN} is a 2Vp-p sinewave with $-V_{IN}$ 180 degrees out of phase with V_{IN}, then V_{IN}+ is a 2Vp-p sinewave riding on a DC bias voltage equal to V_{DC}. Consequently, the converter will be at a positive full scale when the V_{IN}+ input is at V_{DC}+1V and the V_{IN}– input is at V_{DC}-1V (V_{IN}+ - V_{IN}– = 2V). Conversely, the ADS will be at negative full scale when the V_{IN}+ input is equal to V_{DC}-1V and V_{IN}– is at V_{DC}+1V (V_{IN}+ - V_{IN}– = –2V). Thus, the converter has a peak-to-peak differential analog input voltage range of ±2V.

The analog input can be DC coupled, figure 3.3, as long as the inputs are within the analog input common mode voltage range ($1.0V \le V_{DC} \le 4.0V$). The resistors, R, are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from V_{IN}+ to V_{IN}– will help filter high frequency noise. Values of approximately 20pF are normally sufficient but the actual value must take into account the highest frequency component of the input signal.

Single-Ended Analog Input

The circuit in figure 3.4 may be used with a single-ended AC coupled input. Assuming again that the difference between the two internal voltage references is 2V and V_{IN} is a 4Vp-p sinewave, then V_{IN}+ is a 4Vp-p sinewave riding on a positive voltage equal to V_{DC}. The converter will be at a positive full scale when V_{IN}+ is at V_{DC}+2V (V_{IN}+ - V_{IN}– = 2V) and will be equal to a negative full scale when VIN+ is equal toVDC-2V (V_{IN}+ - V_{IN}– = –2V). In this case, V_{DC} could range between 2V and 3V without significant change in the converters performance. The simplest way to obtain a V_{DC} voltage is to use the V_{DC} output provided by the converters.

The single-ended analog input can be DC coupled, as shown figure 3.5, as long as the input is within the analog input common mode voltage range. The resistor, R, shown is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected between V_{IN}+ and V_{IN}– will help filter high frequency noise. A value of approximately 20pF is normally sufficient but the actual value must take into account the highest frequency component of the input signal.

INTERNAL REFERENCE GENERATOR, V_{ROUT} V_{RIN}

The ADS-235/236/237 have an internal reference generator, therefore, an external voltage is not required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage. Two reference voltages are generated internally, 1.3V and 3.3V, for a fully differential input range of ±2V.

An external reference may be used by connecting the external voltage reference to the V_{RIN} pin with V_{ROUT} left open. These units are tested with V_{RIN} equal to 3.5V.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the V_{RIN} pin.

Digital I/O and Clock

The ADS-235, ADS-236 and ADS-237 provide a standard high-speed interface to external TTL/CMOS logic families. In order to ensure rated performance the duty cycle of the clock should be held at 50% ±5%, have low jitter and operate at standard TTL levels. Performance is guaranteed for conversion

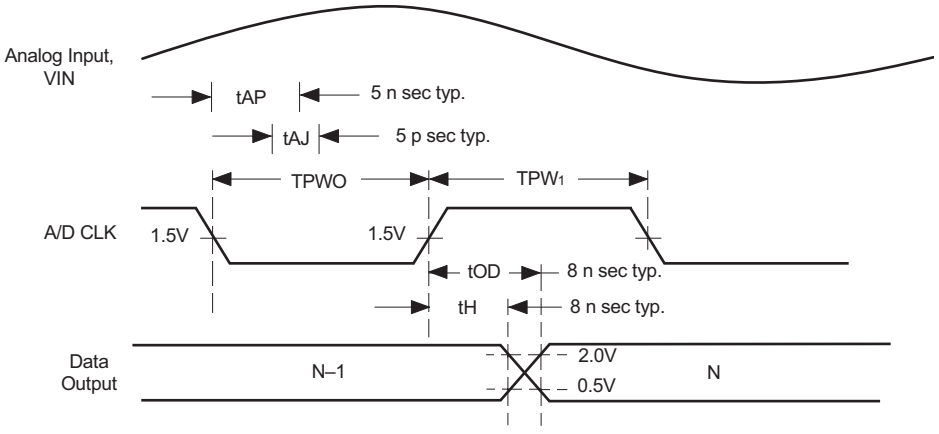


Figure 2B. Input-to-Output Timing

rates above 0.5MHz in order to ensure proper performance of the internal dynamic circuits.

Power Supplies and Grounding

The ADS-235, ADS-236 and ADS-237 have separate digital and analog power supply pins and grounds (refer to the Input/Output Connections table for pin numbers) to reduce digital noise in the analog signal path. The digital data outputs also have a separate supply pin, +DVS2, which can be powered from either a 3.0V or 5.0V supply to allow the user the option of interfacing with 3.0V logic.

The converters should be mounted on a board that provides separate low impedance paths for the analog and digital supplies and grounds. For best performance the supplies used should be clean, linear regulated supplies. All power supplies should be bypassed to ground with a 10uF tantalum capacitor in parallel with a 0.1uF ceramic capacitor. Locate the bypass capacitors as close to the converter as possible. If the converter is to be powered from one supply then the analog supply and ground pins should be isolated with ferrite beads from the digital supply and ground pins. See the Typical Connection Diagram, Figure 4.

In order to minimize overall converter noise it is recommended that the VRIN pin be bypassed using a 4.7 uF tantalum capacitor in parallel with a 0.01 uF ceramic capacitor. Locate the bypass capacitors as close to the unit as possible.

Figure 3.1 Analog Input Sample-and-Hold

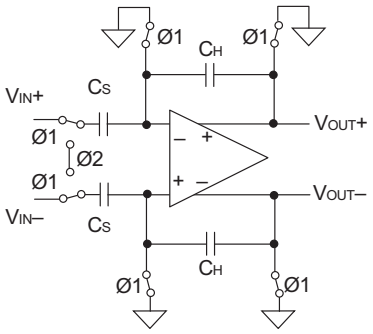


Figure 3.2 AC Coupled Differential Input

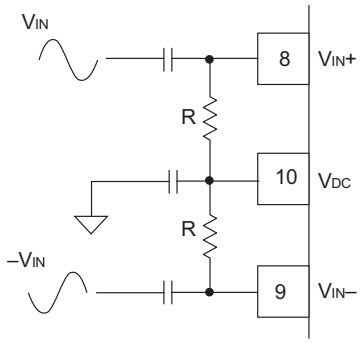


Figure 3.3 DC Coupled Differential Input

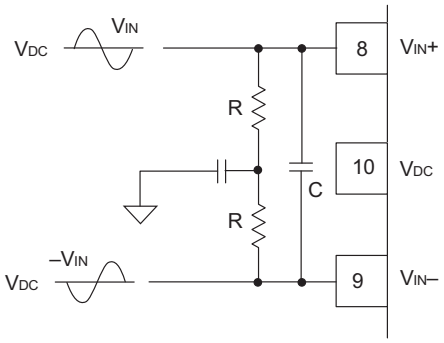


Figure 3.4 AC Coupled Single Ended Input

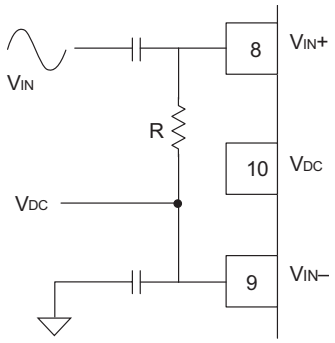


Figure 3.5 DC Coupled Single Ended Input

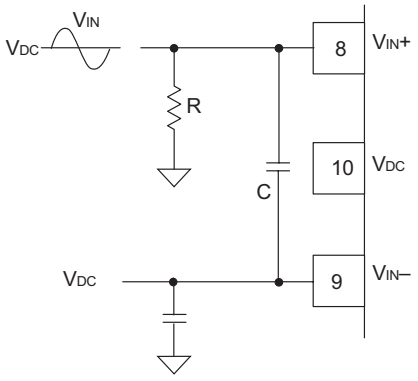


Figure 3.6 Differential Analog Input Common Mode Voltage Range

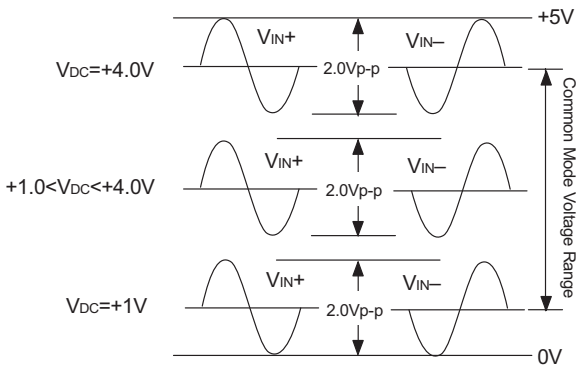


Figure 3. Analog Input

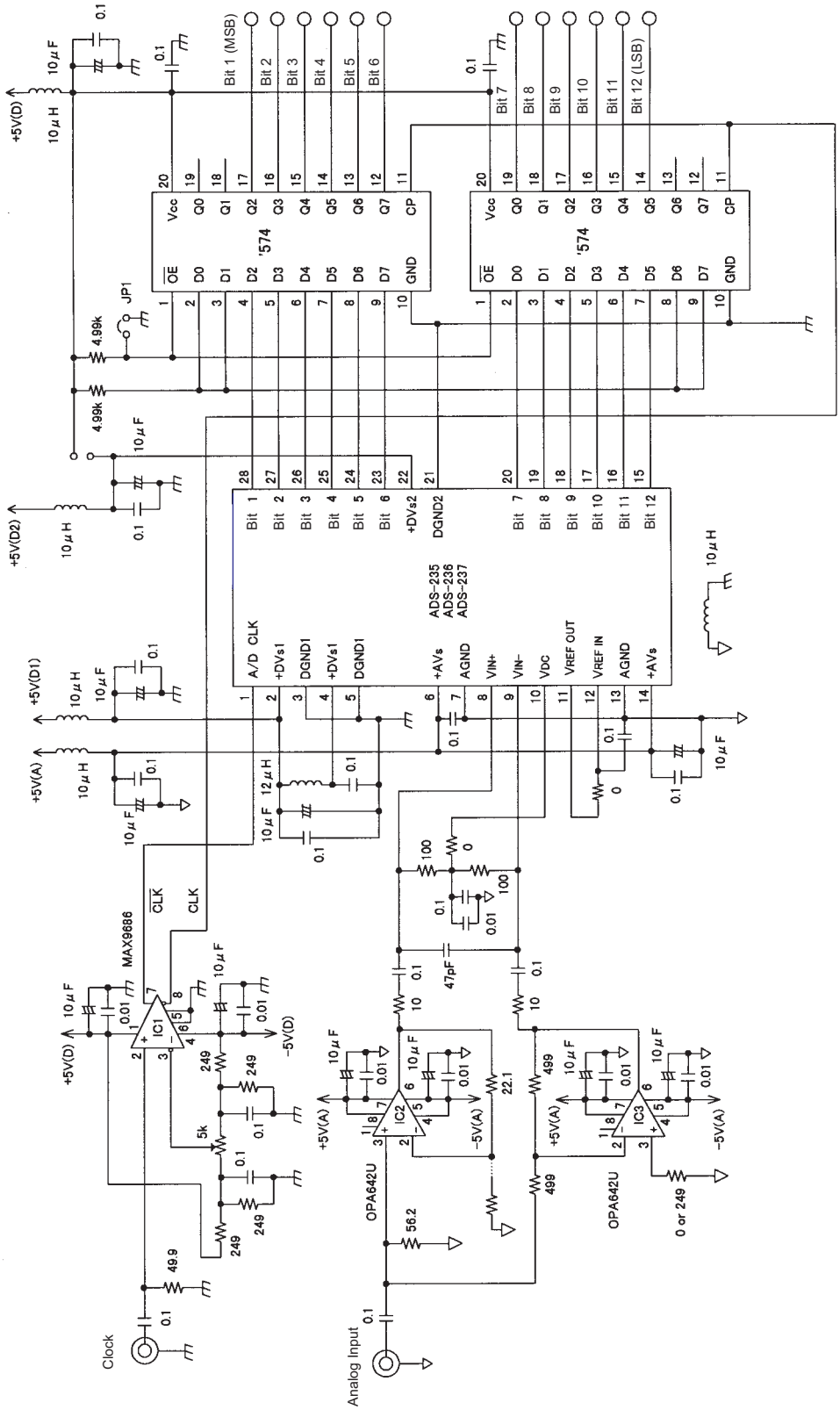
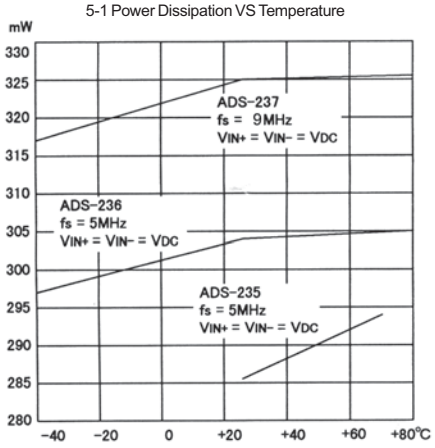
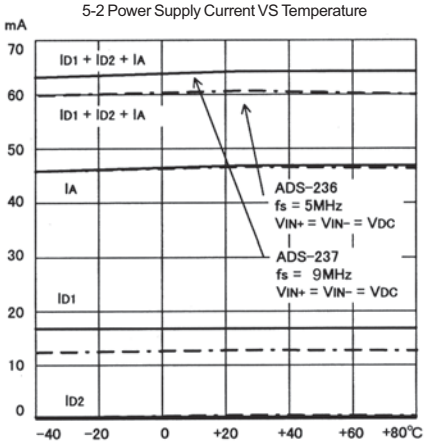


Figure 4. Typical Connection diagram

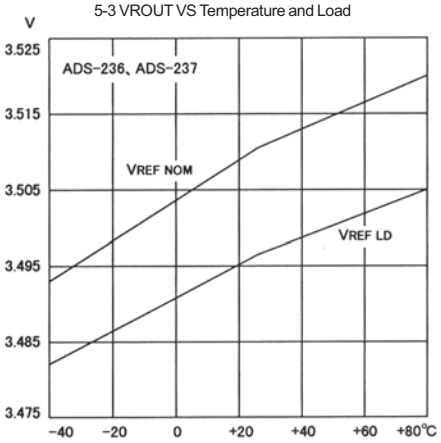
5-1 Power Dissipation VS Temperature



5-2 Power Supply Current VS Temperature

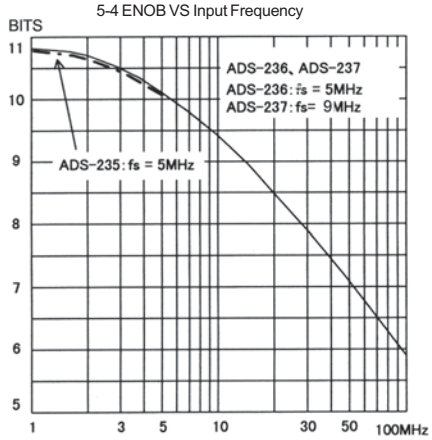


5-3 VROUT VS Temperature and Load

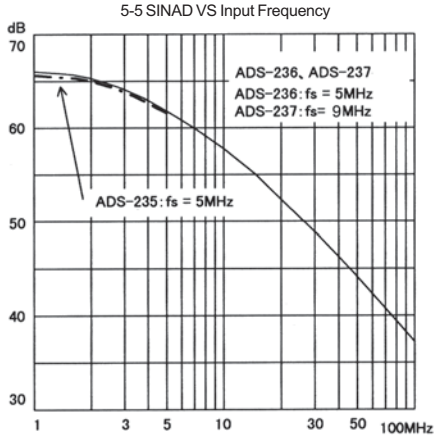


BITS

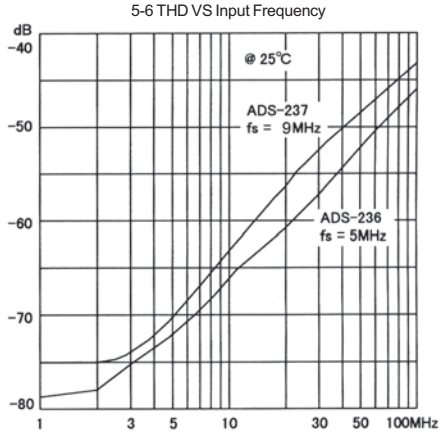
5-4 ENOB VS Input Frequency



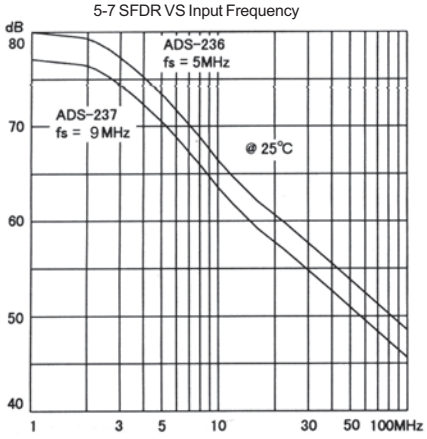
5-5 SINAD VS Input Frequency



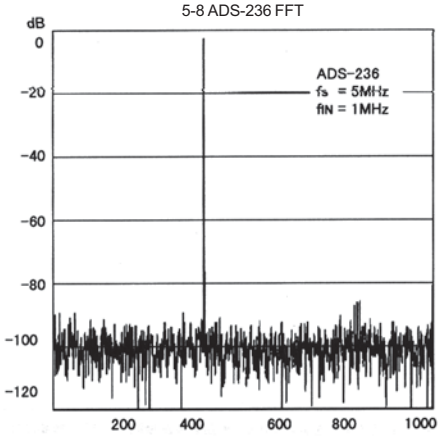
5-6 THD VS Input Frequency



5-7 SFDR VS Input Frequency



5-8 ADS-236 FFT



5-9 ADS-237 FFT

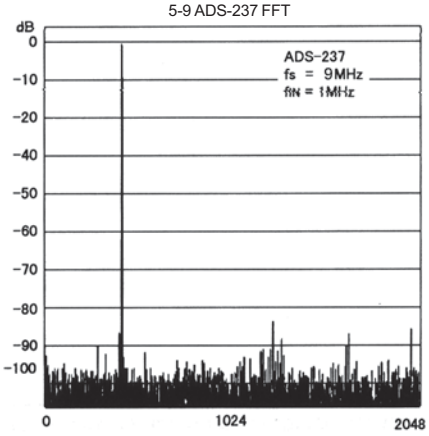
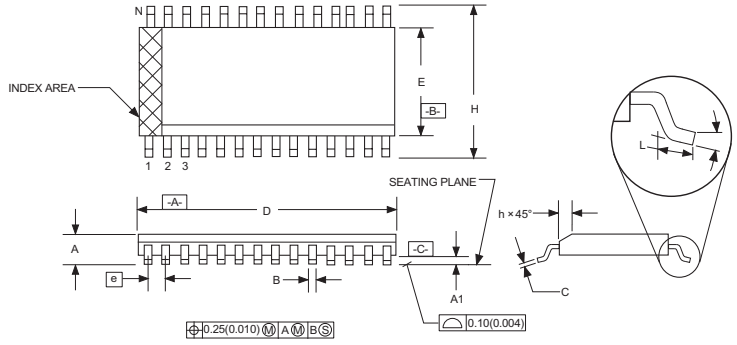


Figure 5. Typical Performance Curve

Table 1. Output Coding

BIPOLAR SCALE	DIFFERENTIAL INPUT VOLTAGE (using internal reference)	OFFSET BINARY MSB		LSB
+FS-1/4LSB	+1.99976V	1111	1111	1111
+FS-1¼LSB	+1.99878V	1111	1111	1110
+3/4 LSB	+732.4µV	1000	0000	0000
–1/4 LSB	–244.1µV	0111	1111	1111
–FS+1¾LSB	–1.99829V	0000	0000	0001
–FS+3/4 LSB	–1.99927V	0000	0000	0000

MECHANICAL DIMENSIONS INCHES (mm)



Notes:
1. Controlling dimensions: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. "L" is the length of terminal for soldering to a substrate.
6. Terminal numbers are shown for reference only.
7. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).

ADS-235S
ADS-236S
ADS-237S
28 Lead Wide Body Versions
SMALL OUTLINE PLASTIC PACKAGES (SOIC)

SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.0926	0.1043	2.35	2.65
A1	0.0040	0.0118	0.10	0.30
B	0.013	0.0200	0.33	0.51
C	0.0091	0.0125	0.23	0.32
D	0.6969	0.7125	17.70	18.10
E	0.2914	0.2992	7.40	7.60
e	0.05 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.01	0.029	0.25	0.75
L	0.016	0.050	0.40	1.27
N	28		28	
α	0°	8°	0°	8°

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SAMPLING FREQUENCY
ADS-235S	0 to +70°C	5MHz
ADS-236S	–45 to +85°C	5MHz
ADS-237S	–45 to +85°C	9MHz

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ISO 9001 REGISTERED

DS-0409A 05/01

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