

# 7

## 21052 Specifications

This chapter describes the mechanical and electrical specifications of the 21052.

### 7.1 Mechanical Specifications

The following sections describe the mechanical specifications of the 21052.

#### 7.1.1 21052 Package

The 21052 is packaged in a 160-pin PQFP. Table 7–1 lists the mechanical specifications, and Figure 7–1 shows the package dimensions of the 21052.

**Table 7–1 Lead Counts and Dimensional Attributes**

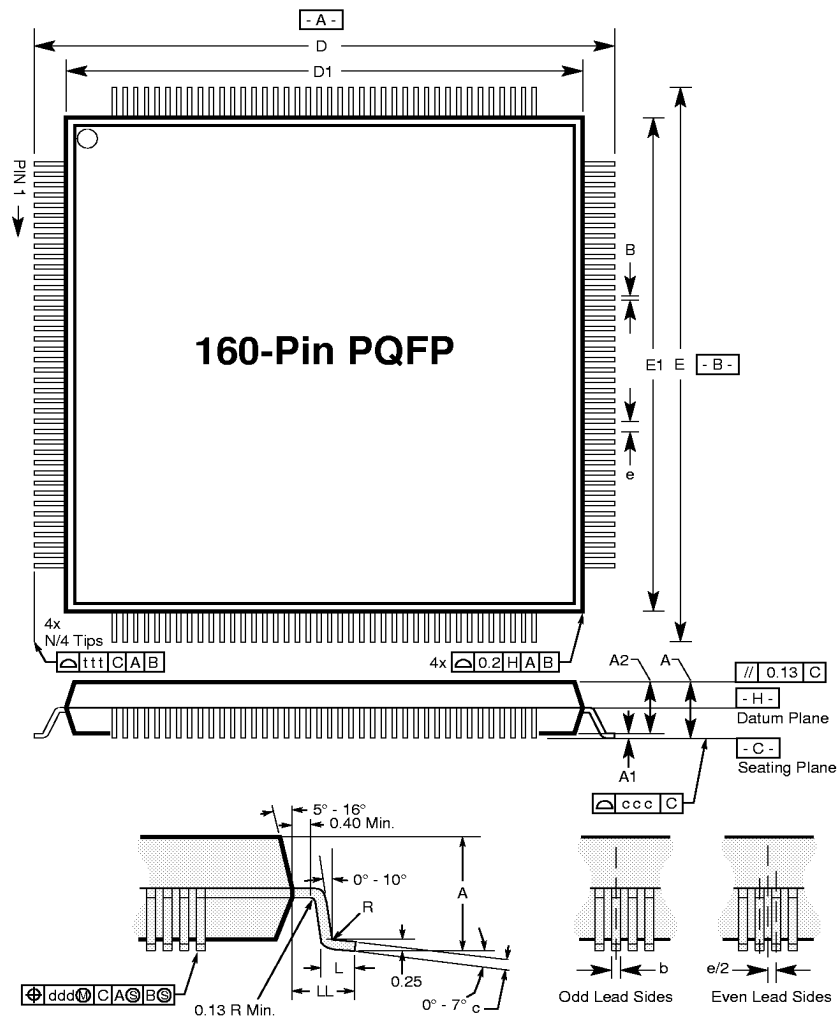
Symbol	Limit	Dimensions in Millimeters
LL	REF	1.6
e	BSC	0.65
L	MIN	0.65
L	MAX	1.03
A	MAX	4.5
A1	MIN	0.25
A2	MIN	3.17
A2	MAX	3.67
b	MIN	0.22
b	MAX	0.38
c	MIN	0.12
c	MAX	0.23

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**Table 7-1 (Cont.) Lead Counts and Dimensional Attributes**

<b>Symbol</b>	<b>Limit</b>	<b>Dimensions in Millimeters</b>
ccc	—	0.1
ddd	—	0.13
ttt	—	0.25
D	BSC	31.2
D1	BSC	28
E	BSC	31.2
E1	BSC	28
R	MIN	0.13
R	MAX	0.3

Figure 7-1 Package Dimensions



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## 7.1.2 Absolute Maximum Ratings

This section lists the absolute maximum ratings.

$V_{DD}$	3.0 V–3.6 V
$T_J$	100°C
$T_A$	70°C
$P_{WC}$	0.85 W
Storage temperature	–55°C to 125°C

## 7.2 Electrical Specifications

The following sections describe the electrical specifications of the 21052.

### 7.2.1 Interface Signal DC Electrical Specifications

Table 7–2 defines the dc parameters met by all 21052 signals.

**Table 7–2 DC Specifications**

Symbol	Parameter	Condition	Minimum	Maximum	Units
$V_{ih}$	Input high voltage	–	0.475 $V_{DD}$	5.5 V	V
$V_{il}$	Input low voltage	–	–0.5	0.325 $V_{DD}$	V
$I_{ih}$	Input high leakage current <sup>1</sup>	$V_{in} = 2.7$ V	–	70	μA
$I_{il}$	Input low leakage current <sup>1</sup>	$0 < V_{in} < V_{DD}$	–	±10	μA
$V_{oh}^2$	Output high voltage	$I_{out} = -500$ μA	0.9 $V_{DD}$	–	V
$V_{oh5V}^3$	Output high voltage	$I_{out} = -2$ mA	2.4	–	V
$V_{ol}^2$	Output low voltage	$I_{out} = 1500$ μA	–	0.1 $V_{DD}$	V
$V_{ol5V}^3, 4$	Output low voltage	$I_{out} = 6$ mA or $I_{out} = 3$ mA	0.55	–	V
$C_{in}$	Input pin capacitance	–	–	10	pF

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**Table 7–2 (Cont.) DC Specifications**

Symbol	Parameter	Condition	Minimum	Maximum	Units
$C_{IDSEL}$	<b>p_idsel</b> pin capacitance	–	–	8	pF
$C_{clk}$	<b>p_clk, s_clk</b> pin capacitance	–	5	12	pF

Footnotes:

1. Input high leakage current and input low leakage current include  $I_{ozl}$  or  $I_{ozh}$  leakage current for bidirectional signals.
2. For 3.3-volt signaling environment.
3. For 5.5-volt signaling environment.
4. Most output low voltage signals have 3 mA of current. The following output low voltage signals have 6 mA of low output current:

<b>p_frame_l</b>	<b>p_trdy_l</b>	<b>p_irdy_l</b>	<b>p_devsel_l</b>
<b>p_stop_l</b>	<b>p_serr_l</b>	<b>p_perr_l</b>	<b>p_lock_l</b>
<b>s_frame_l</b>	<b>s_trdy_l</b>	<b>s_irdy</b>	<b>s_devsel_l</b>
<b>s_stop_l</b>	<b>s_perr_l</b>	<b>s_lock_l</b>	

## 7.2.2 Interface Signal AC Timing Specifications

Table 7–3 and Figure 7–2 show the **p\_clk** and **s\_clk** ac timing.

**Table 7–3 p\_clk and s\_clk AC Timing**

Symbol	Parameter	Minimum	Maximum	Units	Notes
$T_{cyc}$	<b>xclk</b> cycle time	30	–	ns	–
$T_{high}$	<b>xclk</b> high time	12	–	ns	@1.5 V and @1 V/ns
$T_{low}$	<b>xclk</b> low time	12	–	ns	@1.5 V and @1 V/ns
	Slew rate	1	4	V/ns	0.4 to 2.4 V
$T_{skew}$	Delay from <b>p_clk</b> to <b>s_clk</b>	0	7	ns	@ 1.5 V

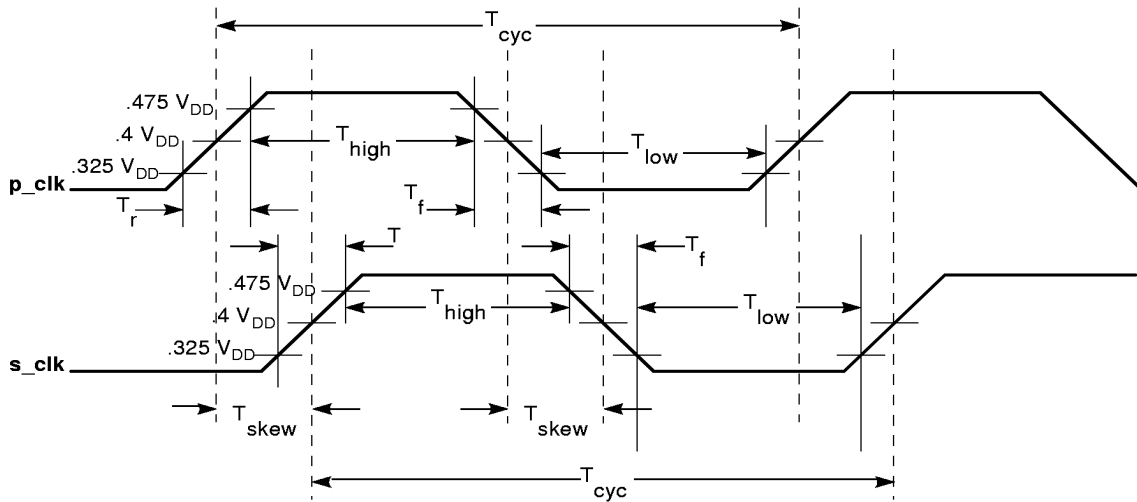
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**Table 7-3 (Cont.) p\_clk and s\_clk AC Timing**

Symbol	Parameter	Minimum	Maximum	Units	Notes
$T_{sclr}$	p_clk rising to s_clk_o<4:0> rising	0	5	ns	@1.5 V <sup>1</sup>
$T_{sclf}$	p_clk falling to s_clk_o<4:0> falling	0	5	ns	@1.5 V <sup>1</sup>

<sup>1</sup>Measured with 30 pF lumped load.

**Figure 7-2 p\_clk and s\_clk AC Timing**



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### 7.2.3 Input Signal AC Timing Specifications

Table 7–4 and Figure 7–3 show the input signal ac timings, and Table 7–5 shows the timing specifications for **xrst\_l**.

**Table 7–4 Input Signal AC Timings**

Symbol	Parameter	Minimum	Maximum	Units
$T_{val}$	<b>xclk</b> -to- <b>xsignal</b> valid delay— bused signals <sup>1, 2, 3</sup>	2	11	ns
$T_{val}$ (ptp)	<b>xclk</b> -to- <b>xsignal</b> valid delay— point-to-point <sup>1, 2, 3</sup>	2	12	ns
$T_{on}$	Float-to-active delay <sup>1</sup>	2	–	ns
$T_{off}$	Active-to-float delay <sup>1</sup>	–	28	ns
$T_{su}$	Input setup time to <b>xclk</b> — bused signals <sup>1, 3</sup>	7	–	ns
$T_{su}$ (ptp)	Input setup time to <b>xclk</b> — point-to-point <sup>1, 3</sup>	10, 12	–	ns
$T_h$	Input signal hold time from <b>xclk</b> <sup>1</sup>	0	–	ns

<sup>1</sup>All primary interface signals are used by **p\_clk** and all secondary interface signals are used by **s\_clk**.

<sup>2</sup>Minimum times measured with 0-pF equivalent load. Maximum times measured with 50-pF equivalent load.

<sup>3</sup>Point-to-point signals are **p\_req\_l**, **s\_req\_l<3:0>**, **p\_gnt\_l**, **s\_gnt\_l<3:0>**, and **s\_cfn\_l**. All other PCI signals are shared. All **xgnt\_l** signals and **s\_cfn\_l** have a setup time of 10 ns. **xreq\_l** has a setup time of 12 ns.

Figure 7-3 AC Timing Waveforms

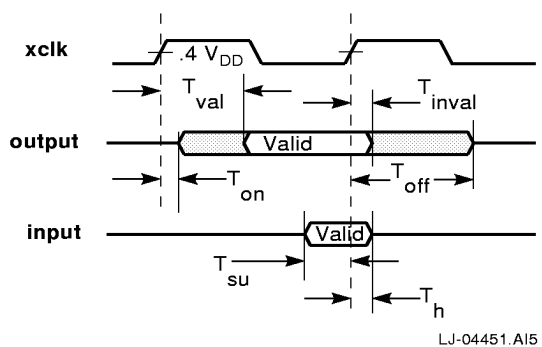


Table 7-5 xrst\_l Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
$T_{prot}$	<b>p_rst_l</b> active time after power stable	1	–	$\mu$ s
$T_{prot-clk}$	<b>p_rst_l</b> active time after <b>p_clk</b> stable	100	–	$\mu$ s
$T_{prot-off}$	<b>p_rst_l</b> active to output float delay	–	40	ns
$T_{srst}$	<b>s_rst_l</b> active after <b>p_rst_l</b> assertion	–	40	ns
$T_{srst-on}$	<b>s_rst_l</b> active time after <b>s_clk</b> stable	100	–	$\mu$ s
$T_{srst-off}$	<b>s_rst_l</b> active to secondary output float delay	–	40	ns