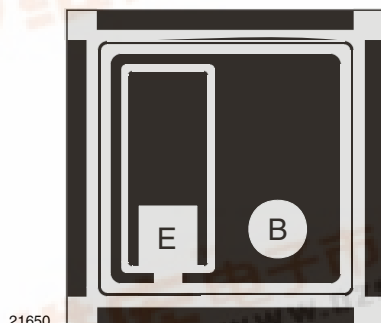


Silicon NPN Phototransistor



FEATURES

- Package type: chip
- Package form: single chip
- Dimensions (L x W x H in mm): 0.53 x 0.53 x 0.185
- High photo sensitivity
- High radiant sensitivity
- Suitable for visible and near infrared radiation
- Fast response times
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC



RoHS
COMPLIANT

DESCRIPTION

T1090P is a silicon NPN phototransistor chip with high radiant sensitivity, sensitive to visible and near infrared radiation.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY

COMPONENT	I_{ca} (mA)	φ (deg)	$\lambda_{0.1}$ (nm)
T1090P	0.43 to 0.77	± 60	440 to 1070

Note

Test condition see table "Basic Characteristics"

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T1090P-SD-F	Wafer sawn on foil with disco frame	MOQ: 50 000 pcs	Chip

Note

MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Collector emitter voltage		V_{CEO}	70	V
Emitter collector voltage		V_{ECO}	5	V
Collector current		I_C	50	mA
Junction temperature		T_j	100	$^{\circ}\text{C}$
Operating temperature range		T_{amb}	- 40 to + 100	$^{\circ}\text{C}$
Storage temperature range		T_{stg1}	- 40 to + 100	$^{\circ}\text{C}$
Storage temperature range on foil		T_{stg2}	- 40 to + 50	$^{\circ}\text{C}$

Note

$T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified

BASIC CHARACTERISTICS ⁽¹⁾

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Collector emitter breakdown voltage	$I_C = 1 \text{ mA}$	$V_{(BR)CEO}$	70			V
Collector emitter dark current	$V_{CE} = 20 \text{ V}, E = 0$	I_{CEO}		1		nA
Collector light current (Vishay selection type ³)	$E_e = 1 \text{ mW/cm}^2, \lambda = 950 \text{ nm},$ $V_{CE} = 5 \text{ V}$	I_{ca}	0.43		0.77	mA
Wavelength of peak sensitivity		λ_p		825		nm
Range of spectral bandwidth		$\lambda_{0.1}$		440 to 1070		nm
Rise time	$V_{CE} = 5 \text{ V}, I_C = 2 \text{ mA}, R_L = 100 \Omega$	t_r, t_f		4.3		μs
Fall time	$V_{CE} = 5 \text{ V}, I_C = 2 \text{ mA}, R_L = 100 \Omega$	t_r, t_f		7.7		μs

Note(1) $T_{amb} = 25^\circ\text{C}$, unless otherwise specified

(2) The measurements are based on samples of die which are mounted on a TO-header without resin coating

(3) Specific selection types possible

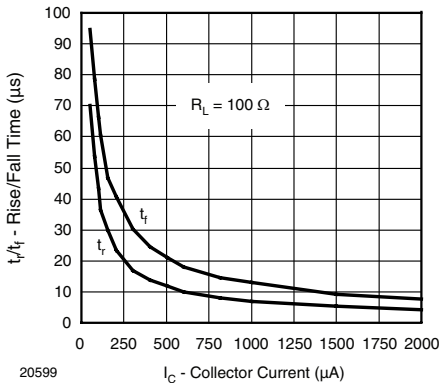
BASIC CHARACTERISTICS $T_{amb} = 25^\circ\text{C}$, unless otherwise specified

Fig. 1 - Rise/Fall Time vs. Collector Current

MECHANICAL DIMENSIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	L_x		0.52		mm
Length of chip edge (y-direction)	L_y		0.52		mm
Die height	H		0.185		mm
Diameter of bond pad base	d		0.1		mm
Bond pad emitter	a x b		0.1 x 0.1		mm ²

ADDITIONAL INFORMATION ⁽¹⁾

Frontside metallization, base (B), emitter (E)	Aluminum
Backside metallization, collector	AuSb
Dicing	Sawing
Die bonding technology	Epoxy bonding

Note

(1) All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.

The visual inspection shall be made in accordance with the "specification of visual inspection as referenced". The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification.

The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.

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