PMU for Embedded Camera Module

Check for Samples: TPS657052, TPS657051

FEATURES

- **Two 400mA Step-Down Converters**
- **Up to 92% Efficiency**
- **V_{IN} Range for DCDC Converter From 3.3V to 6V**
- **2.25 MHz Fixed Frequency Operation**
- **Power Save Mode at Light Load Current**
- **Output Voltage Accuracy in PWM Mode ±1.5%**
- **100% Duty Cycle for Lowest Dropout**
- **180° Out of Phase Operation**
- **1 General Purpose 200mA LDO**
- **V_{IN} Range for LDO From 1.7V to 6.0V**
- **Available in a 16 Ball WCSP With 0.5mm Pitch**

APPLICATIONS

- **Digital Cameras**
- **Portable Media Players**
- **Handheld Equipment**

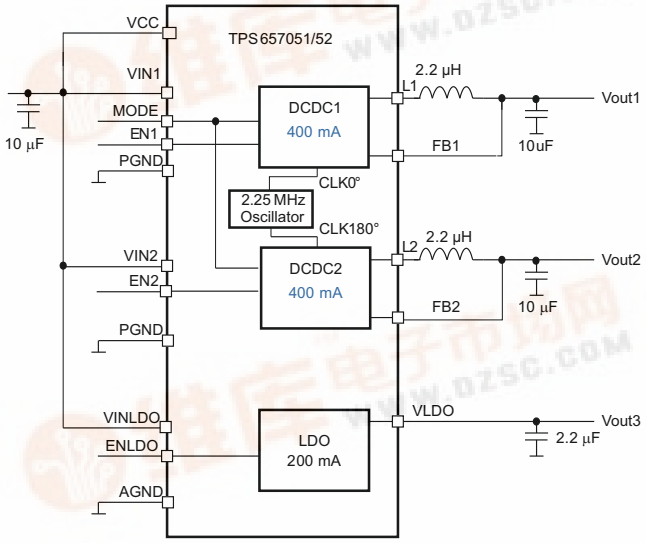


Figure 1. Application Circuit

DESCRIPTION

TPS657051/52 are small power management units targeted for embedded camera module or other portable low power consumer end equipments. It contains two high efficient step down converters, a low dropout linear regulator and additional supporting functions. The 2.25MHz step-down converter enters a low power mode at light load for maximum efficiency across the widest possible range of load currents. For low noise applications the devices can be forced into fixed frequency PWM mode using the MODE pin. The device allows the use of small inductors and capacitors to achieve a small sized solution. TPS657051/52 provides an output current of up to 400mA on both DCDC converters and integrates one 200mA LDO with different output settings. The LDO operates with an input voltage range between 1.7V and 6.0V allowing it to be supplied from the output of the step-down converter or directly from the system voltage.

The TPS657051/52 comes in a small 16-ball wafer chip scale package (WCSP) with 0.5mm ball pitch.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PART NO.(1)	SIZE FOR WCSP VERSION	OPTIONS	PACKAGE CODE	I2C	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS657051	D = 2076 µm ± 25 µm E = 2076 µm ± 25 µm	DCDC1 3.3V FIX, DCDC2 1.8 V FIX DCDC CONVERTERS 400mA, LDO VOUT 3.0V FIX, 200mA	YZH	N/A	WCSP	TPS657051
–40°C to 85°C	TPS657052	D = 2076 µm ± 25 µm E = 2076 µm ± 25 µm	DCDC1 3.3V FIX, DCDC2 1.8 V FIX DCDC CONVERTERS 400mA, LDO VOUT 2.8V FIX, 200mA	YZH	N/A	WCSP	TPS657052

(1) NO NOTE FOR PART NO IN SOURCE? FC

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

	VALUE / UNIT
Input voltage range on all pins except A/PGND pins with respect to AGND	–0.3 to 7 V
Voltage range on pin VLDO1 with respect to AGND	–0.3 to 3.6 V
Current at L1, VLDO1, VINLDO1, PGND	600 mA
Current at AGND	20 mA
Current at all other pins	3 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A	–40°C to 85°C
Maximum junction temperature, T_J	125°C
Storage temperature, T_{ST}	–65°C to 150°C

DISSIPATION RATINGS

DEVICE	PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATI4NG	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
TPS657051/52(1)	YZH	185	540mW	5.4mW	297mW	216mW
TPS657051/52(2)	YZH	75	1.3W	13.3mW	0.7W	0.5W

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN1/2}$	Input voltage range for step-down converter DCDC1and DCDC2	3.3		6.0	V
$I_{OUTDCDC1/2}$	Output current at L			400	mA
L	Inductor at L	1.5	2.2	4.7	µH
V_{INLDO}	Input voltage range for LDO	1.7		6.0	V
I_{LDO}	Output current at LDO			200	mA
$C_{INDCDC1/2}$	Input Capacitor at V_{IN1} and V_{IN2}	4.7			µF
$C_{OUTDCDC1/2}$	Output Capacitor at V_{OUT1}, V_{OUT2}	4.7	10	22	µF
C_{INLDO}	Input Capacitor at V_{INLDO}	2.2			µF
C_{OUTLDO}	Output Capacitor at V_{LDO}	2.2			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: V_{IN1}=V_{IN2}=V_{INLDO}=3.6 V, L=LQMP21P 2.2µH, $C_{OUTDCDCx}$ = 10µF, C_{OUTLDO} =2.2µF, T_A = –40°C to +85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating quiescent current DCDCx	DCDC1 and DCDC2 enabled, I_{OUT} = 0 mA, MODE =0 (PFM mode), LDO disabled		40		µA
		DCDC1 or DCDC2 enabled, I_{OUT} = 0 mA, MODE =0 (PFM mode), LDO disabled		25		µA
		DCDC1 or DCDC2 enabled, I_{OUT} = 0 mA. MODE =1 (forced PWM mode), LDO disabled		4		mA
	Operating quiescent current LDO	DCDC1 and DCDC2 disabled, LDO enabled. IOUT = 0mA		25	37	µA
I_{SD}	Shutdown current	DCDC1, DCDC2, and LDO disable		5	12	µA
DIGITAL PINS (EN1, EN2, ENLDO, MODE)						
V_{IH}	High level input voltage for EN1, EN2, ENLDO, MODE		1.2		VCC	V
V_{IL}	Low level input voltage for EN1, EN2, ENLDO, MODE				0.4	V
I_{LKG}	Input leakage current	EN1, EN2, ENLDO, MODE tied to GND or V_{IN} = V_{IN2}		0.01	0.10	µA
STEP-DOWN CONVERTERS						
V_{IN1}	Input voltage for DCDC1		3.3		6.0	V
V_{IN2}	Input voltage for DCDC2		3.3		6.0	V
UVLO	Internal undervoltage lockout threshold	V_{IN1} = V_{IN2} falling	2.15	2.2	2.25	V
	Internal undervoltage lockout threshold hysteresis	V_{IN1} = V_{IN2} rising		120		mV

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted: V_{IN1}=V_{IN2}=V_{INLDO}=3.6 V, L=LQMP21P 2.2µH, $C_{OUTDCDCx}$ = 10µF, C_{OUTLDO} =2.2µF, T_A = –40°C to +85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN1} = V_{IN2} = 3.6 V		350	750	mΩ
	Low side MOSFET on-resistance	V_{IN1} = V_{IN2} = 3.6 V		350	600	mΩ
I_{LIMF}	Forward current limit	3.3V ≤ V_{IN1} = V_{IN2} ≤ 6.0 V	550	650	770	mA
$I_{OUTDCDC1/2}$	DCDC1/DCDC2 output current	V_{IN1} = V_{IN2} > 3.3 V , L = 2.2 µH			400	mA
OSCILLATOR						
f_{SW}	Oscillator frequency		2.03	2.25	2.48	MHz
OUTPUT						
V_{OUT1}	DCDC1 default output voltage	V_{IN1} = V_{IN2} ≥ 3.3 V		3.3		V
V_{OUT2}	DCDC2 default output voltage	V_{IN1} = V_{IN2} ≥ 3.3 V		1.8		V
I_{FB}	FB pin input current	DCDC converter disabled			0.1	µA
V_{OUT}	DC output voltage accuracy(1)	V_{IN1} = V_{IN2} = 3.3 V to 6.0 V, +1% voltage positioning active; PFM operation, 0 mA < I_{OUT} < I_{OUTMAX}		+1%	+3%	
	DC output voltage accuracy	V_{IN1} = V_{IN2} = 3.3 V to 6.0 V, PWM operation, 0 mA < I_{OUT} < I_{OUTMAX}	–1.5%		+1.5%	
	DC output voltage load regulation	PWM operation		0.5		%/A
t_{Start}	Start-up time	Time from active EN to Start switching		200		µs
t_{Ramp}	V_{OUT} ramp time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
R_{DIS}	Internal discharge resistor at L1 or L2 (TPS657051 Only)	DCDC1 or DCDC2 disabled	250	400	600	Ω
THERMAL PROTECTION SEPARATELY FOR DCDC1, DCDC2 AND LDO1						
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shudown hysteresis	Decreasing junction temperature		30		°C
VLDO, LOW DROPOUT REGULATOR						
V_{INLDO}	Input voltage range for LDO		1.7		6.0	V
V_{LDO}	TPS657051 LDO default output voltage(2)			3.0		V
V_{LDO}	TPS657052 LDO default output voltage(3)			2.8		V
I_O	Output current for LDO				200	mA
I_{SC}	LDO short circuit current limit	V_{LDO} = GND	340	400	550	mA
	Dropout voltage at LDO	I_O = 200 mA			200	mV
	Output voltage accuracy for LDO	I_O = 100 mA, V_{OUT} = 2.8V	–2%		+2%	
	Line regulation for LDO	V_{INLDO} = V_{LDO} + 0.5V (min. 1.7 V) to 6 V, I_O = 50 mA	–1%		1%	
	Load regulation for LDO	I_O = 1 mA to 200 mA for LDO	–1%		1%	
PSRR	Power supply rejection ratio	f_{NOISE} ≤ 10 kHz, C_{OUT} ≥ 2.2 µf Vin = 5.0 V, Vout = 2.8 V, IOUT = 100 mA		50		dB
Vn	Ouput noise voltage	Vout = 2.8 V, BW = 10Hz to 100kHz		160		µV RMS
t_{Ramp}	V_{OUT} ramp time	Internal soft-start when LDO is enabled; Time to ramp from 5% to 95% of V_{OUT}		200		µs
R_{DIS}	Internal discharge resistor at VLDO	LDO disabled	250	400	550	Ω

(1) In Power Save Mode (PFM), the internal reference voltage is 1.01 × Vref.
(2) VINLDO > 3.0V
(3) VINLDO > 2.8V

Chip Scale Version (YFF Package): PIN ASSIGNMENT (Top View – preliminary)

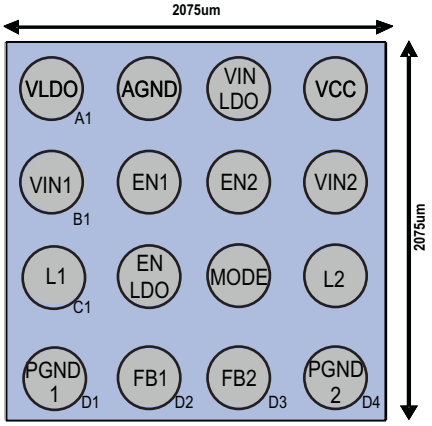


Figure 2. Preliminay Pin Out – Top View

Chip Scale Version (YFF Package): PIN ASSIGNMENT (Bottom View – preliminary)

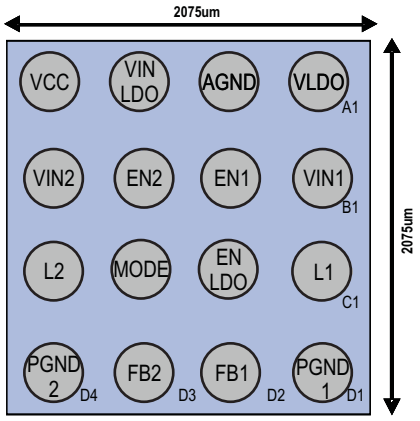
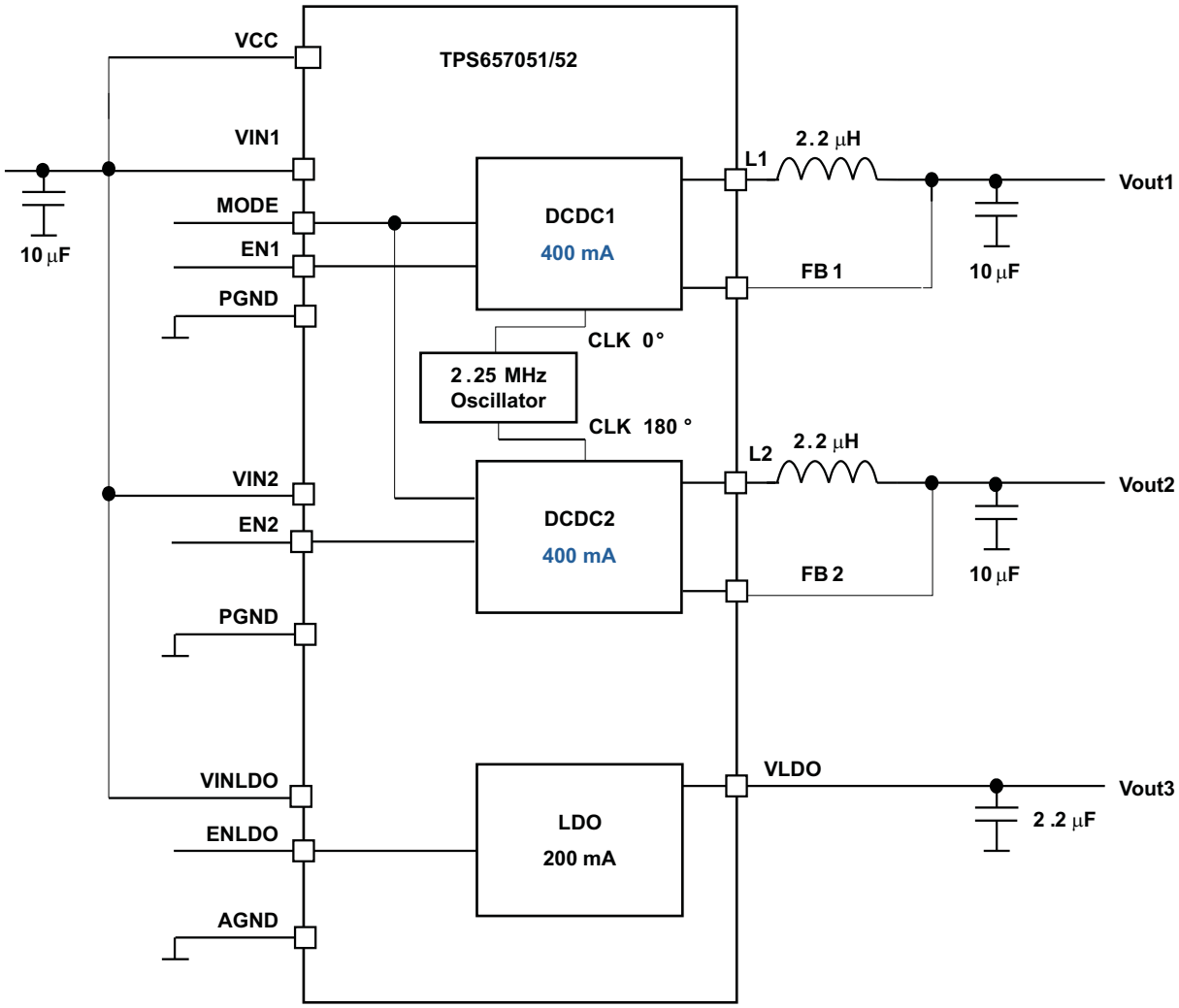


Figure 3. Preliminay Pin Out – Bottom View

FUNCTIONAL BLOCK DIAGRAM



Pin Functions for Chip Scale Version Based on Topview (YFF Package)

PIN		I/O	DESCRIPTION
NAME	NO.		
VCC	A4 (1)	I	Supply Input for internal reference, has to be connected to VIN1/ VIN2
AGND	A2		Analog ground
PGND1	D1		Power ground
PGND2	D4		Power ground
VIN2	B4 (2)	I	Input voltage pin for buck converter 2
VIN1	B1 (2)	I	Input voltage pin for buck converter 1
L1	C1	O	Switch output from buck converter 1
FB1	D2	I	Feedback input from buck converter 1
EN1	B2	I	Actively high enable input voltage for buck converter 1
L2	C4	O	Switch output from buck converter 2
FB2	D3	I	Feedback input from buck converter 2
EN2	B3	I	Actively high enable input voltage for buck converter 2
ENLDO	C2	I	Actively high enable input voltage for LDO
VINLDO	A3	I	Input voltage pin for LDO
VLDO	A1	O	Output voltage from LDO
MODE	C3	I	Set low to enable Power Save Mode. Pulling this PIN to high forces the device to operate in PWM mode over the whole load range.

(1) VCC has to be the highest input for device to function correctly.
(2) VIN1/VIN2 must be connected to VCC.

TYPICAL CHARACTERISTICS

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Efficiency DCDC (VDCDC= 1.8V), L = BRC1608 1.5 µH	vs Load current / PFM mode	Figure 6
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Line transient response DCDC 1.8V (PFM)	Scope plot	Figure 9
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Load transient reponse DCDC 1.8V (PWM) 20mA to 180mA	Scope plot	Figure 12
Load transient reponse DCDC 1.8V (PFM/PWM) 20mA to 360mA	Scope plot	Figure 13
Load transient response DCDC 1.8V (PWM) 20mA to 360mA	Scope plot	Figure 14
Load transient response LDO 2.8V	Scope plot	Figure 15
DCDC PFM to PWM mode transition	Scope plot	Figure 16
DCDC PWM to PFM mode transition	Scope plot	Figure 17
DCDC Output voltage ripple in PFM mode	Scope plot	Figure 18
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Startup timing DCDC 1.8V	Scope plot	Figure 20
Startup timing LDO 2.8V	Scope plot	Figure 21
LDO PSRR	Scope plot	Figure 22
DCDC Quiescent current	vs VINDCDC	Figure 23
LDO Quiescent current	vs VINDCDC	Figure 24
Shutdown current	vs VINDCDC	Figure 25

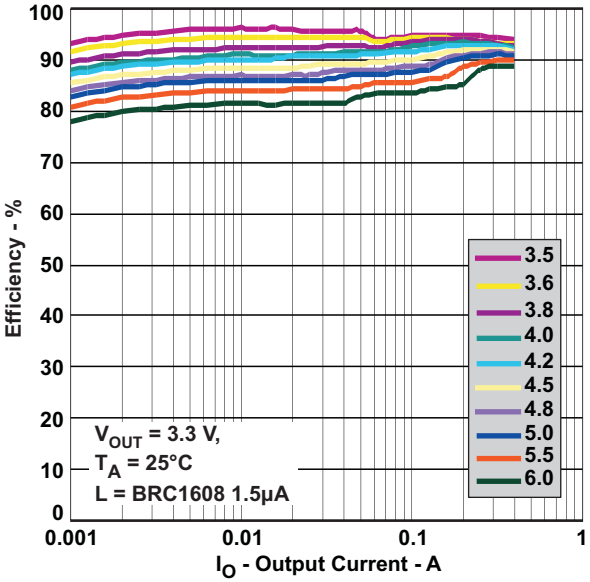


Figure 4. Efficiency DCDC (VDCDC=3.3V) vs Load Current PFM Mode

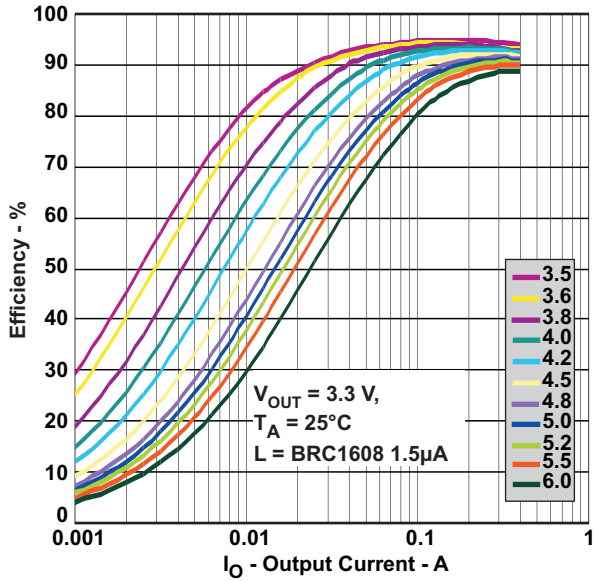


Figure 5. Efficiency DCDC (VDCDC=3.3V) vs Load Current PWM Mode

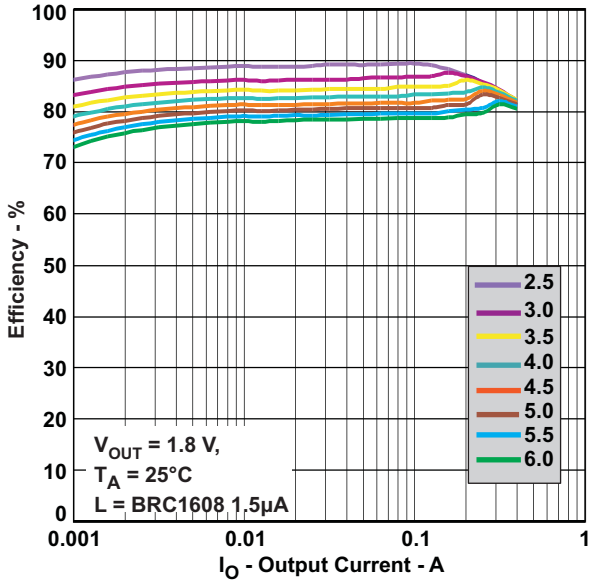


Figure 6. Efficiency DCDC (VDCDC=1.8V) vs Load Current PFM mode

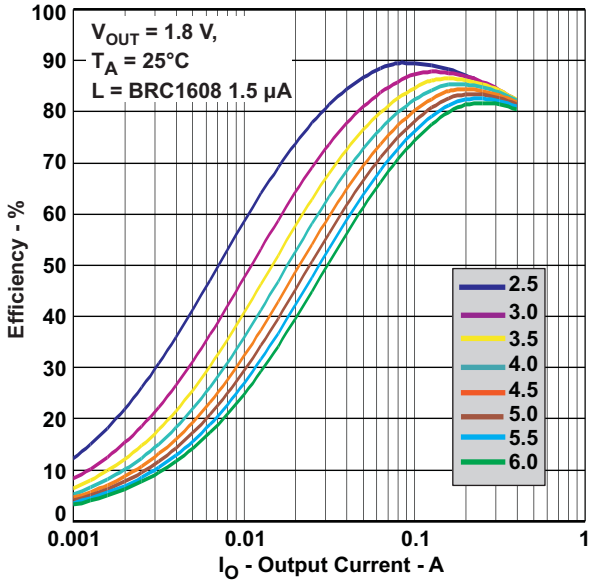


Figure 7. Efficiency DCDC (VDCDC=1.8V) vs Load Current PWM mode

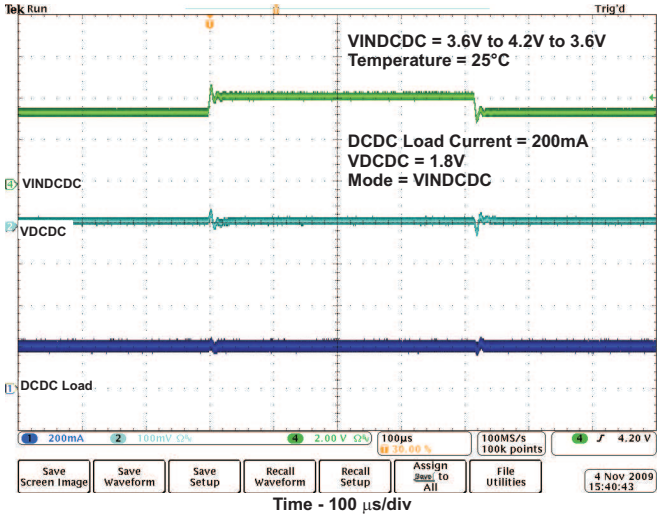


Figure 8. Line transient response DCDC 1.8V (PWM)

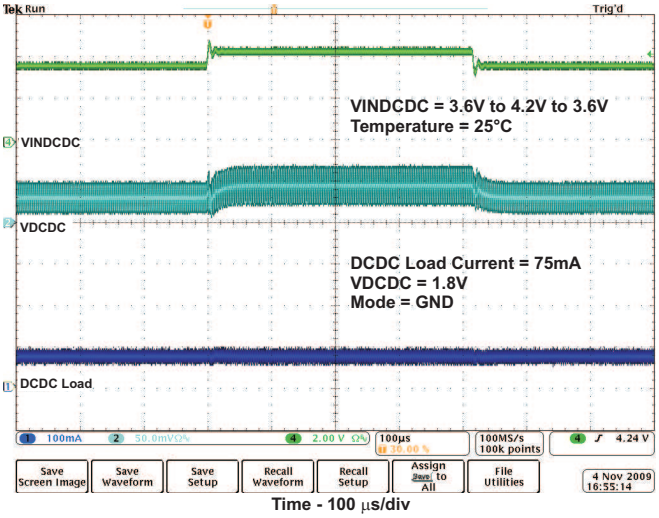


Figure 9. Line transient response DCDC 1.8V (PFM)

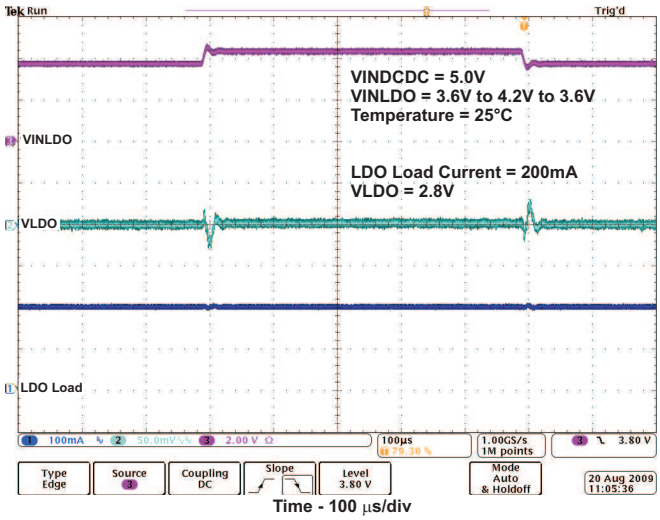


Figure 10. Line Transient Response LDO 2.8V

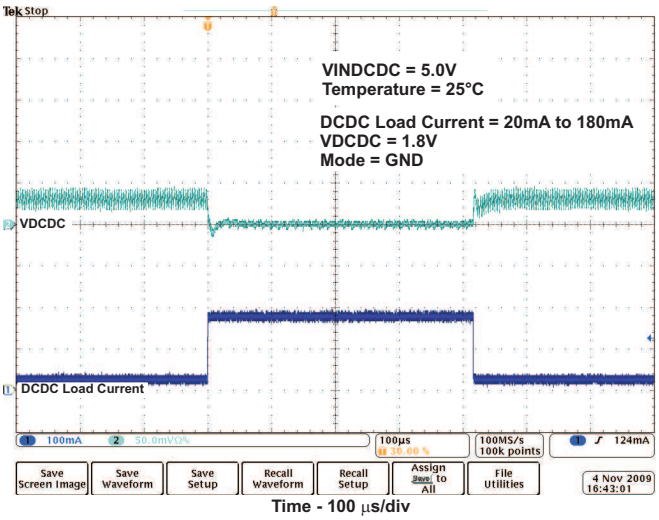


Figure 11. Load Transient Reponse DCDC 1.8V (PWM/PFM) 20mA to 180mA

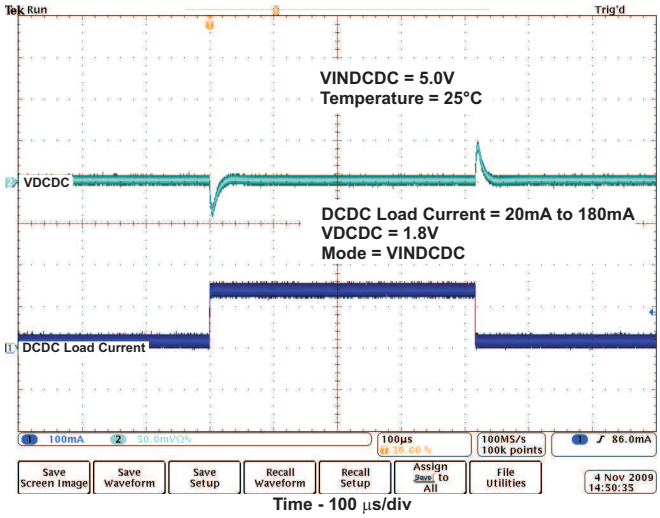


Figure 12. Load transient reponse DCDC 1.8V (PWM) 20mA to 180mA

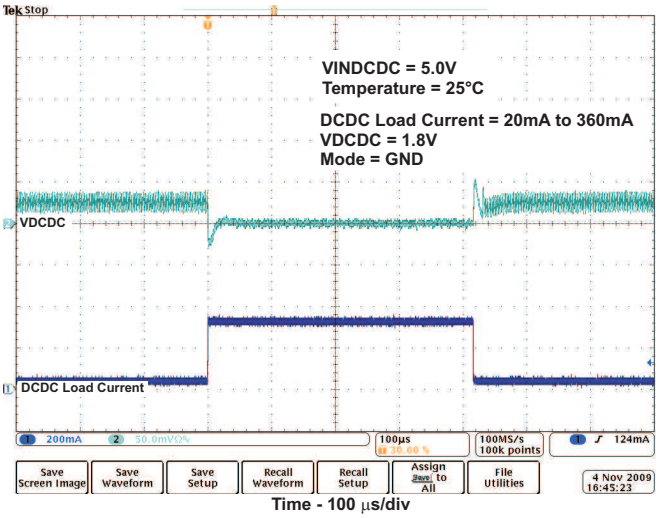


Figure 13. Load transient reponse DCDC 1.8V (PFM/PWM) 20mA to 360mA

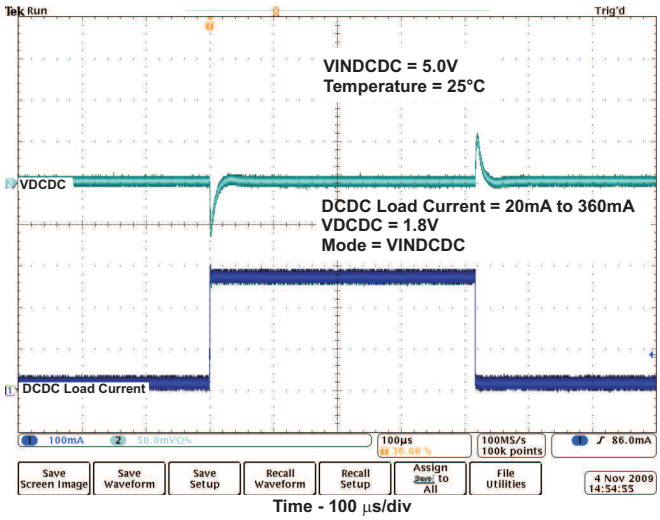


Figure 14. Load transient reponse DCDC 1.8V (PWM) 20mA to 360mA

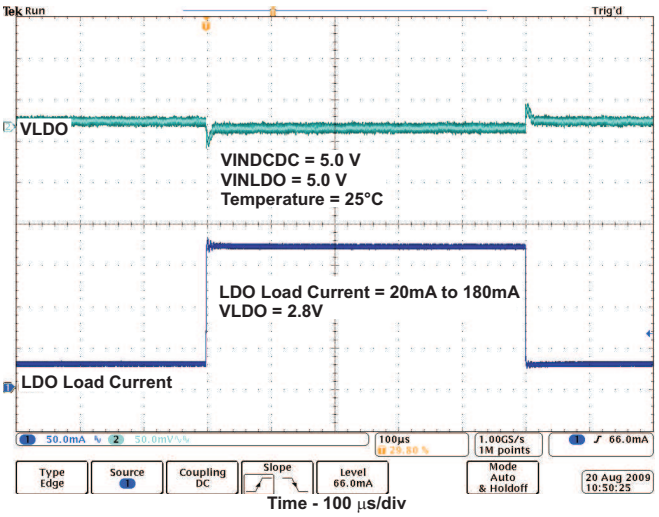


Figure 15. Load Transient Reponse LDO

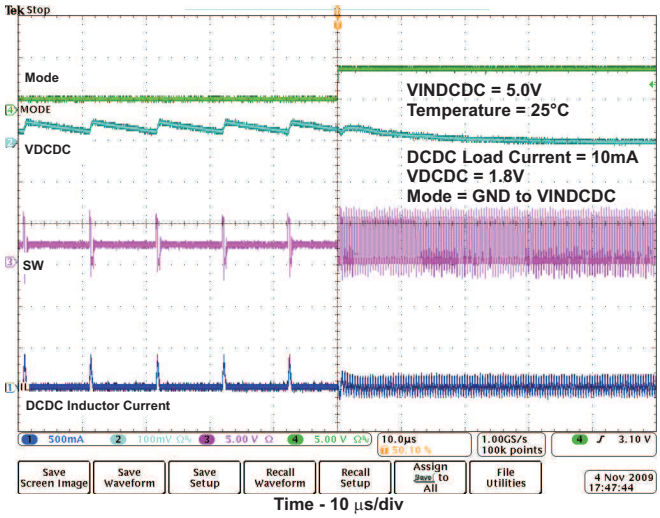


Figure 16. DCDC PFM to PWM Mode Transition

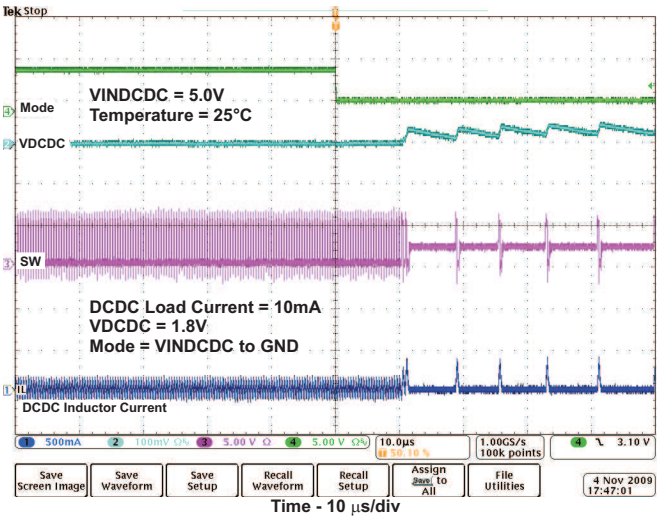


Figure 17. DCDC PWM to PFM Mode Transition

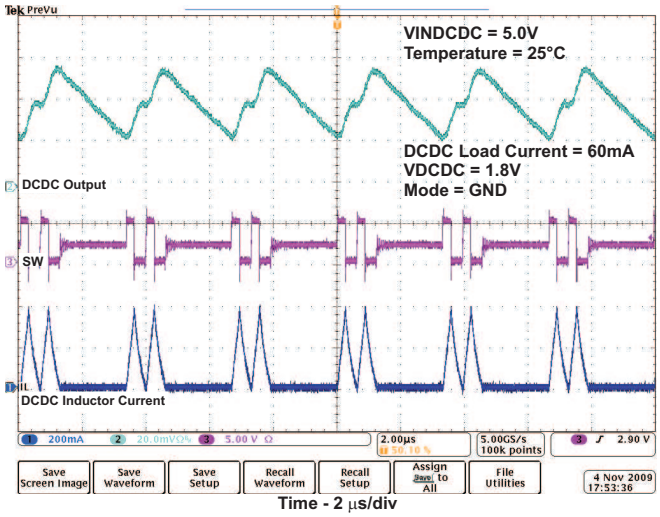


Figure 18. DCDC Output Voltage Ripple in PFM Mode

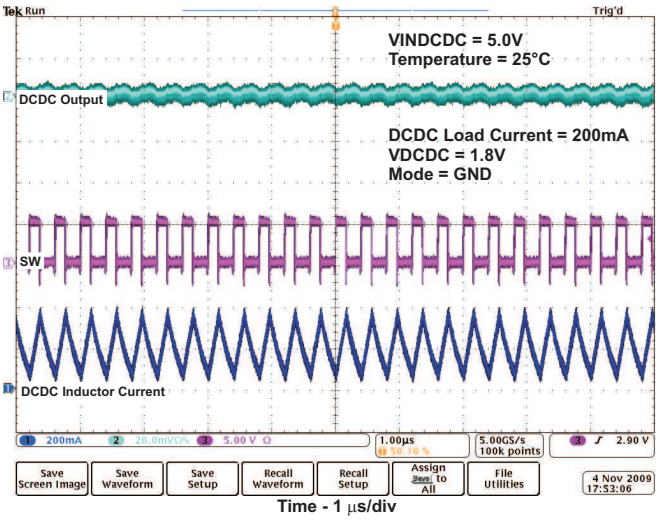


Figure 19. DCDC Output Voltage Ripple in PWM Mode

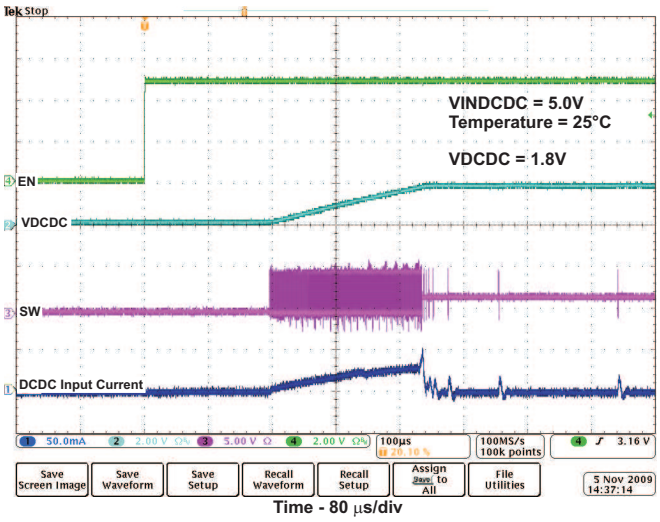


Figure 20. Startup Timing DCDC

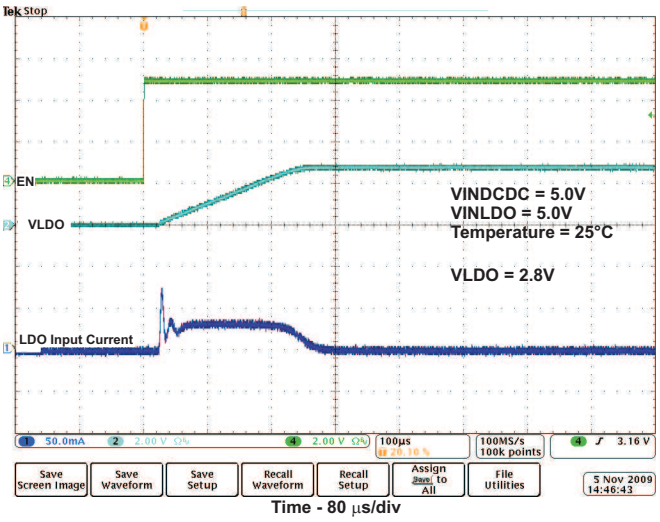


Figure 21. Startup Timing LDO

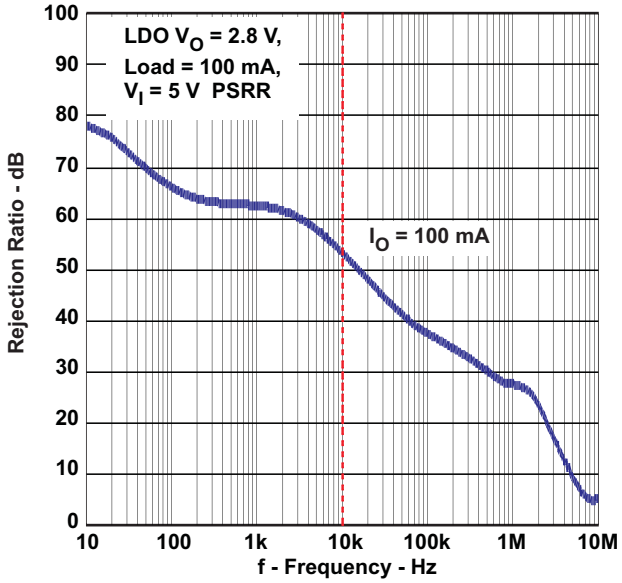


Figure 22. LDO PSRR

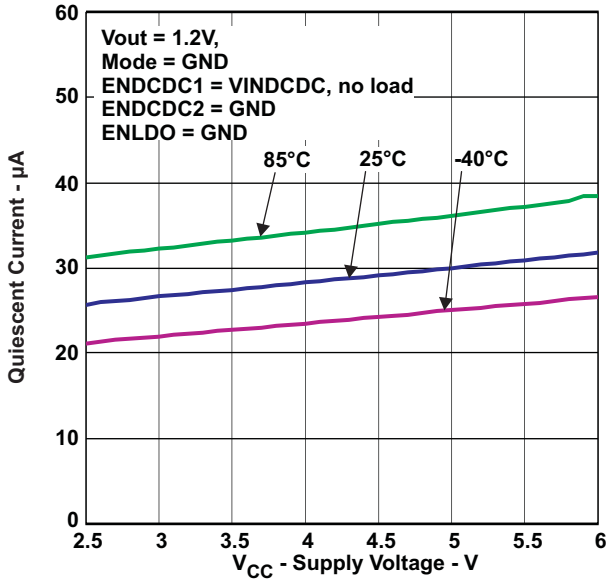


Figure 23. DCDC Quiescent Current

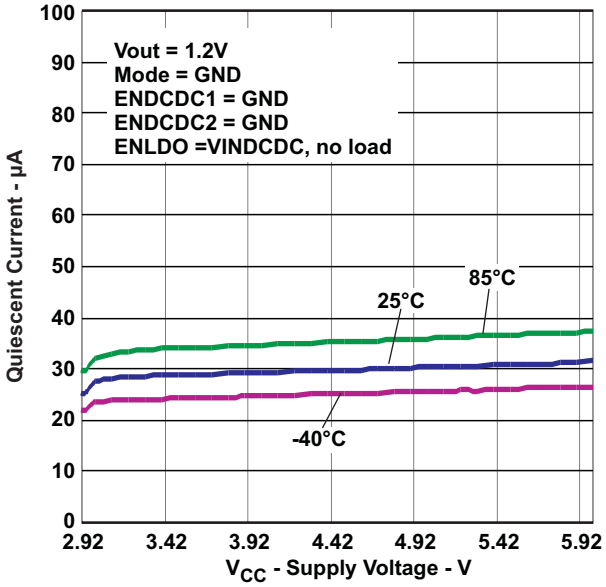


Figure 24. LDO Quiescent Current

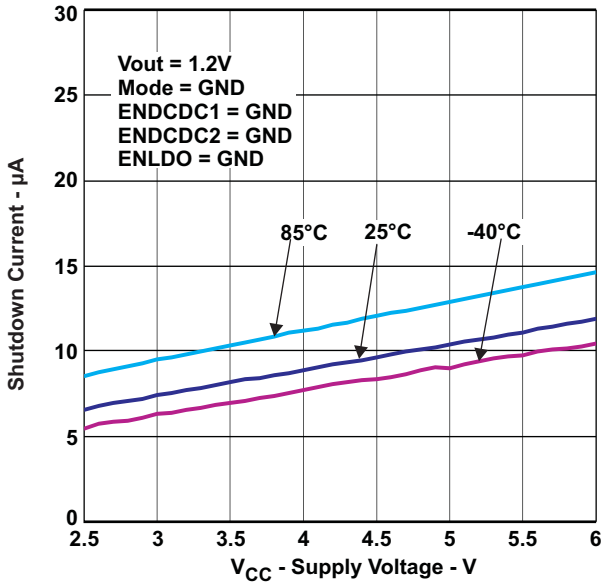


Figure 25. Shutdown Current

DETAILED DESCRIPTION

DCDC CONVERTER

The TPS6570521/52 step down converter operates with typically 2.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. With MODE pin set to low, at light load currents the converter can automatically enter Power Save Mode and operates then in PFM mode.

During PWM operation the converter use a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the High Side MOSFET switch is turned on. The current flows now from the input capacitor via the High Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the High Side MOSFET switch is exceeded. After an off time preventing shoot through current, the Low Side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the Low Side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the Low Side MOSFET rectifier and turning on the on the High Side MOSFET switch. The DCDC1 converter output voltage is set to 3.3V and the DCDC2 converter output voltage is set to 1.8V per default. A 180° phase shift between DCDC1 and DCDC 2 decreases the input RMS current and synchronizes the operation of the two DCDC converts. The FB pin must be directly connected to the output voltage of DCDC and no external resistor network must be connected.

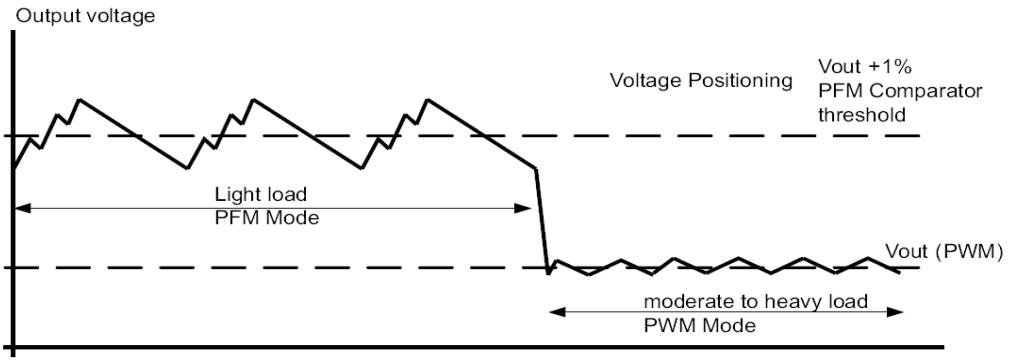
POWER SAVE MODE

The Power Save Mode is enabled with Mode Pin set to low. If the load current decreases, the converter will enter Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step. The transition from PWM mode to PFM mode occurs once the inductor current in the Low Side MOSFET switch becomes zero, which indicates discontinuous conduction mode. During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of VOUT nominal +1%, the device starts a PFM current pulse. The High Side MOSFET switch will turn on, and the inductor current ramps up. After the On-time expires, the switch is turned off and the Low Side MOSFET switch is turned on until the inductor current becomes zero. The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 25µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold. With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM Pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values. The PFM mode is left and PWM mode is entered in case the output current can not longer be supported in PFM mode. The Power Save Mode can be disabled by setting Mode pin to high. The converter will then operate in fixed frequency PWM mode.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in Power Save Mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.



Soft Start

The step-down converter in TPS657051/52 has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250s. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used.

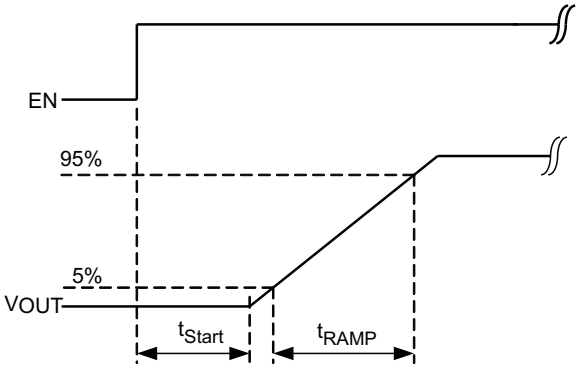


Figure 26. Soft Start

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the High Side MOSFET switch is turned on 100% for one or more cycles. With further decreasing VIN the High Side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{INmin} = V_{Omax} + I_{Omax} (R_{DS(on)}max + R_L)$$

With:

I_{Omax} = maximum output current plus inductor ripple current
$R_{DS(on)}$max = maximum high side switch RDSon.
R_L = DC resistance of the inductor
V_{Omax} = nominal output voltage plus maximum output voltage tolerance

180° OUT-OF-PHASE OPERATION

In PWM Mode the converters operate with a 180° turn-on phase shift of the PMOS (high side) transistors. This prevents the high-side switches of both converters from being turned on simultaneously, and therefore smooths the input current. This feature reduces the surge current drawn from the supply.

Under-Voltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the converters and LDOs. The under-voltage lockout threshold is typically 2.2V.

SHORT-CIRCUIT PROTECTION

All outputs are short circuit protected with a maximum output current as defined in the electrical specifications.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 150°C for the DCDC converter or LDO, the device goes into thermal shutdown. In this mode, the low side and high side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for the LDO or the DCDC converter will disable both power supplies simultaneously.

LDO

The low dropout voltage regulator is designed to operate well with low value ceramic input and output capacitors. It operates with input voltages down to 1.7V. The LDO offers a maximum dropout voltage of 200mV at rated output current. The LDO supports a current limit feature.

ENABLE FOR DCDC1, DCDC2 AND LDO

Disabling the DCDC converter or LDO, forces the device into shutdown, with a shutdown quiescent current as defined in the electrical characteristics. In this mode, the power FETs are turned-off and the entire internal control circuitry is switched-off.

APPLICATION INFORMATION

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

Inductor selection

The converter operates typically with 2.2µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductor will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 1. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

With:

f = Switching Frequency (2.25MHz typical)
L = Inductor Value
ΔI_L = Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

The highest inductor current will occur at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Notice that the step down converter has internal loop compensation. As the internal loop compensation is designed to work with a certain output filter corner frequency calculated as follows:

$$f_c = \frac{1}{2\pi\sqrt{L \times Cout}} \quad \text{with } L = 2.2\ \mu H,\ Cout = 10\ \mu F \quad (3)$$

This leads to the fact the selection of external L-C filter has to be coped with the above formula. As a general rule of thumb the product of LxCout should be constant while selecting smaller inductor or increasing output capacitor value.

Refer to Table 1 and the typical applications for possible inductors.

Table 1. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
BRC1608	1.5 µH	Taiyo Yuden
MLP2012	2.2 µH	TDK
MIPSA2520	2.2 µH	FDK
LPS3015	2.2 µH	Coilcraft
LQM21P	2.2 µH	Murata

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the step-down converter allows the use of small ceramic capacitors with a typical value of 10µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. For an inductor value of 2.2µH, an output capacitor with 10µF can be used. Refer to recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (5)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 2. Tested Capacitors

TYPE	COMPONENT SUPPLIER	VALUE	VOLTAGE RATING	SIZE	MATERIAL
DCDC Output Cap	Murata GRM155R60G475ME47D	4.7 µF	4 V	0402	Ceramic X5R
LDO Input/Output Cap	Murata GRM155R60J225ME15D	2.2 µF	6.3 V	0402	Ceramic X5R
DCDC Output Cap	Murata GRM188R60J475K	4.7 µF	6.3 V	0603	Ceramic X5R
DCDC Input/Output Cap	Murata GRM188R60J106M69D	10 µF	6.3 V	0603	Ceramic X5R

PACKAGING INFORMATION

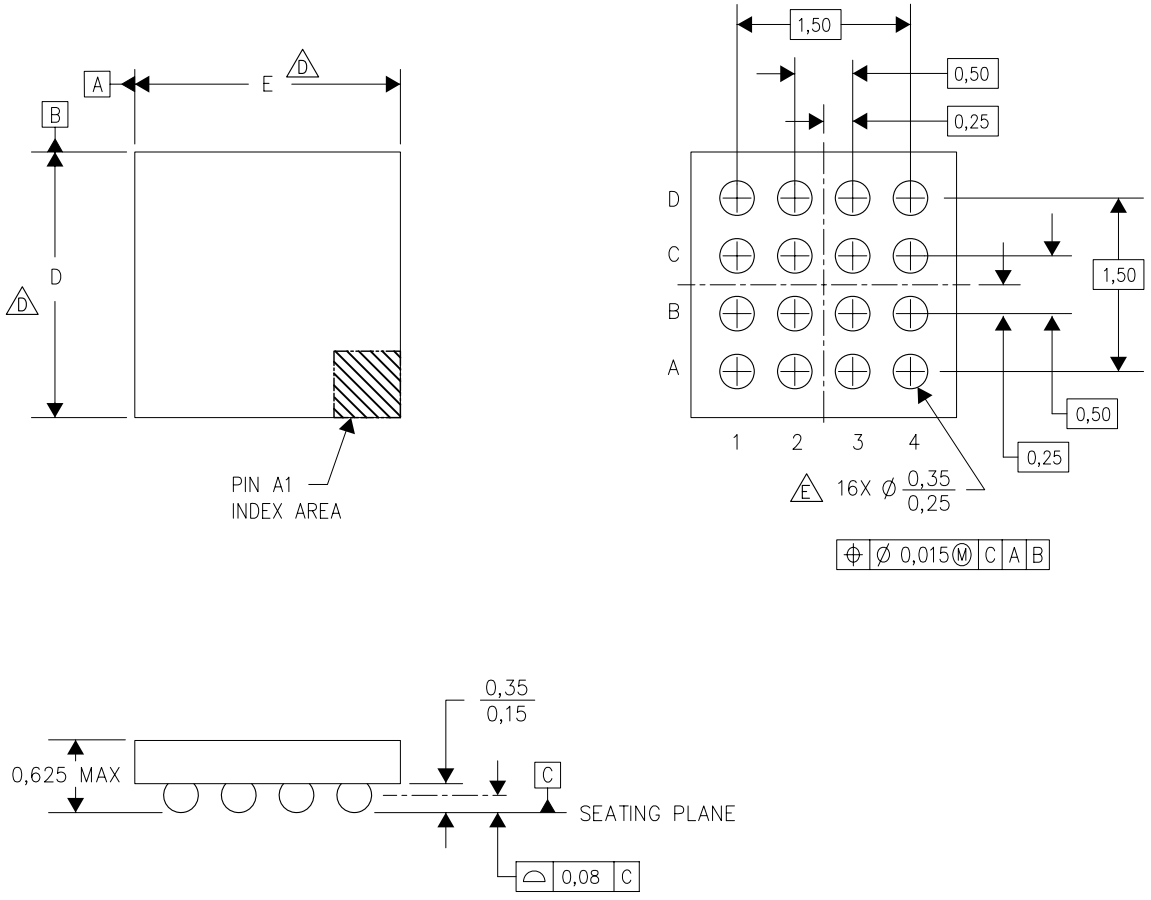
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS657051YZHR	ACTIVE	DSBGA	YZH	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS657051YZHT	ACTIVE	DSBGA	YZH	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS657052YZHR	ACTIVE	DSBGA	YZH	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS657052YZHT	ACTIVE	DSBGA	YZH	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

YZH (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



X: Max = 2086 µm, Min = 1986 µm

Y: Max = 2086 µm, Min = 1986 µm

4205060/D 06/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZH package can have dimension D ranging from 1.94 to 2.65 mm and dimension E ranging from 1.94 to 2.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 4 x 4 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEH (Drawing #4204183) for tin–lead (SnPb) balls.

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