REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Inactivate device type 02 for new design. Add device types 03 and 04. Alter electrical performance characteristics and associated waveforms. Editorial changes throughout.	89-04-24	Michael A. Frye
B	Add device types 05 and 06. Change minimum limits for device type 01, test numbers 10 and 27 and minimum limits for device type 04, test numbers 41 and 62 in table I. Correct vendor CAGE number and vendor address. Editorial changes throughout . - tvn	98-06-01	Monica L. Poelking

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					

REV STATUS OF SHEETS																	
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

PREPARED BY
Greg A. Pitz

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-02-25

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, CMOS, MICROPROCESSOR OPTIMIZED FOR DIGITAL SIGNAL PROCESSING, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87735

SHEET 1 OF 29

DSCC FORM 2233
APR 97

5962-E316-98

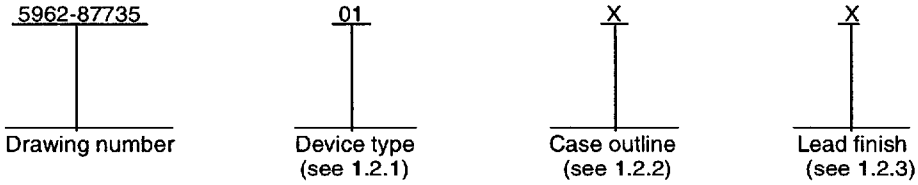
DISTRIBUTION STATEMENT A Approved for public release; distribution is unlimited.

9004708 0036385 247

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	2100SG	Digital signal processor	6 MHz
02	2100TG	Digital signal processor	8 MHz
03	2100ASG	Digital signal processor	8 MHz
04	2100ATG	Digital signal processor	10 MHz
05	2100AUG	Digital signal processor	12 MHz
06	2100AVG	Digital signal processor	16 MHz

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA17-P100	100	Pin grid array

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.3 V dc to +7 V dc
Input voltage ..... -0.3 V dc to V_{CC} + 0.3 V dc
Output voltage swing ..... -0.3 V dc to V_{CC} + 0.3 V dc
Maximum power dissipation (P_D) ..... 0.750 W
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-PRF-38535
Junction temperature (T_J) ..... +165°C

1.4 Recommended operating conditions.

Operating supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Test circuit and waveforms. The test circuit and waveforms are as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level input voltage 1/	V_{IH1}	V_{CC} = maximum	All	1, 2, 3	2.2		V
	V_{IH2}	V_{CC} = maximum, at CLKIN	03,04, 05,06	1, 2, 3	2.4		
Low level input voltage 1/	V_{IL}	V_{CC} = minimum	All	1, 2, 3		0.8	
High level output voltage 2/	V_{OH}	V_{CC} = minimum, I_{OH} = -1 mA	All	1, 2, 3	2.4		V
Low level output voltage 2/	V_{OL}	V_{CC} = minimum, I_{OL} = 4 mA	All	1, 2, 3		0.6	
High level input current 3/	I_{IH}	V_{CC} = maximum, V_{IN} = 5.0 V	All	1, 2, 3		10	µA
Low level input current 3/	I_{IL}	V_{CC} = maximum, V_{IN} = 0.0 V	All	1, 2, 3		10	
Three-state leakage current 4/	I_{OZH}	V_{CC} = maximum V_{IN} = V_{CC} maximum 5/	All	1, 2, 3		10	µA
Three-state leakage current 6/	I_{OZL}	V_{CC} = maximum V_{IN} = 0.0 V 5/	All	1, 2, 3		10	
Three-state pull-up leakage current 7/	I_{OZL}	V_{CC} = maximum V_{IN} = 0.0 V 5/	01,02,03	1, 2, 3		150	
			04,05,06			180	
Supply current (power down) 8/	I_{CC}	V_{CC} = maximum V_{IN} = 0.0 V 5/ 7/	All	1, 2, 3		15	mA
Supply current (dynamic)	I_{CC}	V_{CC} = maximum maximum clock rate 9/	01	1, 2, 3		100	
			02,03			130	
			04			180	
			05,06			200	
Input capacitance	C_{IN}	See 4.3.1c V_{IN} = 200 mV T_C = +25°C f_{IN} = 100 kHz	All	4		10	pF
Functional test		See 4.3.1d	All	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Clock signals		See figure 3 and table III					
CLKIN period 10/	1	A	01	9, 10, 11	40.5		ns
			02,03		30.5		
			04		24.4		
			05		20.0		
			06		15.0		
CLKIN width low	2	A	01	9, 10, 11	11		ns
			02,03		8		
			04		7		
			05		4		
			06		3		
CLKIN width high	3	A	01	9, 10, 11	18		ns
			02,03		12		
			04		9		
			05		8		
			06		4		
CLKIN low (3-4) to CLKOUT low	4	B	01	9, 10, 11		34	ns
			02,03			29	
			04			24	
			05			22	
			06			17	
CLKIN low (7-8) to CLKOUT high	5	B	01	9, 10, 11		24	ns
			02,03			20	
			04			20	
			05			18	
			06			14	
CLKOUT width low 11/	6	A	01	9, 10, 11	60		ns
			02,03		45		
			04		36		
			05		28		
			06		22		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Control signals		See figure 3 and table III					
$\overline{\text{RESET}}$ low to CLKIN high	7	B	All	9, 10, 11	2		ns
CLKIN high to $\overline{\text{RESET}}$ high 11/	8	B	01	9, 10, 11	6	36	ns
			02,03		6	26	
			04		4	20	
			05		4	16	
			06		4	11	
$\overline{\text{RESET}}$ width low 11/	9	A	01	9, 10, 11	170		ns
			02,03		128		
			04		98		
			05		80		
			06		60		
$\overline{\text{HALT}}$ valid to CLKIN low (3-4)	10	B	All	9, 10, 11	2		ns
CLKIN low (3-4) to $\overline{\text{HALT}}$ invalid	11	B	01	9, 10, 11	12		ns
			02,03,04		10		
			05		8		
			06		6		
CLKIN low (7-8) to TRAP valid	12	B	01	9, 10, 11		25	ns
			02,03			20	
			04			18	
			05			16	
			06			13	
CLKIN low (7-8) to $\overline{\text{IRQ}}$ valid	13	B	All	9, 10, 11		1	ns
CLKIN low (7-8) to $\overline{\text{IRQ}}$ invalid	14	B	01	9, 10, 11	21		ns
			02,03		17		
			04,05		14		
			06		10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
BUS request/grant		See figure 3 and table III					
$\overline{BR}$ valid to CLKIN low (3-4)	15	B	01,02,03	9, 10, 11	1		ns
			04,05		4		
			06		1		
CLKIN low (3-4) to $\overline{BR}$ invalid	16	B	01	9, 10, 11	10		ns
			02,03,04		7		
			05,06		4		
CLKIN low (3-4) to $\overline{BG}$ low	17	B	01	9, 10, 11		38	ns
			02,03			30	
			04			26	
			05			24	
			06			18	
CLKIN low (7-8) to $\overline{BG}$ high	18	B	01	9, 10, 11		31	ns
			02,03			25	
			04			24	
			05			20	
			06			18	
$\overline{BG}$ low to xMxx disable 12/	19	C	01	9, 10, 11		22	ns
			02,03			17	
			04,05			16	
			06			13	
xMxx enable to $\overline{BG}$ high 12/	20	D	01	9, 10, 11		12	ns
			02,03,04			10	
			05			8	
			06			2	
$\overline{BR}$ low to $\overline{BG}$ low during $\overline{RESET}$	21	A	01	9, 10, 11		28	ns
			02,03			23	
			04			18	
			05			16	
			06			13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
BUS request/grant - continued		See figure 3 and table III					
$\overline{BR}$ high to $\overline{BG}$ high during $\overline{RESET}$	22	A	01	9, 10, 11		21	ns
			02,03			18	
			04			16	
			05			14	
			06			11	
Program memory		See figure 3 and table III					
$\overline{PMRD}$ width low 11/	23	A	01	9, 10, 11	60		ns
			02,03		45		
			04		36		
			05		28		
			06		22		
PMA valid to $\overline{PMRD}$ low 11/	24	A	01	9, 10, 11	18		ns
			02,03		14		
			04		6		
			05,06		4		
$\overline{PMRD}$ high to PMA invalid 11/	25	A	01	9, 10, 11	20		ns
			02,03		10		
			04		8		
			05,06		6		
PMDA valid to $\overline{PMRD}$ low 11/	26	A	01	9, 10, 11	41		ns
			02,03		24		
			04		20		
			05,06		15		
$\overline{PMRD}$ high to PMDA invalid 11/	27	A	01	9, 10, 11	18		ns
			02,03		12		
			04		10		
			05,06		9		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Program memory - continued		See figure 3 and table III					
$\overline{PMS}$ valid to $\overline{PMRD}$ low 11/	28	A	01	9, 10, 11	55		ns
			02,03		40		
			04		32		
			05,06		26		
$\overline{PMRD}$ high to $\overline{PMS}$ invalid 11/	29	A	01	9, 10, 11	16		ns
			02,03,04		8		
			05,06		6		
$\overline{PMRD}$ low to PMD in valid 11/	30	A	01	9, 10, 11		45	ns
			02,03			33	
			04			28	
			05			18	
			06			14	
PMA valid to PMD in valid 11/	31	A	01	9, 10, 11		57	ns
			02,03			50	
			04			46	
			05			32	
			06			29	
$\overline{PMS}$ valid to PMD in valid 11/	32	A	01	9, 10, 11		90	ns
			02,03			65	
			04			50	
			05			35	
			06			45	
$\overline{PMRD}$ high to PMD in invalid	33	A	All	9,10, 11	0		ns
$\overline{PMWR}$ width low 11/	34	A	01	9, 10, 11	60		ns
			02,03		45		
			04		36		
			05		28		
			06		22		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Program memory - continued		See figure 3 and table III					
PMA valid to $\overline{PMWR}$ low 11/	35	A	01	9, 10, 11	16		ns
			02,03		12		
			04		8		
			05,06		4		
$\overline{PMWR}$ high to PMA invalid 11/	36	A	01	9, 10, 11	19		ns
			02,03		10		
			04		8		
			05,06		6		
PMDA valid to $\overline{PMWR}$ low 11/	37	A	01	9, 10, 11	39		ns
			02,03		28		
			04		20		
			05,06		16		
$\overline{PMWR}$ high to PMDA invalid 11/	38	A	01	9, 10, 11	21		ns
			02,03		12		
			04		10		
			05,06		8		
$\overline{PMS}$ valid to $\overline{PMWR}$ low 11/	39	A	01	9, 10, 11	54		ns
			02,03		40		
			04		32		
			05,06		26		
$\overline{PMWR}$ high to $\overline{PMS}$ invalid 11/	40	A	01	9, 10, 11	14		ns
			02,03		8		
			04		6		
			05		4		
			06		6		
$\overline{PMWR}$ low to PMD out enable 11/	41	D	01	9, 10, 11	15		ns
			02,03		8		
			04		4		
			05		3		
			06		1		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Program memory - continued		See figure 3 and table III					
$\overline{PMWR}$ high to PMD out disable 11/	42	C	01	9, 10, 11		43	ns
			02,03			38	
			04			32	
			05			29	
			06			21	
$\overline{PMWR}$ low to PMD out valid 11/	43	A	01	9, 10, 11		40	ns
			02,03			32	
			04			29	
			05			26	
			06			14	
$\overline{PMWR}$ high to PMD out invalid 11/	44	A	01	9, 10, 11	21		ns
			02,03		12		
			04		10		
			05,06		8		
PMD out valid to $\overline{PMWR}$ high 11/	45	A	01	9, 10, 11	33		ns
			02,03		25		
			04		16		
			05,06		13		
Data memory		See figure 3 and table III					
$\overline{DMRD}$ width low 11/	46	A	01	9, 10, 11	60		ns
			02,03		45		
			04		36		
			05		28		
			06		22		
DMA valid to $\overline{DMRD}$ low 11/	47	A	01	9, 10, 11	21		ns
			02,03		14		
			04		6		
			05,06		4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data memory - continued		See figure 3 and table III					
$\overline{DMRD}$ high to DMA invalid 11/	48	A	01	9, 10, 11	19		ns
			02,03		10		
			04		8		
			05,06		6		
$\overline{DMS}$ valid to $\overline{DMRD}$ low	49	A	01	9, 10, 11	35		ns
			02,03		27		
			04		18		
			05		14		
			06		26		
$\overline{DMRD}$ high to $\overline{DMS}$ invalid	50	A	01	9, 10, 11	21		ns
			02,03		10		
			04		8		
			05,06		6		
$\overline{DMRD}$ low to DMACK valid 11/	51	A	01	9, 10, 11		31	ns
			02,03			21	
			04			16	
			05			10	
			06			5	
DMA valid to DMACK valid 11/	52	A	01	9, 10, 11		57	ns
			02,03			42	
			04			30	
			05,06			20	
$\overline{DMRD}$ low to DMD in valid 11/	53	A	01	9, 10, 11		55	ns
			02,03			37	
			04			28	
			05			18	
			06			14	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ Tc ≤ +125°C +4.5 V ≤ Vcc ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data memory - continued		See figure 3 and table III					
DMA valid to DMD in valid 11/	54	A	01	9, 10, 11		79	ns
			02,03			59	
			04			46	
			05			32	
			06			29	
$\overline{DMS}$ valid to DMD in valid	55	A	01	9, 10, 11		96	ns
			02,03			67	
			04			50	
			05			35	
			06			45	
$\overline{DMRD}$ high to DMD in invalid	56	A	All	9, 10, 11	0		ns
$\overline{DMWR}$ width low 11/	57	A	01	9, 10, 11	60		ns
			02,03		45		
			04		36		
			05		28		
			06		22		
DMA valid to $\overline{DMWR}$ low 11/	58	A	01	9, 10, 11	24		ns
			02,03		17		
			04		8		
			05,06		4		
$\overline{DMWR}$ high to DMA invalid 11/	59	A	01	9, 10, 11	19		ns
			02,03		10		
			04		8		
			05,06		6		
$\overline{DMS}$ valid to $\overline{DMWR}$ low	60	A	01	9, 10, 11	37		ns
			02,03		28		
			04		20		
			05		16		
			06		26		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data memory - continued		See figure 3 and table III					
$\overline{DMWR}$ high to $\overline{DMS}$ invalid	61	A	01	9, 10, 11	22		ns
			02,03		8		
			04		6		
			05		4		
			06		6		
$\overline{DMWR}$ low to DMD out enable 11/	62	D	01	9, 10, 11	14		ns
			02,03		8		
			04		4		
			05		3		
			06		1		
$\overline{DMWR}$ high to DMD out disable 11/	63	C	01	9, 10, 11		40	ns
			02,03			38	
			04			32	
			05			29	
			06			21	
$\overline{DMWR}$ low to DMD out valid 11/	64	A	01	9, 10, 11		38	ns
			02,03			32	
			04			29	
			05			26	
			06			14	
$\overline{DMWR}$ high to DMD out valid 11/	65	A	01	9, 10, 11	19		ns
			02,03		12		
			04		10		
			05,06		8		
DMD out valid to $\overline{DMWR}$ high 11/	66	A	01	9, 10, 11	33		ns
			02,03		25		
			04		16		
			05,06		13		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data memory - continued		See figure 3 and table III					
$\overline{DMWR}$ low to DMACK valid 11/	67	A	01	9, 10, 11		31	ns
			02,03			20	
			04			16	
			05			10	
			06			2.5	
DMACK width 11/	68	A	01	9, 10, 11	81		ns
			02,03		61		
			04		50		
			05		40		
			06		30		
DMACK low to CLKOUT high 11/	69	A	01	9, 10, 11	45		ns
			02,03		37		
			04		36		
			05		32		
			06		25		
CLKOUT low to DMACK high 11/	70	A	01	9, 10, 11		28	ns
			02,03			19	
			04			17	
			05			12	
			06			6	

1/ Applies to pins: PMD_{0-23}, DMD_{0-15}, $\overline{BR}$, $\overline{IRQ}_{0-3}$, DMACK, $\overline{RESET}$, $\overline{HALT}$, CLKIN (49 input pins).
2/ Applies to pins: PMA_{0-13}, $\overline{PMS}$, PMD_{0-23}, $\overline{PMRD}$, $\overline{PMWR}$, PMDA, $\overline{BG}$, DMA_{0-13}, $\overline{DMS}$, DMD_{0-15}, $\overline{DMRD}$, $\overline{DMWR}$, TRAP, CLKOUT (78 output pins).
3/ Applies to pins: $\overline{BR}$, $\overline{IRQ}_{0-3}$, DMACK, $\overline{RESET}$, $\overline{HALT}$, CLKIN (9 input only pins).
4/ Applies to pins: PMA_{0-13}, $\overline{PMS}$, PMD_{0-23}, $\overline{PMRD}$, $\overline{PMWR}$, PMDA, DMA_{0-13}, $\overline{DMS}$, DMD_{0-15}, $\overline{DMRD}$, $\overline{DMWR}$ (75 three-stateable pins).
5/ Additional test conditions: V_{IN} = 0 V on $\overline{BR}$ and $\overline{RESET}$, CLKIN active, forces three-state condition.
6/ Applies to pins: PMA_{0-13}, PMDA, DMA_{0-13}, (29 three-stateable pins without pullup).
7/ Applies to pins: PMD_{0-23}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, DMD_{0-15}, $\overline{DMS}$, $\overline{DMRD}$, $\overline{DMWR}$ (46 three-stateable pins with pullup).
8/ Power down refers to an idle state. While the device does not have any special standby or low-power mode, these conditions represent a low-power consumption state.
9/ Additional test conditions: Outputs loaded TTL loads with 100 pF capacitance, V_{IH} = 2.4 V, V_{IL} = 0.4 V, clock rate = 6.144 MHz for device type 01, 8.192 MHz for device types 02 and 03, 10.24 MHz for device type 04, 12.5 MHz for device type 05, 16.67 MHz for device type 06.
10/ Rise and fall times ≤ 5 ns.
11/ These items are cycle time dependent.
12/ xMxx refers to PMA_{0-13}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, PMDA, DMA_{0-13}, $\overline{DMS}$, $\overline{DMRD}$, and $\overline{DMWR}$.

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
A1	GND	B13	PMA1	G11	PMD6	M2	GND
A2	DMD5	C1	DMD10	G12	PMD7	M3	DMACK
A3	DMD4	C2	DMD9	G13	V_{CC}	M4	PMDA
A4	DMD2	C6	$\overline{IRQ0}$	H1	V_{CC}	M5	$\overline{DMS}$
A5	DMD0	C7	$\overline{IRQ2}$	H2	DMA8	M6	$\overline{DMWR}$
A6	GND	C8	PMA11	H3	DMA7	M7	$\overline{DMRD}$
A7	V_{CC}	C12	PMA2	H11	PMD9	M8	$\overline{BR}$
A8	PMA13	C13	PMA0	H12	PMD8	M9	$\overline{PMRD}$
A9	PMA10	D1	DMD12	H13	GND	M10	PMD22
A10	PMA8	D2	DMD11	J1	GND	M11	PMD19
A11	GND	D12	PMD0	J2	DMA6	M12	PMD17
A12	PMA5	D13	PMD1	J12	PMD11	M13	PMD16
A13	PMA3	E1	DMD14	J13	PMD10	N1	DMA0
B1	DMD8	E2	DMD13	K1	DMA5	N2	$\overline{RESET}$
B2	DMD7	E12	PMD2	K2	DMA4	N3	$\overline{HALT}$
B3	DMD6	E13	GND	K12	PMD13	N4	TRAP
B4	DMD3	F1	DMA12	K13	PMD12	N5	$\overline{PMS}$
B5	DMD1	F2	DMA13	L1	DMA3	N6	GND
B6	$\overline{IRQ1}$	F3	DMD15	L2	DMA1	N7	GND
B7	$\overline{IRQ3}$	F11	PMD3	L6	$\overline{PMWR}$	N8	V_{CC}
B8	PMA12	F12	PMD4	L7	CLKIN	N9	$\overline{BG}$
B9	PMA9	F13	PMD5	L8	CLKOUT	N10	PMD23
B10	PMA7	G1	DMA9	L12	PMD15	N11	PMD21
B11	PMA6	G2	DMA11	L13	PMD14	N12	PMD20
B12	PMA4	G3	DMA10	M1	DMA2	N13	PMD18

FIGURE 1. Terminal connections.

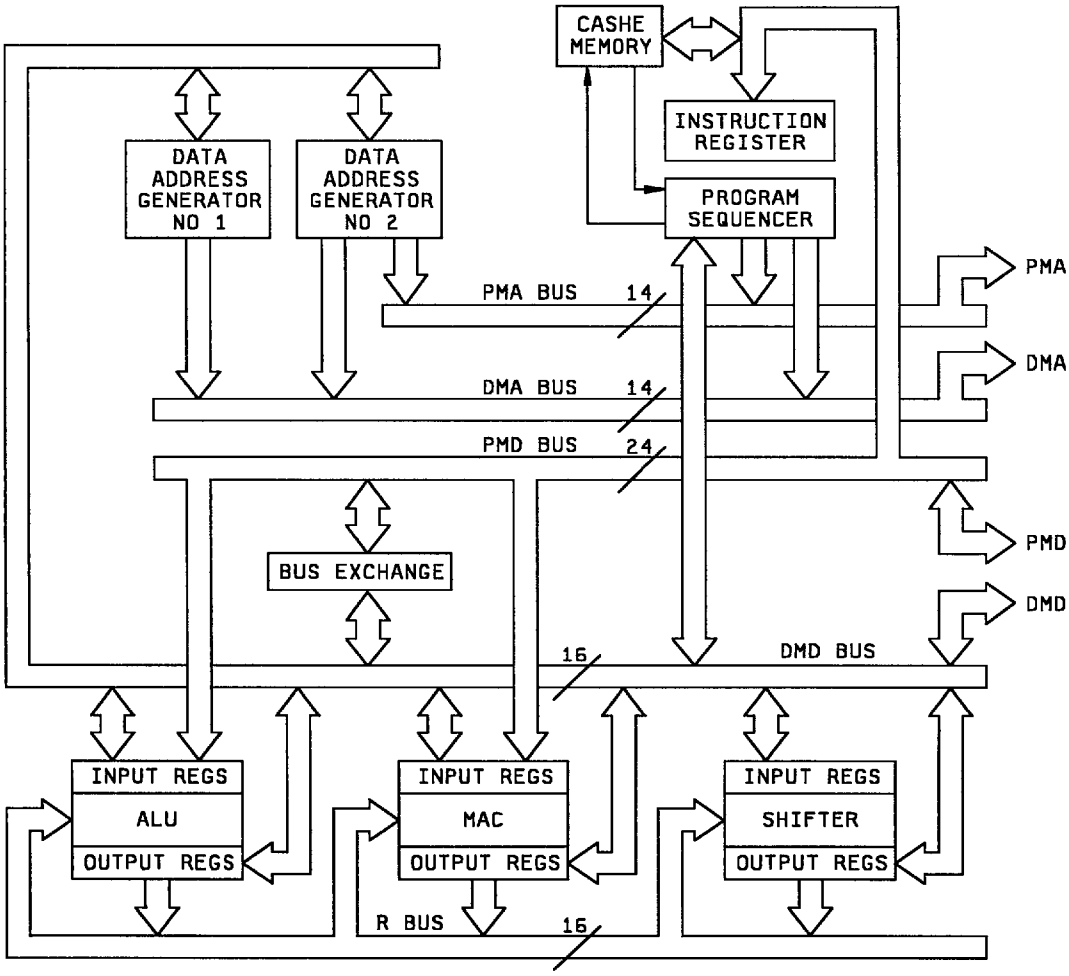
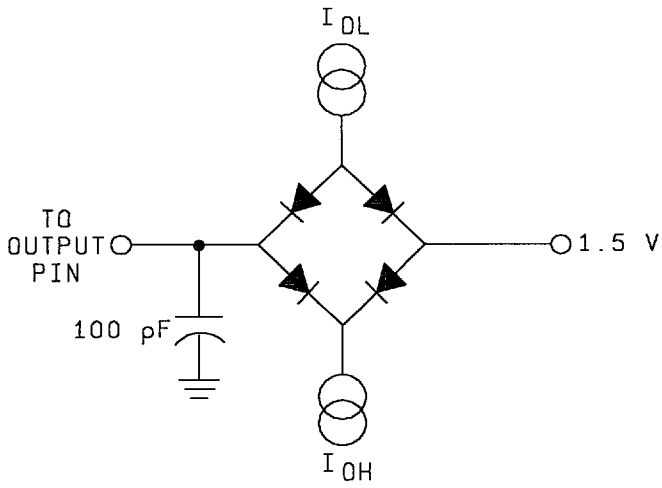
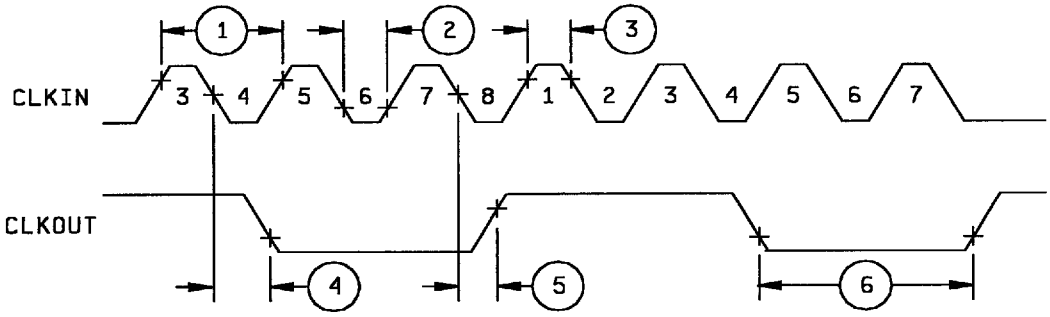


FIGURE 2. Block diagram.



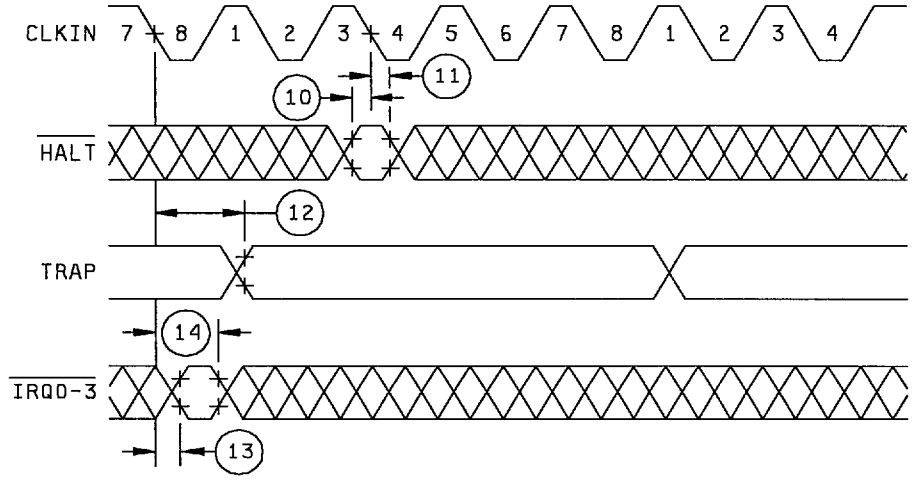
Normal load for AC measurements



NOTE: The processor cycle is divided into eight internal states determined by the rising and falling edges of CLKIN. CLKOUT is synchronized to the processor states as shown above.

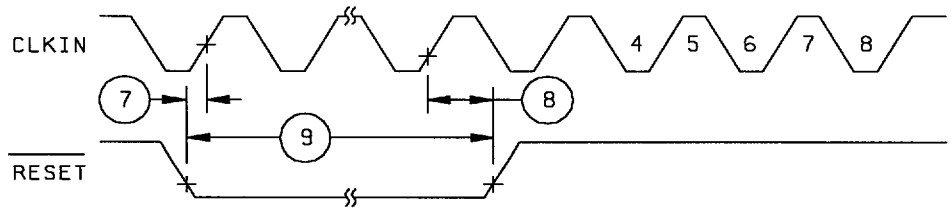
Clock signals

FIGURE 3. Test circuit and waveforms.



NOTE: The control signals are shown in relationship to the processor states in which they are recognized or asserted as defined by CLKIN. There is no implied relationship between $\overline{\text{HALT}}$, TRAP, and $\overline{\text{IRQ}}_{0\text{-}3}$.

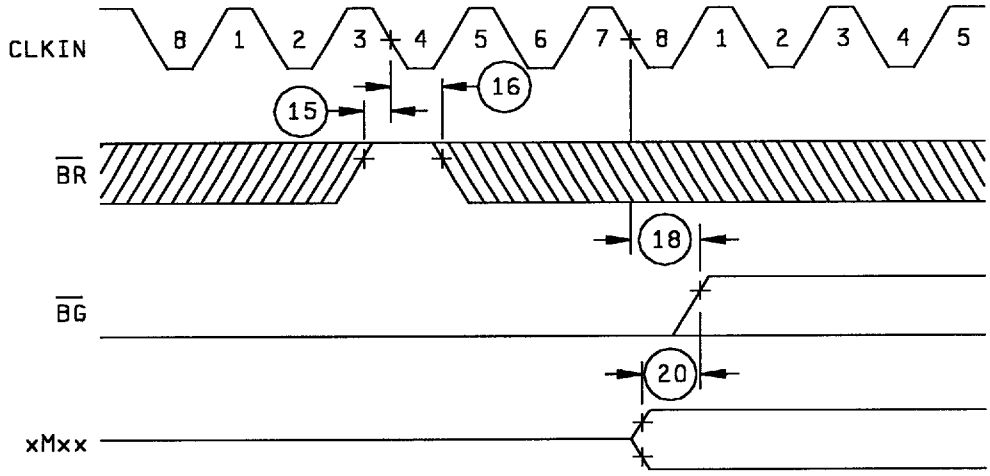
Control signals



NOTE: The $\overline{\text{RESET}}$ signal determines the phase of the processor cycle. The processor starts from state 4 after the release of the $\overline{\text{RESET}}$ signal.

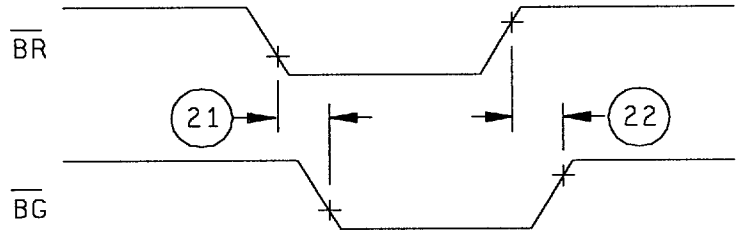
$\overline{\text{RESET}}$ signal

FIGURE 3. Test circuit and waveforms - Continued.



NOTE: xMxx refers to PMA_{0-13}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, PMDA, DMA_{0-13}, $\overline{DMS}$, $\overline{DMRD}$, and $\overline{DMWR}$.

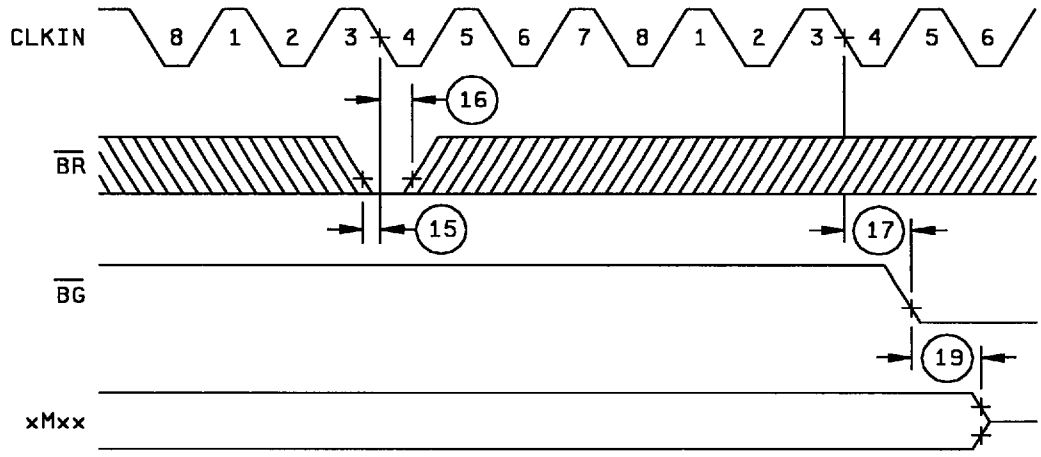
Bus request negated



NOTE: During $\overline{RESET}$, the processor bus ignores the CLKIN signal and therefore the bus request/grant signals operate asynchronously.

Bus request/grant with $\overline{RESET}$ low

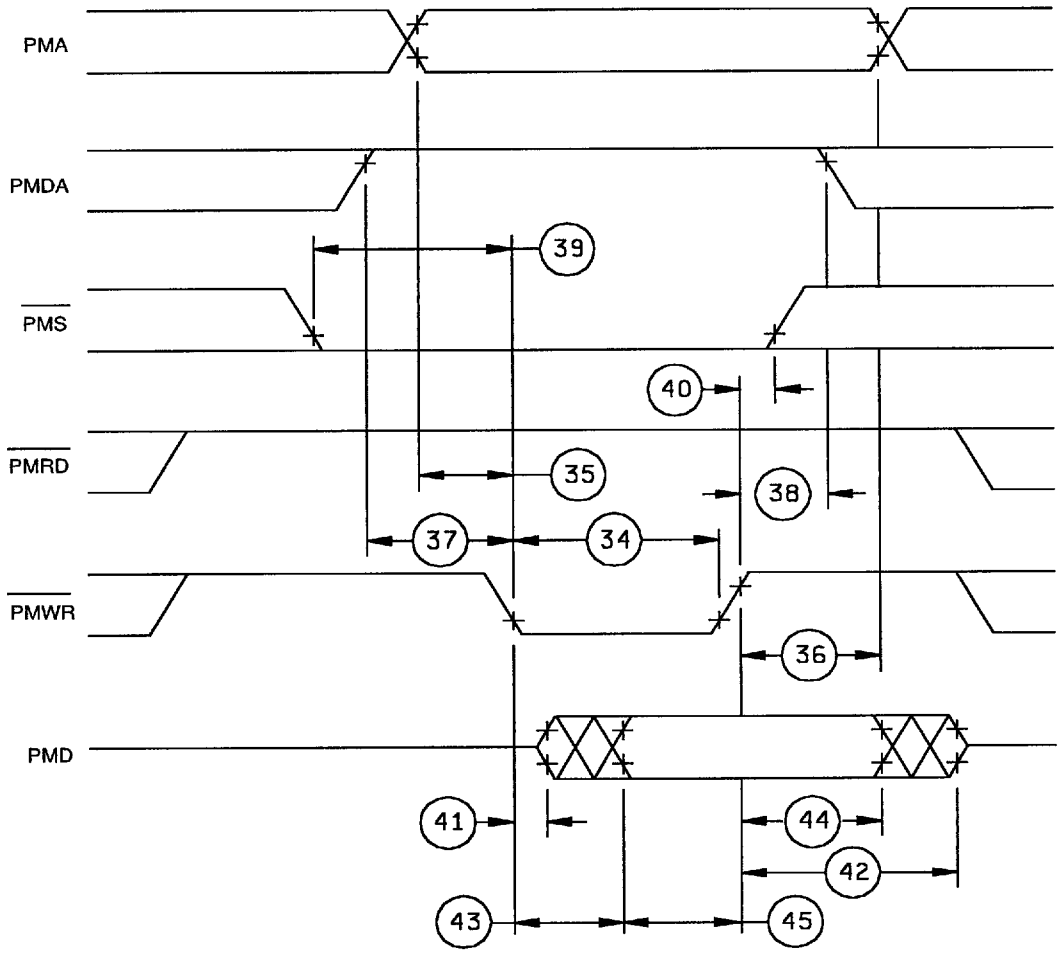
FIGURE 3. Test circuit and waveforms - Continued.



NOTE: xMxx refers to PMA_{0-13}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, PMDA, DMA_{0-13}, $\overline{DMS}$, $\overline{DMRD}$, and $\overline{DMWR}$.

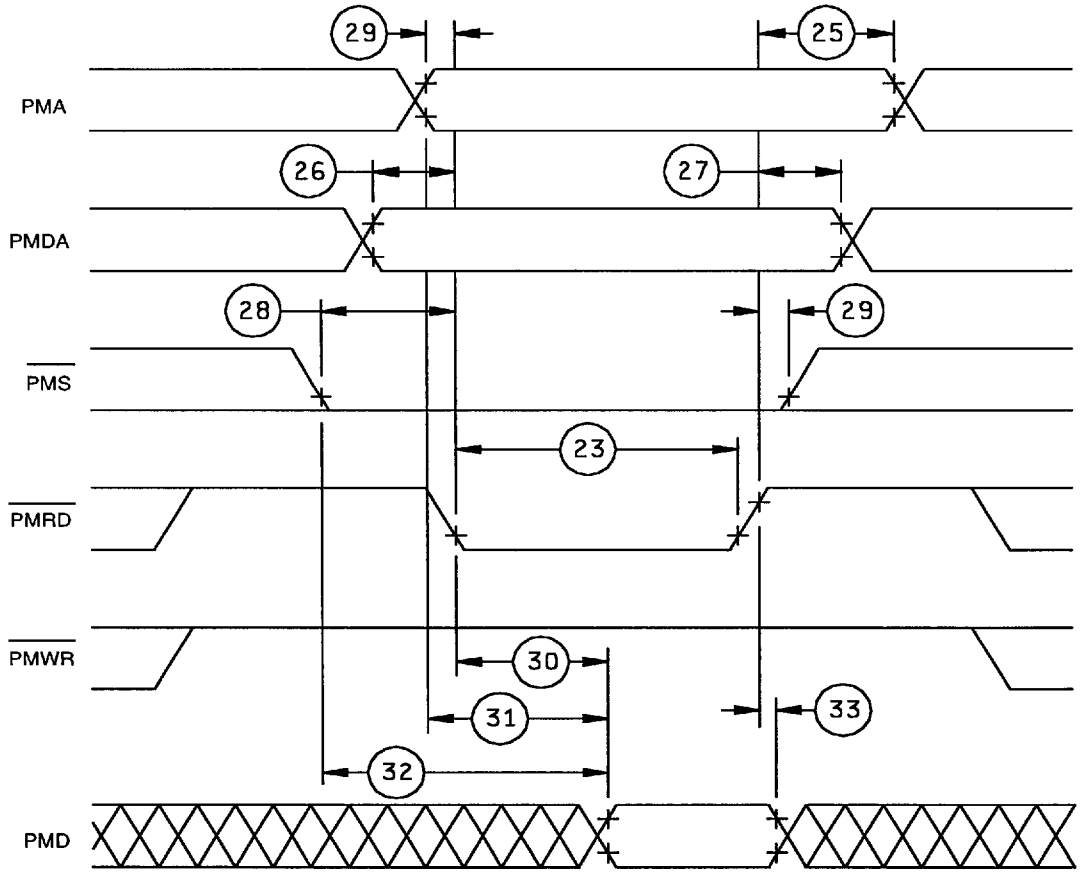
Bus request asserted

FIGURE 3. Test circuit and waveforms - Continued.



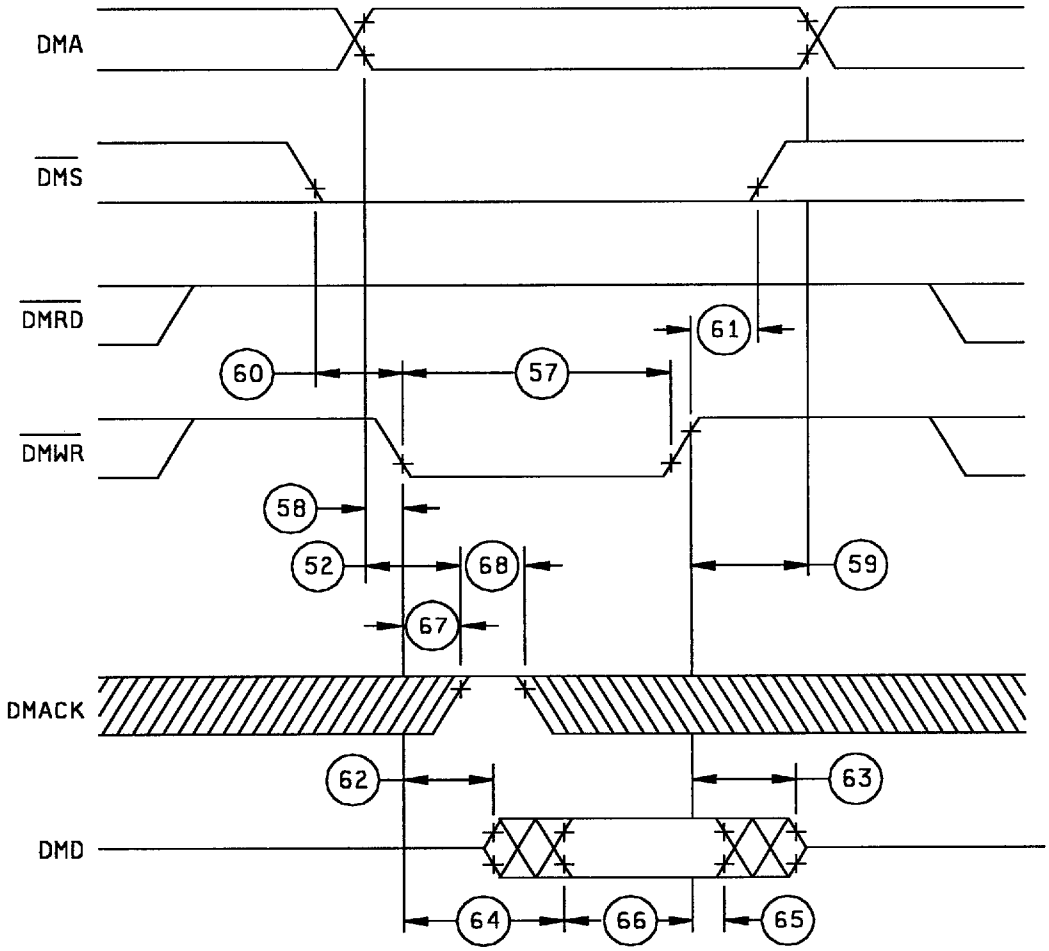
Program memory write

FIGURE 3. Test circuit and waveforms - Continued.



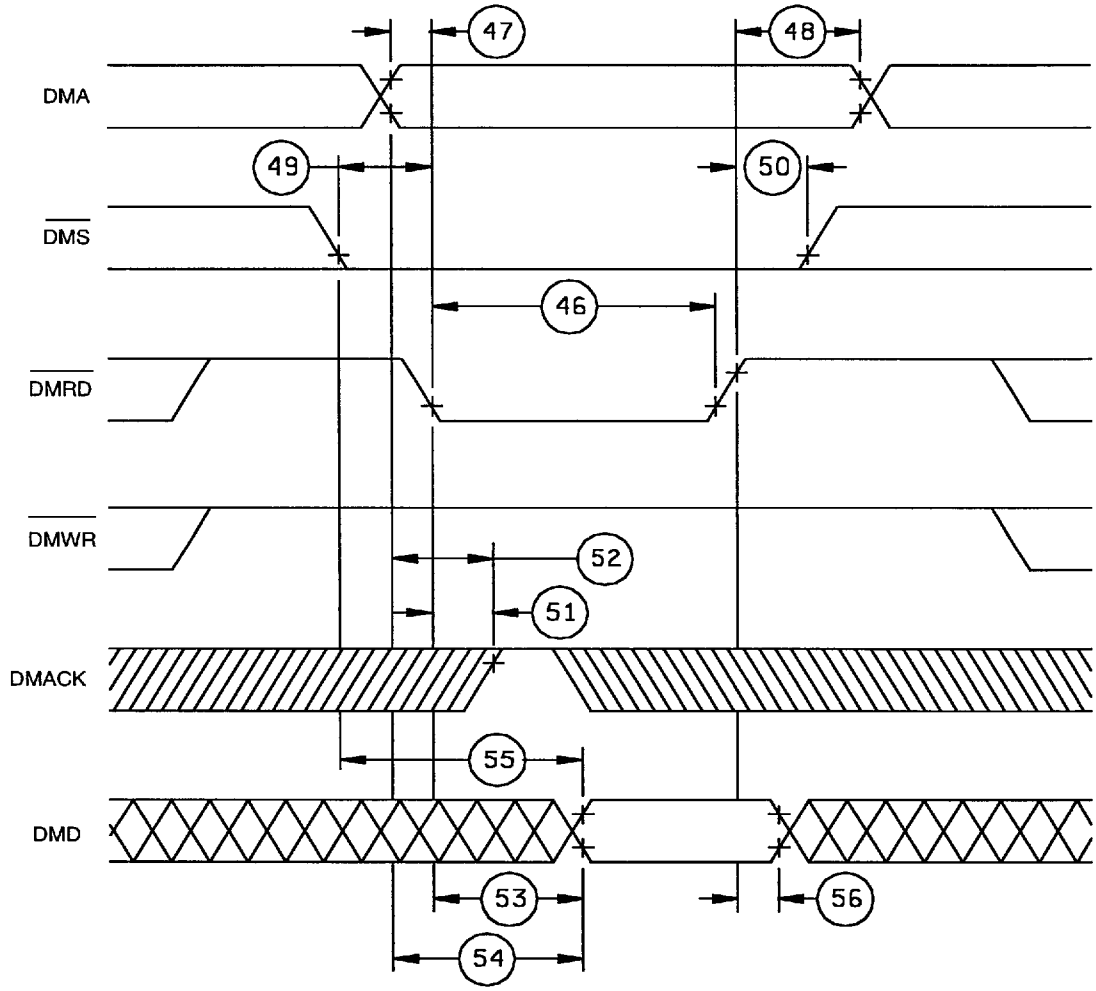
Program memory read

FIGURE 3. Test circuit and waveforms - Continued.



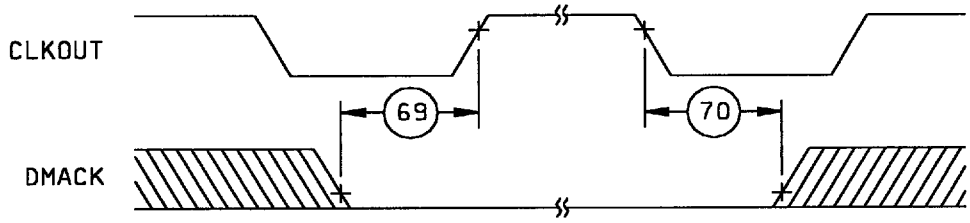
Data memory write

FIGURE 3. Test circuit and waveforms - Continued.



Data memory read

FIGURE 3. Test circuit and waveforms - Continued.



Data memory wait states extended with DMACK

FIGURE 3. Test circuit and waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of three devices with zero rejects shall be required.

d. Subgroups 7 and 8 tests shall verify the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available for review from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Test codes.

Code	Test type	Level references
A	Inputs, outputs	Low = 0.8 V, high = 2.0 V
B	CLKIN To or from inputs, outputs	1.5 V Low = 0.8 V, high = 2.0 V
C	Output To output disable	Low = 0.8 V, high = 2.0 V Low = V_{OL} + 0.5 V, high = V_{OH} - 0.5 V
D	Output To or from output enable	Low = 0.8 V, high = 2.0 V Low = V_T - 0.1 V, high = V_T + 0.1 V 1/

1/ V_T = 1.5 V, the voltage to which three-stated outputs are forced.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-06-01

Approved sources of supply for SMD 5962-87735 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8773501XX	24355	ADSP-2100SG/883B
5962-8773502XX	3/	ADSP-2100TG/883B
5962-8773503XX	24355	ADSP-2100ASG/883B
5962-8773504XX	24355	ADSP-2100ATG/883B
5962-8773505XX	24355	ADSP-2100AUG/883B
5962-8773506XX	24355	ADSP-2100AVG/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Inactive for new design. Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.