CS3302A

# High-Z, Programmable Gain, Differential Amplifier

## Features

- Signal Bandwidth: DC to 2 kHz
- Selectable Gain: x1, x2, x4, x8, x16, x32, x64
- Differential Inputs, Differential Outputs
  - Multiplexed inputs: INA, INB, 800Ω termination
  - Rough / fine charge outputs for CS5371A / 72A / 73A
  - Max signal amplitude: 5 $V_{pp}$ differential
  - Ultra-low input bias: < 1 pA
- Excellent Noise Performance
  - 1 $\mu V_{p-p}$ between 0.1 Hz and 10 Hz
  - 8.5 nV/ $\sqrt{Hz}$ from 200 Hz to 2 kHz
- Low Total Harmonic Distortion
  - -118 dB THD typical (0.000126%)
  - -112 dB THD maximum (0.000251%)
- Low Power Consumption
  - Normal operation: 5 mA
  - Power down: 10 µA
- Dual Power Supply Configuration
  - VA+ = +2.5 V; VA- = -2.5 V; VD = +3.3 V

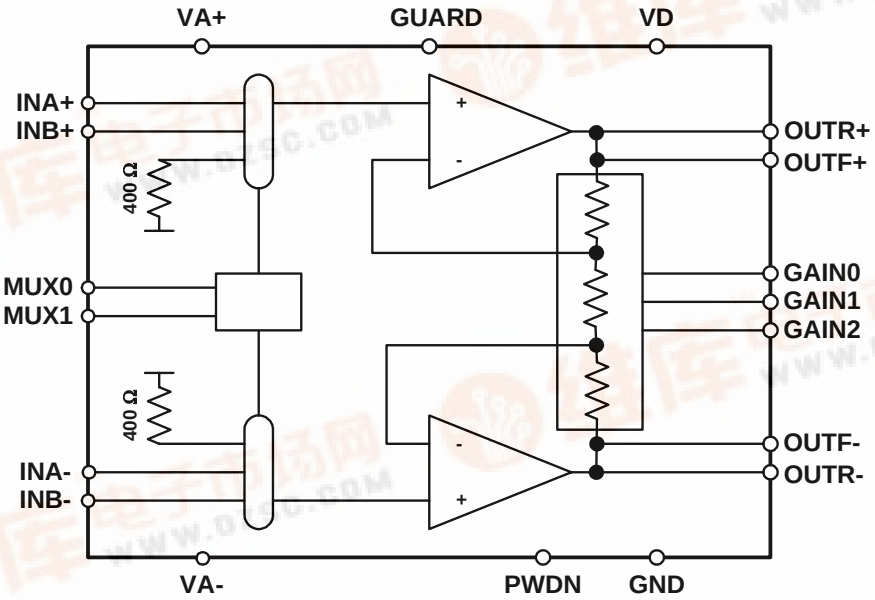
## Description

The CS3302A is a high input-impedance, differential input, differential output amplifier with programmable gain, optimized for amplifying signals from high-impedance sensors such as hydrophones. The gain settings are binary weighted (x1, x2, x4, x8, x16, x32, x64) and are selected using simple pin settings. Two sets of external inputs, INA and INB, simplify system design as inputs from a sensor and test DAC. An internal 800Ω termination can also be selected for noise tests.

Amplifier input impedance is very high, requiring less than 1 pA of input current. Noise performance is very good at 1 $\mu V_{p-p}$ between 0.1 Hz and 10 Hz, and a noise density of 8.5 nV/ $\sqrt{Hz}$ over the 200 Hz to 2 kHz bandwidth. Distortion performance is also extremely good, typically -118 dB THD. Low input current, low noise, and low total harmonic distortion make this amplifier ideal for high-impedance differential sensors requiring maximum dynamic range.

### ORDERING INFORMATION

See page 15.




*Preliminary Product Information* | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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## REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| PP1 | NOV 2007 | Initial release. |

## Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**

# 1. CHARACTERISTICS AND SPECIFICATIONS

- Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A$ = 25°C.
- GND = 0 V, all voltages with respect to 0 V.
- Device connected as shown in Figure 5 on page 12 unless otherwise noted.

## SPECIFIED OPERATING CONDITIONS

| Parameter | | Symbol | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| ***Bipolar Power Supplies*** | | | | | | |
| Positive Analog | ±2% | VA+ | 2.45 | 2.50 | 2.55 | V |
| Negative Analog | (Note 1) ±2% | VA- | -2.55 | -2.50 | -2.45 | V |
| Positive Digital | (Note 2) ±3% | VD | 3.20 | 3.30 | 3.40 | V |
| ***Thermal*** | | | | | | |
| Ambient Operating Temperature | Industrial (-IS, -ISZ) | $T_A$ | -40 | 25 | 85 | °C |

Notes: 1. VA- must be the most negative voltage to avoid potential SCR latch-up conditions.
2. VD must conform to Digital Supply Differential under Absolute Maximum Ratings.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Symbol | CS3302A Min | CS3302A Max | Unit |
|---|---|---|---|---|---|
| DC Power Supplies | Positive Analog | VA+ | -0.3 | 6.8 | V |
| | Negative Analog | VA- | -6.8 | 0.3 | V |
| | Digital | VD | -0.3 | 6.8 | V |
| Analog Supply Differential | [(VA+) - (VA-)] | $VA_{DIFF}$ | - | 6.8 | V |
| Digital Supply Differential | [(VD) - (VA-)] | $VD_{DIFF}$ | - | 6.8 | V |
| Input Current, Any Pin Except Supplies | (Note 3) | $I_{IN}$ | - | ±10 | mA |
| Input Current, Power Supplies | (Note 3) | $I_{PWR}$ | - | ±50 | mA |
| Output Current | (Note 3) | $I_{OUT}$ | - | ±25 | mA |
| Power Dissipation | | PD | - | 500 | mW |
| Analog Input Voltages | | $V_{INA}$ | (VA-)-0.5 | (VA+)+0.5 | V |
| Digital Input Voltages | | $V_{IND}$ | -0.5 | (VD)+0.5 | V |
| Storage Temperature Range | | $T_{STG}$ | -65 | 150 | ºC |

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 3. Transient currents up to 100mA will not cause SCR latch-up.

## THERMAL CHARACTERISTICS

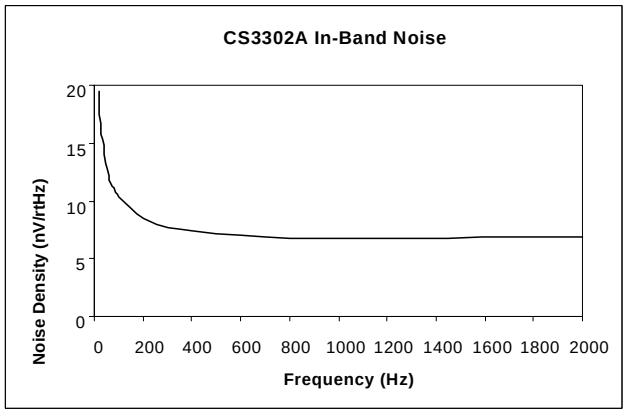
| Parameter | Symbol | CS3302A Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Storage Temperature Range | $T_{STR}$ | -65 | - | 150 | ºC |
| Allowable Junction Temperature | | - | - | 125 | ºC |
| Junction to Ambient Thermal Impedance | $\Theta_{JA}$ | - | 65 | - | ºC / W |
| Ambient Operating Temperature | $T_A$ | -40 | - | +85 | ºC |

## ANALOG CHARACTERISTICS

| Parameter | | Symbol | CS3302A Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***Noise Performance*** | | | | | | |
| Input Voltage Noise | $f_0$ = 0.1 Hz to 10 Hz | $VN_{PP}$ | - | 1 | 3 | $\mu V_{pp}$ |
| Input Voltage Noise Density | $f_0$ = 200 Hz to 2 kHz | $VN_D$ | - | 8.5 | 12 | $nV/\sqrt{Hz}$ |
| Input Current Noise Density | (Note 4) | $IN_D$ | - | 20 | - | $fA/\sqrt{Hz}$ |
| ***Distortion Performance*** | | | | | | |
| Total Harmonic Distortion (Note 5) | x1 | THD | - | -118 | -112 | dB |
| | x2 | | - | -119 | - | |
| | x4 | | - | -119 | - | |
| | x8 | | - | -119 | - | |
| | x16 | | - | -118 | - | |
| | x32 | | - | -115 | - | |
| | x64 | | - | -112 | - | |
| Linearity (Note 5) | x1 | LIN | - | 0.0001259 | 0.0002512 | % |
| | x2 | | - | 0.0001122 | - | |
| | x4 | | - | 0.0001122 | - | |
| | x8 | | - | 0.0001122 | - | |
| | x16 | | - | 0.0001259 | - | |
| | x32 | | - | 0.0001778 | - | |
| | x64 | | - | 0.0002512 | - | |

Notes: 4. Guaranteed by design and/or characterization.

5. Tested with a 31.25 Hz sine wave at -1 dB amplitude.



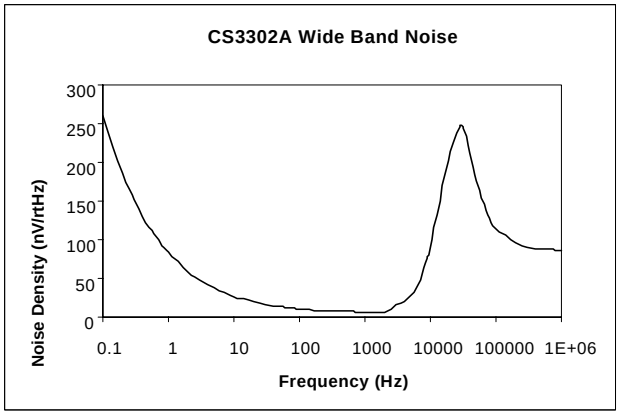




**Figure 1. CS3302A Noise Performance**

## ANALOG CHARACTERISTICS (CONT.)

| Parameter | | Symbol | CS3302A Min | CS3302A Typ | CS3302A Max | Unit |
|---|---|---|---|---|---|---|
| ***Gain*** | | | | | | |
| Gain, Differential | | GAIN | x1 | - | x64 | |
| Gain, Common Mode | (Note 6) | $GAIN_{CM}$ | - | x1 | - | |
| Gain Accuracy, Absolute | (Note 7) | $GAIN_{ABS}$ | - | ±1 | ±2 | % |
| Gain Accuracy, Relative (Note 8) | x2 | LIN | -0.4 | -0.2 | 0 | % |
| | x4 | | - | -0.2 | - | |
| | x8 | | - | -0.2 | - | |
| | x16 | | - | -0.2 | - | |
| | x32 | | - | -0.2 | - | |
| | x64 | | - | -0.2 | - | |
| Gain Drift | (Note 4, 9) | $GAIN_{TC}$ | - | 5 | - | ppm / ºC |
| ***Offset*** | | | | | | |
| Offset Voltage, Input Referred | (Note 10) | OFST | - | ±250 | ±750 | µV |
| Offset After Calibration, Absolute | (Note 11) | $OFST_{CAL}$ | - | ±1 | - | µV |
| Offset Calibration Range | (Note 12) | $OFST_{RNG}$ | - | 100 | - | % F.S. |
| Offset Voltage Drift | (Note 4, 9) | $OFST_{TC}$ | - | 1 | - | µV / ºC |

Notes:
6. Common mode signals pass unchanged through the differential amplifier architecture and are rejected by the CS5371A / 72A / 73A modulator CMRR.
7. Absolute gain accuracy tests the matching of x1 gain across multiple CS3302A devices.
8. Relative gain accuracy tests the tracking of x1,x2, x4,x16,x32,x64 gain relative to x1 gain on a single CS3302A device.
9. Specification is for the parameter over the specified temperature range and is for the CS3302A device only. It does not include the effects of external components.
10. Offset voltage is tested with the amplifier inputs connected to the internal 800Ω termination.
11. The absolute offset after calibration specification applies to the effective offset voltage of the CS3302A output when used with the CS5371A / 72A / 73A modulator and the CS5376A / 78 digital filter, and is measured from the digitally calibrated output codes of the CS5376A / 78.
12. The CS3302A offset calibration is performed digitally with the CS5371A / 72A / 73A modulator and CS5376A / 78 digital filter and includes the full scale signal range. Calibration offsets of greater than ± 5% of full scale will begin to subtract from system dynamic range.

## ANALOG CHARACTERISTIC (Cont.)

| Parameter | | Symbol | CS3302A Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***Analog Input Characteristics*** | | | | | | |
| Input Signal Frequencies | | BW | DC | - | 2000 | Hz |
| Input Voltage Range (Signal + Vcm) | x1 | $V_{IN}$ | (VA-)+0.7 | - | (VA+)-1.25 | V |
| | x2 - x64 | | (VA-)+0.7 | - | (VA+)-1.75 | |
| Full Scale Input, Differential | x1 | $V_{INFS}$ | - | - | 5 | $V_{p-p}$ |
| | x2 | | - | - | 2.5 | $V_{p-p}$ |
| | x4 | | - | - | 1.25 | $V_{p-p}$ |
| | x8 | | - | - | 625 | $mV_{p-p}$ |
| | x16 | | - | - | 312.5 | $mV_{p-p}$ |
| | x32 | | - | - | 156.25 | $mV_{p-p}$ |
| | x64 | | - | - | 78.125 | $mV_{p-p}$ |
| Input Impedance, Differential | | $Z_{INDIFF}$ | - | 1, 20 | - | TΩ, pF |
| Input Impedance, Common Mode | | $Z_{INCM}$ | - | 0.5, 40 | - | TΩ, pF |
| Input Bias Current | | $I_{IN}$ | - | 1 | 40 | pA |
| Crosstalk, Multiplexed Inputs | (Note 4) | XT | - | -130 | - | dB |
| Common to Differential Mode Rejection | (Note 4, 13) | CDMR | 90 | 100 | - | dB |
| ***Analog Output Characteristics*** | | | | | | |
| Full Scale Output, Differential | | $V_{OUT}$ | - | - | 5 | $V_{pp}$ |
| Output Voltage Range (Signal + Vcm) | | $V_{RNG}$ | (VA-)+0.5 | - | (VA+)-0.5 | V |
| Output Impedance | (Note 14) | $Z_{OUT}$ | - | 40 | - | Ω |
| Output Impedance Drift | (Note 14) | $Z_{TC}$ | - | 0.38 | - | Ω/°C |
| Output Current | | $I_{OUT}$ | - | - | ±25 | mA |
| Load Capacitance | | $C_L$ | - | - | 100 | nF |
| ***Guard Output Characteristics*** | | | | | | |
| Guard Output Voltage | | $V_{GUARD}$ | - | $V_{cm}$ | - | V |
| Guard Output Impedance | | $ZG_{OUT}$ | - | 500 | - | Ω |
| Guard Output Current | | $IG_{OUT}$ | - | 40 | - | µA |
| Guard Load Capacitance | | $CG_L$ | - | - | 100 | pF |

Notes: 13. Ratio of common mode input amplitude vs. differential mode output amplitude for a perfectly matched common mode input signal. Characterized with a 50 Hz, 500 $mV_{peak}$ common mode sine wave applied to the analog inputs.

14. Output impedance characteristics are approximate and can vary up to +/- 30% depending on process parameters.

## DIGITAL CHARACTERISTICS

| Parameter | Symbol | CS3302A Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***Digital Characteristics*** | | | | | |
| High-level Input Drive Voltage (Note 15) | $V_{IH}$ | 0.6*VD | - | VD | V |
| Low-level Input Drive Voltage (Note 15) | $V_{IL}$ | 0.0 | - | 0.8 | V |
| Input Leakage Current | $I_{IN}$ | - | ±1 | ±10 | µA |
| Digital Input Capacitance | $C_{IN}$ | - | 9 | - | pF |
| Rise Times | $t_{RISE}$ | - | - | 100 | ns |
| Fall Times | $t_{FALL}$ | - | - | 100 | ns |

Notes: 15. Device is intended to be driven with CMOS logic levels.

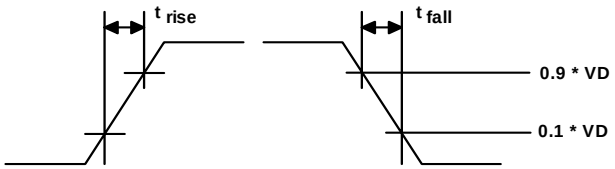



**Figure 2. Digital Input Rise and Fall Times**

| Input Selection | MUX1 | MUX0 |
|---|---|---|
| 800 Ω termination | 0 | 0 |
| INA only | 1 | 0 |
| INB only | 0 | 1 |
| INA + INB | 1 | 1 |

| Gain Selection | GAIN2 | GAIN1 | GAIN0 |
|---|---|---|---|
| x1 | 0 | 0 | 0 |
| x2 | 0 | 0 | 1 |
| x4 | 0 | 1 | 0 |
| x8 | 0 | 1 | 1 |
| x16 | 1 | 0 | 0 |
| x32 | 1 | 0 | 1 |
| x64 | 1 | 1 | 0 |
| Reserved | 1 | 1 | 1 |

**Table 1. Digital Selection for Gain and Input Mux Control**

## POWER SUPPLY CHARACTERISTICS

| Parameter | Symbol | CS3302A Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***Power Supply Current, Normal Mode*** | | | | | |
| Analog Power Supply Current (Note 16) | $I_A$ | - | 5.0 | 5.75 | mA |
| Digital Power Supply Current (Note 16) | $I_D$ | - | 0.1 | 0.2 | mA |
| ***Power Supply Current, Power Down Mode*** | | | | | |
| Analog Power Supply Current, PWDN = 1 (Note 16) | $I_A$ | - | 9 | 11 | µA |
| Digital Power Supply Current, PWDN = 1 (Note 16) | $I_D$ | - | 2 | 8 | µA |
| ***Power Supply Rejection*** | | | | | |
| Power Supply Rejection Ratio (Note 4, 17) | PSRR | 95 | 120 | - | dB |

Notes: 16. All outputs unloaded. Analog inputs connected to the internal 800 Ω termination. Digital inputs forced to VD or GND respectively.

17. Power supply rejection characterized with a 50 Hz, 400 $mV_{pp}$ sine wave applied separately to each supply.

# 2. GENERAL DESCRIPTION

The CS3302A is a high-impedance, low-noise CMOS differential input, differential output amplifier for precision analog signals between DC and 2 kHz. It has multiplexed inputs, rough/fine charge outputs, and programmable gains of x1, x2, x4, x8, x16, x32, and x64.

The performance of this amplifier makes it ideal for low-frequency, high-dynamic-range applications requiring low distortion and minimal power consumption. It is optimized for use in acquisition systems designed around the CS5371A/72A single/dual ΔΣ modulators and the CS5376A quad digital filter or the CS5373A ΔΣ modulator and CS5378 digital filter. Figure 3 shows the system-level architecture of a 4-channel acquisition system using four CS3302A, two CS5372A, one CS4373A, and one CS5376A. Figure 4 shows the system architecture of a single channel acquisition system using a CS3302A, CS5373A, and CS5378.

## 2.1 Analog Signals

### 2.1.1 Analog Inputs

The amplifier analog inputs are designed for high-impedance differential sensors. Input multiplexing simplifies system connections by providing separate inputs for a sensor and test DAC (INA, INB) as well as an internal termination for noise tests. The MUX0, MUX1 digital pins determine which multiplexed input is connected to the amplifier.

### 2.1.2 Analog Outputs

The amplifier analog outputs are separated into rough charge / fine charge signals to easily connect to the CS5371A/72A/73A inputs. Each differential output

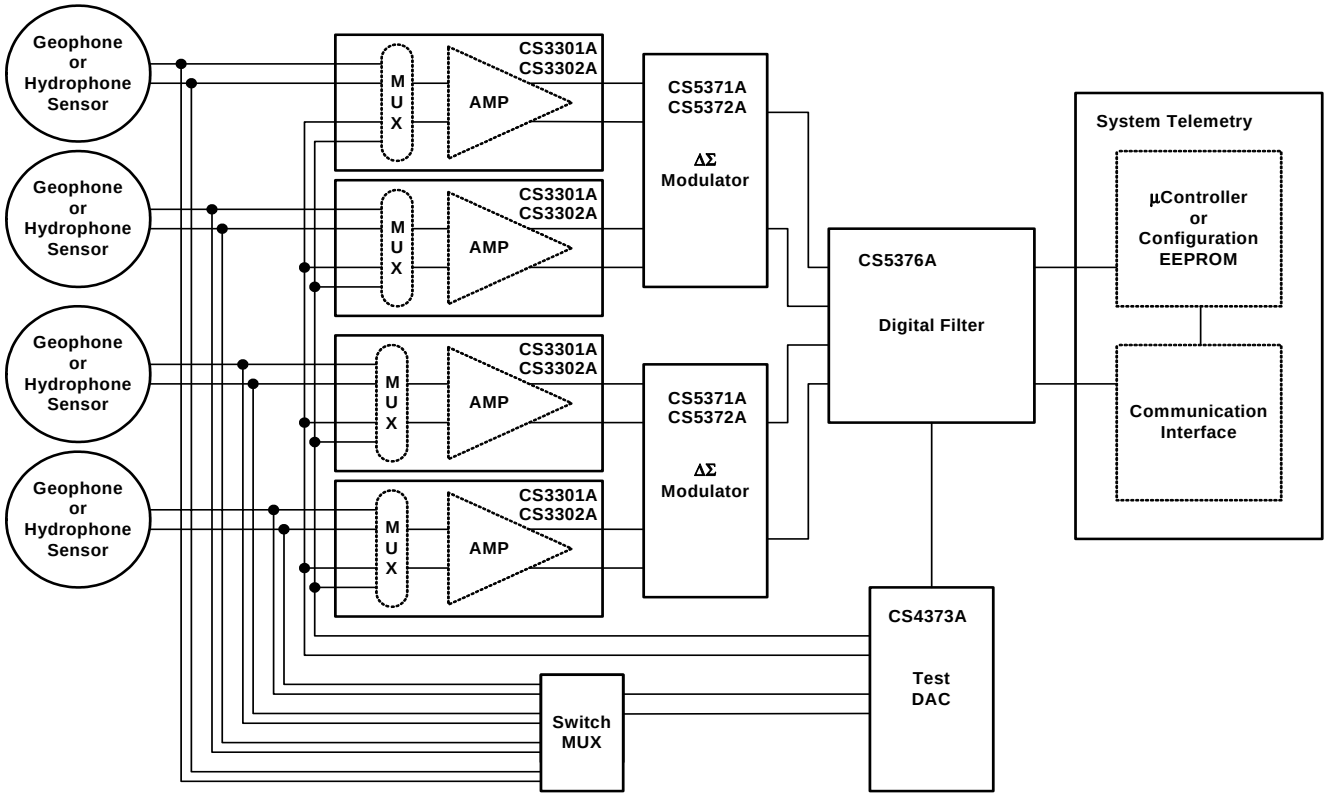



**Figure 3. System Architecture**

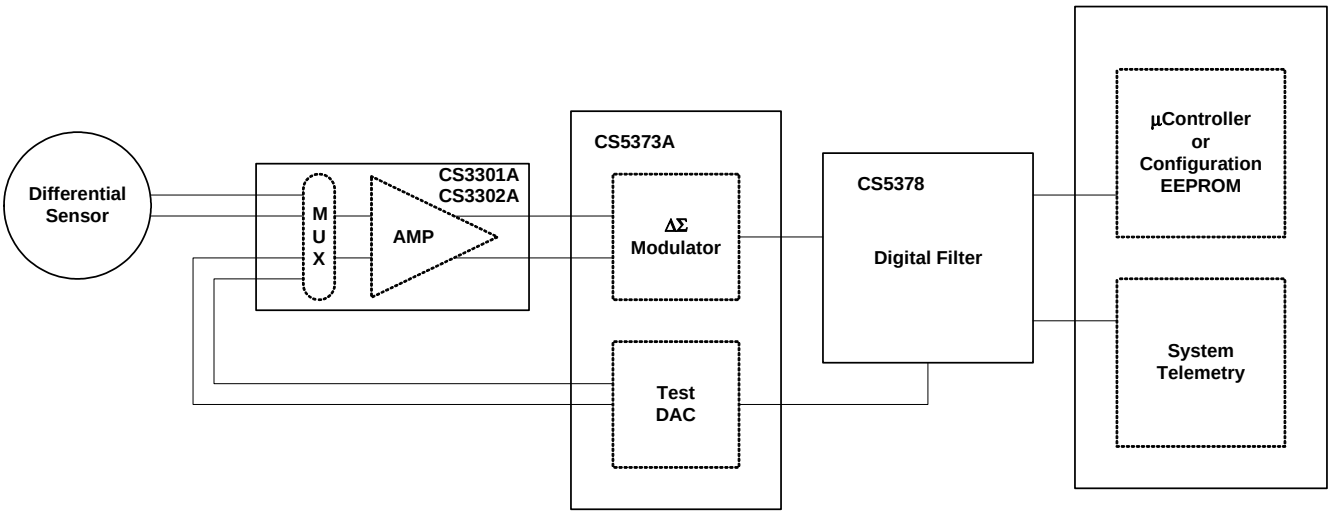



**Figure 4. System Architecture**

requires two series resistors and a differential capacitor to create the modulator anti-alias RC filter.

#### 2.1.3 Differential Signals

Analog signals into and out of the CS3302A are differential, consisting of two halves with equal but opposite magnitude varying about a common mode voltage.

A full scale 5 $V_{pp}$ differential signal centered on a -0.15 V common mode can have:

SIG+ = -0.15 V + 1.25 V = 1.1 V

SIG- = -0.15 V - 1.25 V = -1.4 V

SIG+ is +2.5 V relative to SIG-

For the reverse case:

SIG+ = -0.15 V - 1.25 V = -1.4 V

SIG- = -0.15 V + 1.25 V = 1.1 V

SIG+ is -2.5 V relative to SIG-

The total swing for SIG+ relative to SIG- is (+2.5 V) - (-2.5 V) = 5 $V_{pp}$. A similar calculation can be done for SIG- relative to SIG+. Note that a 5 $V_{pp}$ differential signal centered on a -0.15 V common mode voltage never exceeds 1.1 V and never drops below -1.4 V on either half of the signal.

By definition, differential voltages are to be measured with respect to the opposite half, not relative to ground. A multimeter differentially measuring between SIG+ and SIG- in the above example would properly read 1.767 $V_{rms}$, or 5 $V_{pp}$.

#### 2.1.4 Guard Output

The GUARD pin outputs the common mode voltage of the currently selected analog signal input. It can be used to drive the cable shield between a high-impedance sensor and the amplifier inputs. Driving the cable shield with the analog signal common mode voltage minimizes leakage and improves signal integrity from high-impedance sensors.

The GUARD output is defined as the midpoint voltage between the + and - halves of the currently selected differential input signal, and will vary as the signal common mode varies. The GUARD output will not drive a significant load, it only provides a shielding voltage.

### 2.2 Digital Signals

#### 2.2.1 Gain Selection

The CS3302A supports gain ranges of x1, x2, x4, x8, x16, x32, and x64. They are selected using the GAIN0, GAIN1, and GAIN2 pins as shown in Table 1 on page 8.

#### 2.2.2 Mux Selection

The analog inputs to the amplifier are multiplexed, with external signals applied to the INA+, INA- or INB+, INB- pins. An internal termination is also available for noise tests. Input mux selection is made using the MUX0 and MUX1 pins as shown in Table 1 on page 8.

Although a mux selection is provided to enable the INA and INB switches simultaneously, significant current should not be driven through them in this mode. The CS3302A mux switches will maintain good linearity only with minimal signal current.

#### 2.2.3 Power Down Selection

A power-down mode is available to shut down the amplifier when not in use. When enabled, all internal circuitry is disabled, the analog inputs and outputs go high-impedance, and the device enters a micro-power state. Power down mode is selected using the PWDN pin, which is active high.

## 2.3 Power Supplies

#### 2.3.1 Analog Power Supplies

The analog power pins of the CS3302A are to be supplied with a total of 5 V between VA+ and VA-. This voltage is typically from a bipolar ±2.5 V supply. When using bipolar supplies the analog signal common mode voltage should be biased to 0 V. The analog power supplies are recommended to be bypassed to system ground using 0.1 µF X7R type capacitors.

The VA- supply is connected to the CMOS substrate and as such must remain the most negative applied voltage to prevent potential latch-up conditions. It is recommended to clamp the VA- supply to system ground using a reverse biased Schottky diode to prevent possible latch-up conditions related to mismatched supply rail initialization.

#### 2.3.2 Digital Power Supplies

The digital power supply across the VD and GND pins is specified for a +3.3 V power supply. The digital power supply should be bypassed to system ground using a 0.01 µF X7R type capacitor.

## 2.4 Connection Diagram

Figure 5 shows a connection diagram for the CS3302A amplifier when used with the CS5372A dual ΔΣ modulator, the CS4373A test DAC and the CS5376A digital filter. The diagram shows differential sensors, a test DAC, and analog outputs with anti-alias capacitors; power supply connections including recommended bypassing; and digital control connections back to the CS5376A GPIO pins.

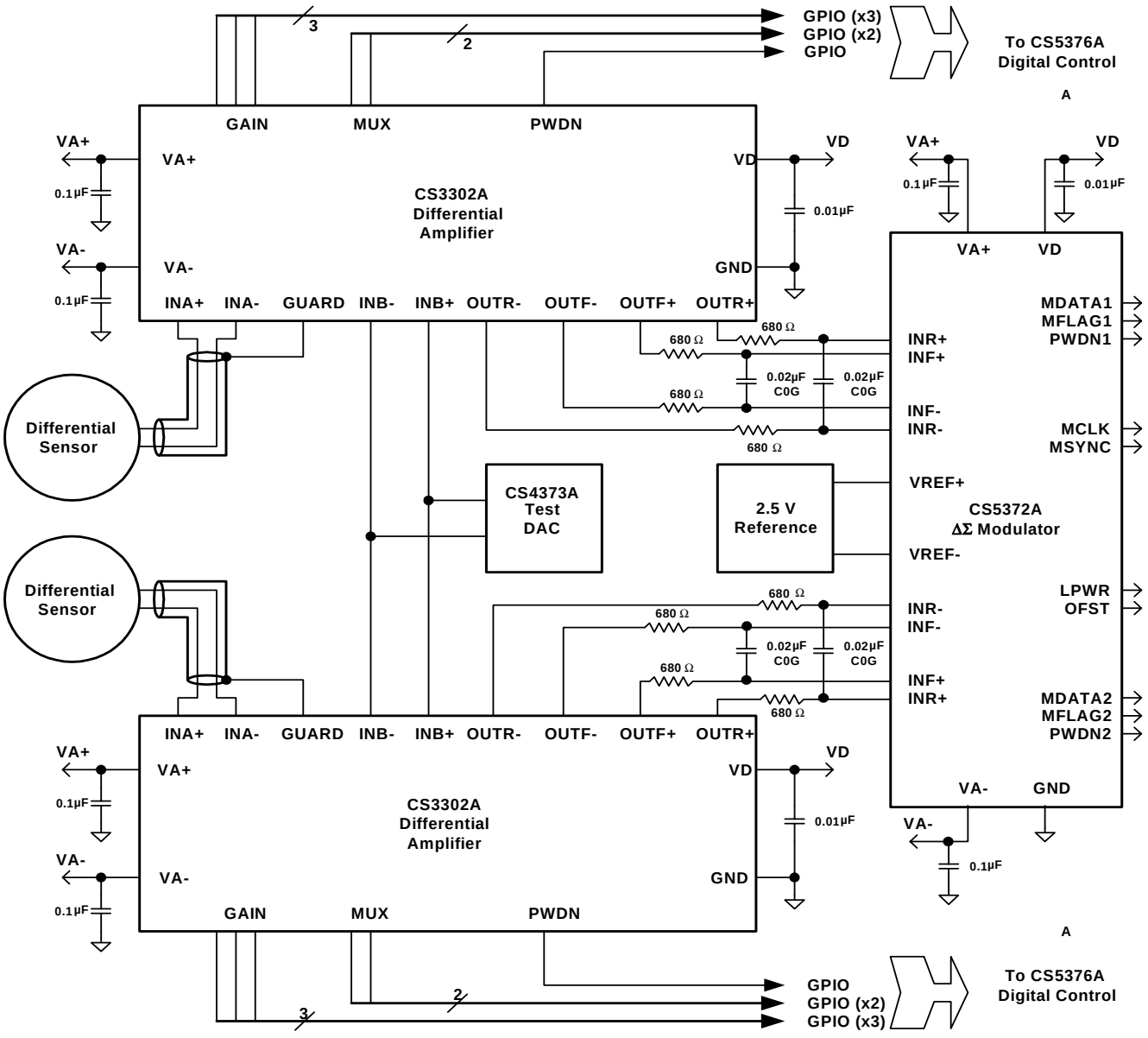



**Figure 5. CS3302A Amplifier Connections**

# 3. PIN DESCRIPTION

| Pin Name | Pin # | I/O | Pin Description |
|---|---|---|---|
| **VA+** | 1 | I | Positive analog supply voltage. |
| **VA-** | 4 | I | Negative analog supply voltage. |
| **VD** | 16 | I | Positive digital supply voltage. |
| **GND** | 15, 18 | I | Ground. |
| **INA+, INA-** | 5, 6 | I | Channel A differential analog inputs. Selected via MUX pins. |
| **INB+, INB-** | 8, 7 | I | Channel B differential analog inputs. Selected via MUX pins. |
| **GUARD** | 13 | O | Guard voltage output. |
| **OUTR+, OUTR-** | 11, 2 | O | Rough charge differential analog outputs. |
| **OUTF+, OUTF-** | 10, 3 | O | Fine charge differential analog outputs. |
| **GAIN0, GAIN1, GAIN2** | 22, 21, 20 | I | Gain range select. See Gain Selection table in Digital Characteristics section. |
| **PWDN** | 19 | I | Power down mode enable. Active high. |
| **MUX0, MUX1** | 24, 23 | I | Analog input select. See Input Selection table in Digital Characteristics section. |
| **TEST0** | 12 | I | Test mode select, factory use only. Connect to VA- during normal operation. |
| **TEST1, TEST2** | 17, 14 | I | Test mode select, factory use only. Connect to GND during normal operation. |
| **TESTOUT** | 9 | O | Test mode output, factory use only. Do not connect during normal operation. |

**Table 2. Pin Descriptions**

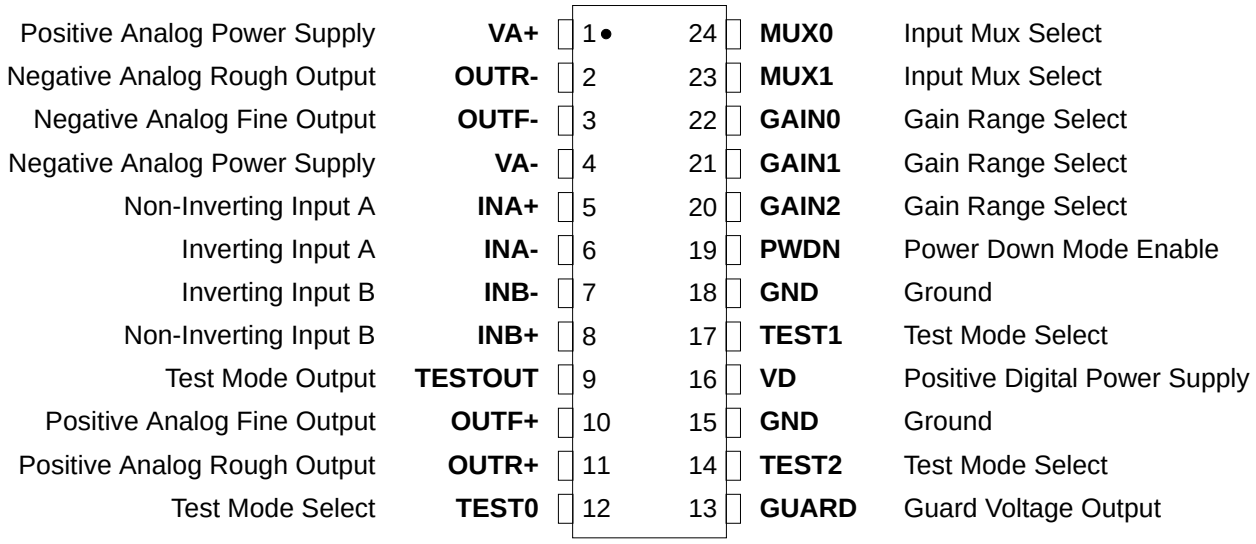



**Figure 6. CS3302A Pin Assignments**

# 4. ORDERING INFORMATION

| Model | Temperature | Package |
|---|---|---|
| CS3302A-IS | -40 to +85 °C | 24-pin SSOP |
| CS3302A-ISZ, lead (Pb) free | | |

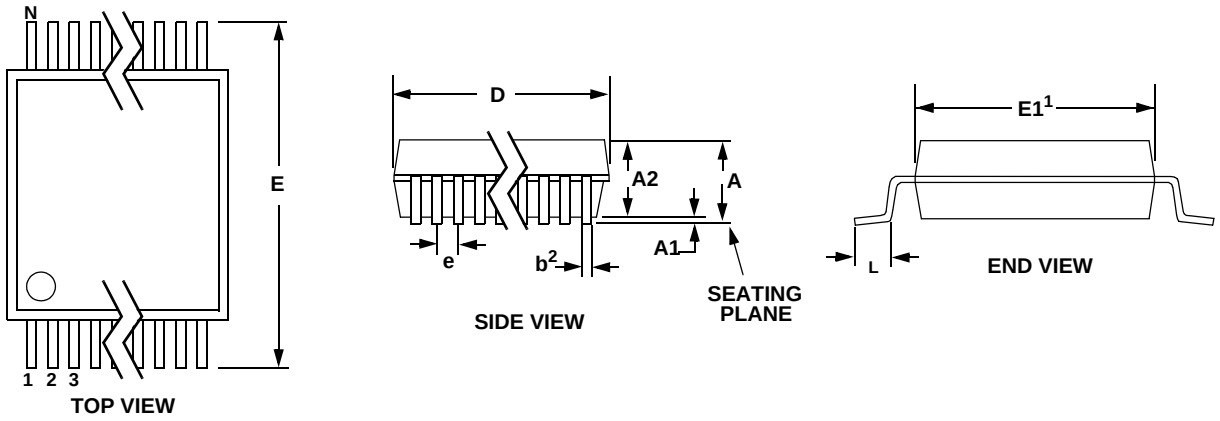
# 5. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

| Model Number | Peak Reflow Temp | MSL Rating* | Max Floor Life |
|---|---|---|---|
| CS3302A-IS | 240 °C | 2 | 365 Days |
| CS3302A-ISZ, lead (Pb) free | 260 °C | 3 | 7 Days |

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

# 6. PACKAGE DIMENSIONS

## 24 PIN SSOP PACKAGE DRAWING




| | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | |
| A | -- | 0.084 | -- | 2.13 | |
| A1 | 0.002 | 0.010 | 0.05 | 0.25 | |
| A2 | 0.064 | 0.074 | 1.62 | 1.88 | |
| b | 0.009 | 0.015 | 0.22 | 0.38 | 2,3 |
| D | 0.311 | 0.335 | 7.90 | 8.50 | 1 |
| E | 0.291 | 0.323 | 7.40 | 8.20 | |
| E1 | 0.197 | 0.220 | 5.00 | 5.60 | 1 |
| e | 0.024 | 0.027 | 0.61 | 0.69 | |
| L | 0.025 | 0.040 | 0.63 | 1.03 | |
| ∝ | 0° | 8° | 0° | 8° | |

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.