

圖 2SK739 快開管

# MOS FIELD EFFECT POWER TRANSISTORS

## 2SK739, 2SK739-Z

### FAST SWITCHING N-CHANNEL SILICON POWER MOS FET INDUSTRIAL USE

#### FEATURES

- Suitable for switching power supplies, actuator controls, and pulse circuits.
- Low  $R_{DS(on)}$
- No second breakdown
- 4 V Gate Drive – Logic level –
- Designed for Hybrid Integrated Circuits

#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current	$I_{D(DC)}$	$\pm 2.0$	A
Peak Drain Current	$I_{D(pulse)^*}$	$\pm 8.0$	A
Total Power Dissipation	$P_T^{**}$	20	W
Total Power Dissipation at $25^\circ\text{C}$ Ambient Temperature	$P_T^{***}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

\*  $PW \leq 300 \mu\text{s}$ , Duty Cycle  $\leq 10\%$ \*\*  $T_c = 25^\circ\text{C}$ \*\*\* Mounted on ceramic substrate of  $2.5 \text{ cm}^2 \times 0.7 \text{ mm}$ 

#### ELECTRICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

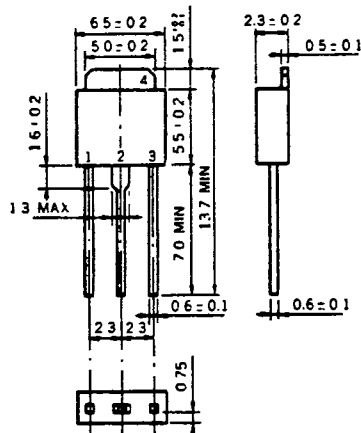
CHARACTERISTIC	SYMBOL	MIN.	TYP	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	$I_{DSS}$			10	$\mu\text{A}$	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to Source Leakage Current	$I_{GSS}$			$\pm 100$	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	1.0			S	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ A}$
Drain to Source On-State Resistance	$R_{DS(on)}$		0.17	0.25	$\Omega$	$V_{GS} = 10 \text{ V}, I_D = 1 \text{ A}$
Drain to Source On-State Resistance	$R_{DS(on)}$		0.22	0.35	$\Omega$	$V_{GS} = 4 \text{ V}, I_D = 0.8 \text{ A}$
Input Capacitance	$C_{iss}$		550		pF	
Output Capacitance	$C_{oss}$		200		pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0$ $f = 1 \text{ MHz}$
Reverse Transfer Capacitance	$C_{rss}$		60		pF	
Turn-On Delay Time	$t_d(on)$		10		ns	$I_D = 1 \text{ A}, V_{CC} = 30 \text{ V}$
Rise Time	$t_r$		20		ns	$V_{GS(on)} = 10 \text{ V}$
Turn-Off Delay Time	$t_d(off)$		80		ns	$R_L = 30 \Omega$
Fall Time	$t_f$		20		ns	$R_{in} = 10 \Omega$

NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

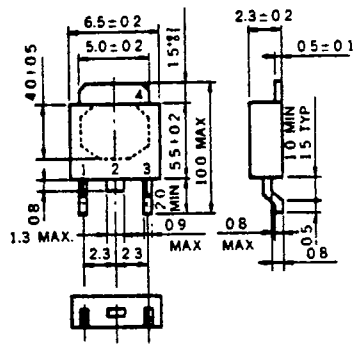
PACKAGE DIMENSIONS (Unit: mm)

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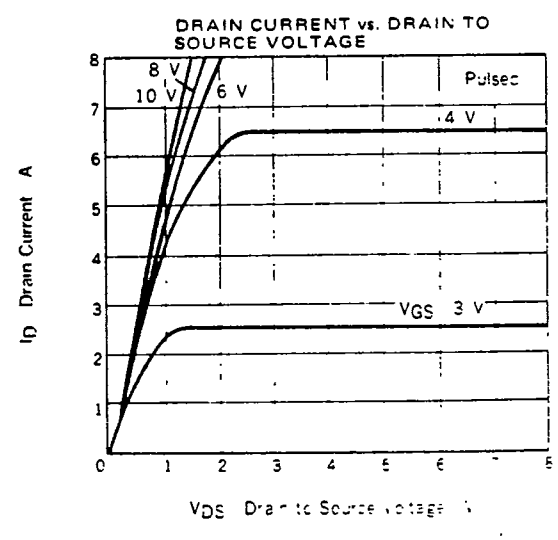
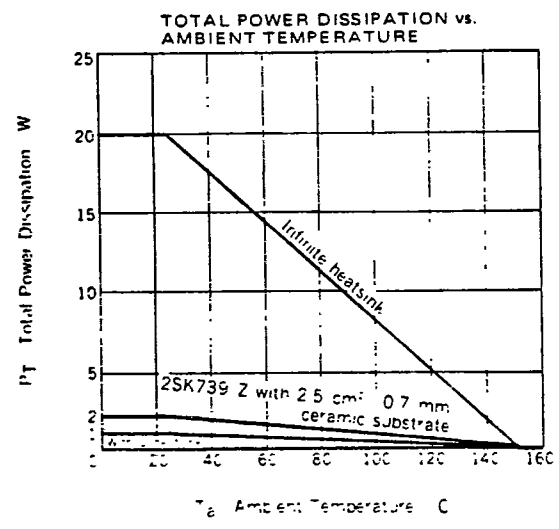
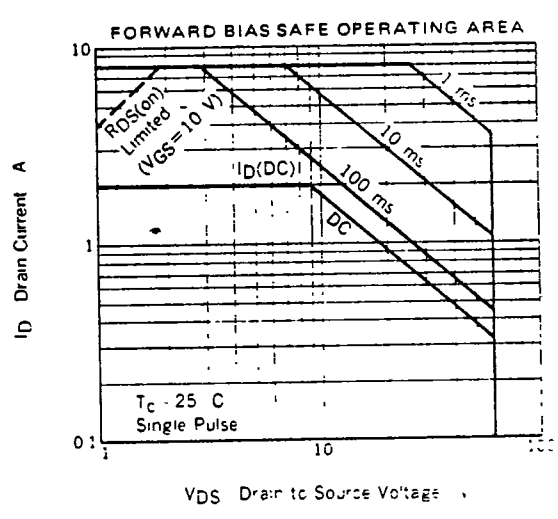
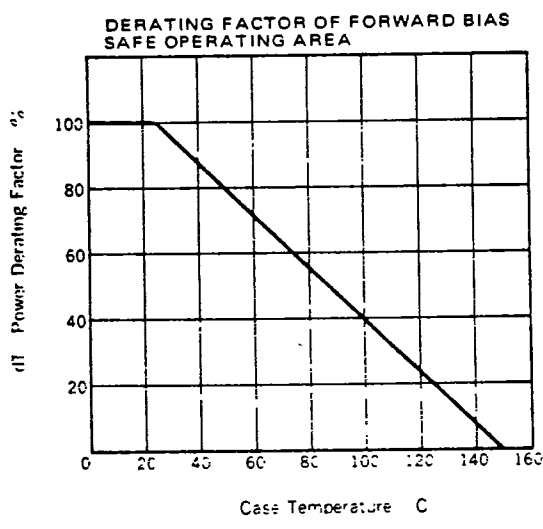


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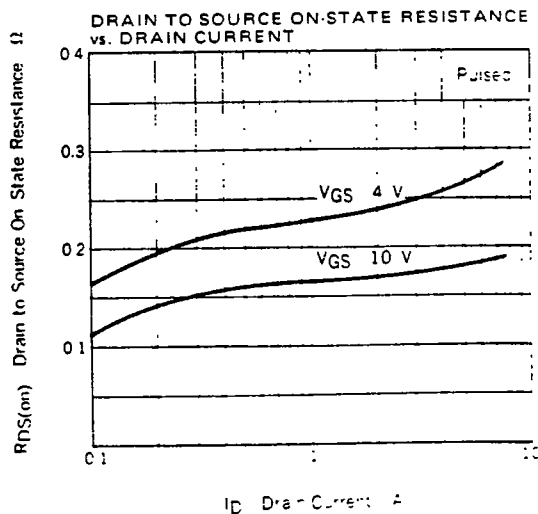
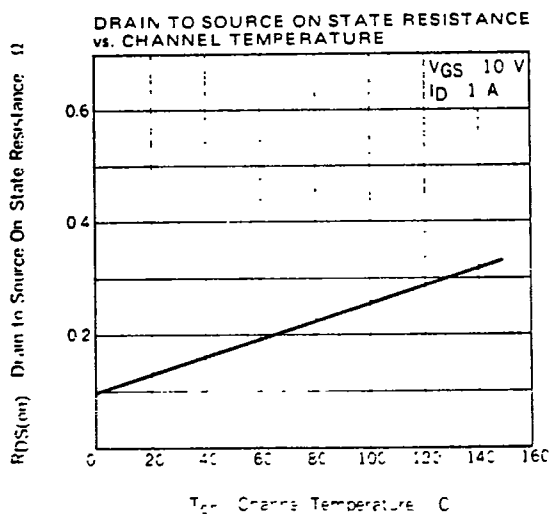
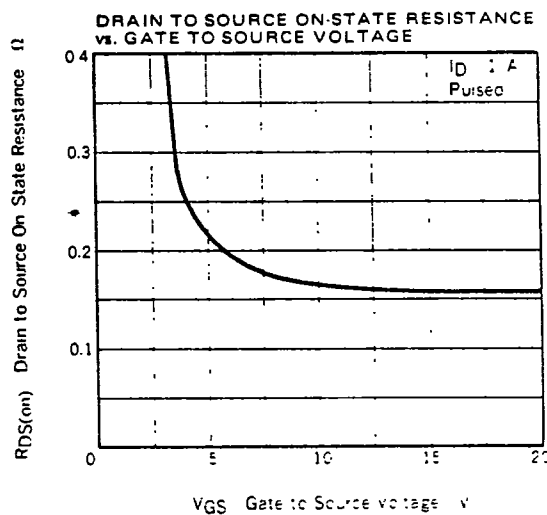
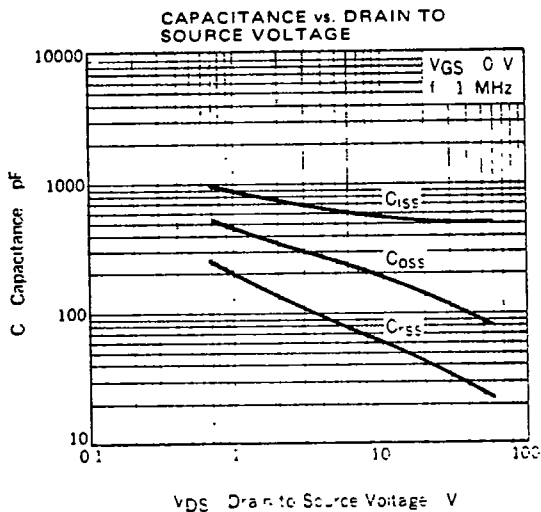
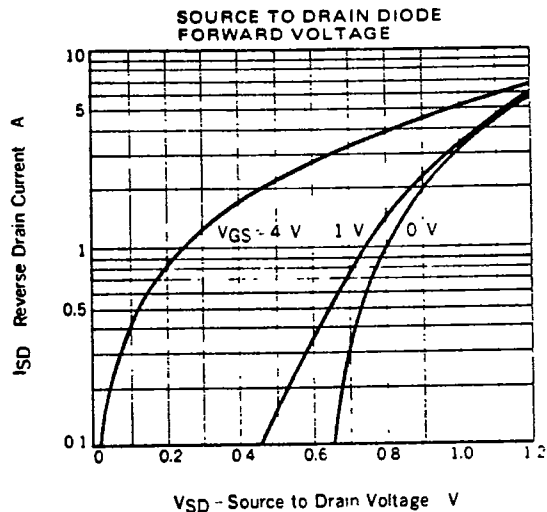
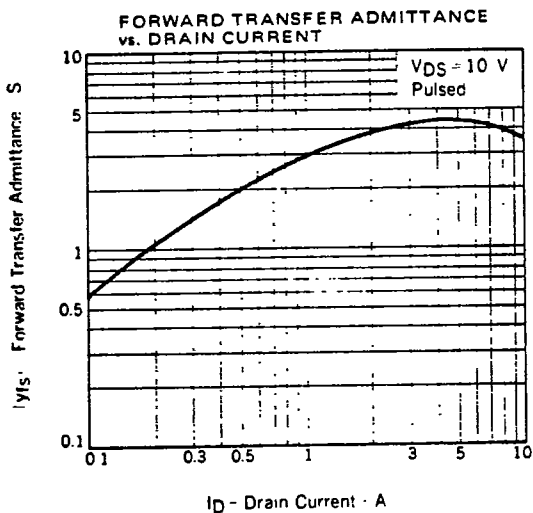


- 1. Gate
- 2. Drain
- 3. Source
- 4. Drain (Fin)

TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)

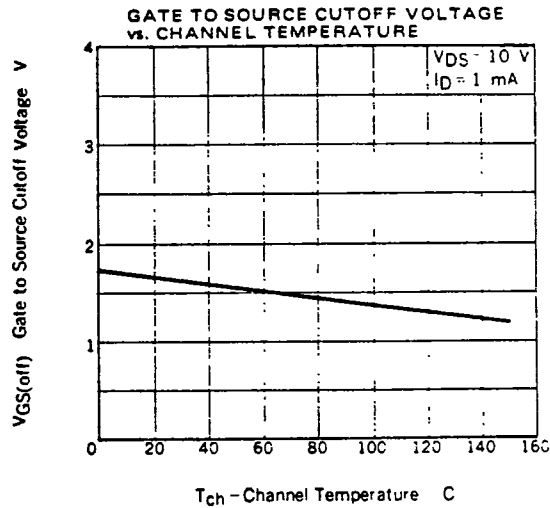
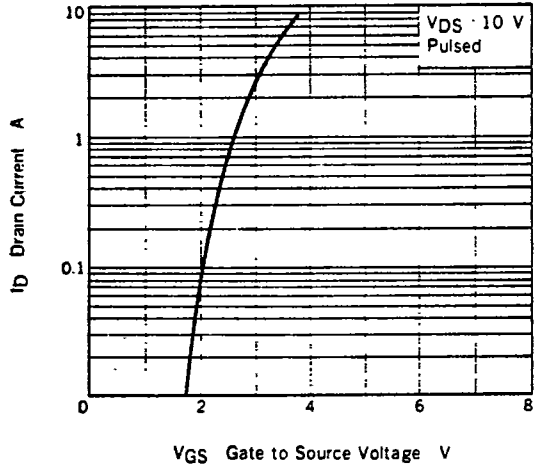


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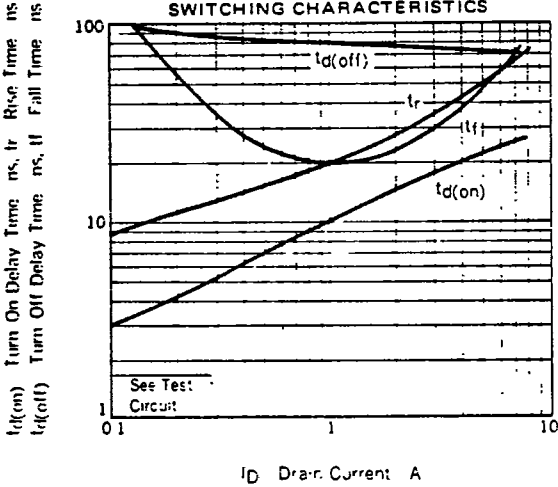


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TYPICAL TRANSFER CHARACTERISTICS



SWITCHING CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT

