25-W FILTER-FREE MONO CLASS-D AUDIO POWER AMPLIFIER with SPEAKER GUARD™

Check for Samples: TPA3112D1

FEATURES

- **25-W into an 8-Ω Load at < 0.1% THD+N From a 24-V Supply**
- **20-W into an 4-Ω Load at 10% THD+N From a 12-V Supply**
- **94% Efficient Class-D Operation into 8-Ω Load Eliminates Need for Heat Sinks**
- **Wide Supply Voltage Range Allows Operation from 8 to 26 V**
- **Filter-Free Operation**
- **SpeakerGuard™ Speaker Protection Includes Adjustable Power Limiter plus DC Protection**
- **Flow Through Pin Out Facilitates Easy Board Layout**
- **Robust Pin-to-Pin Short Circuit Protection and Thermal Protection with Auto-Recovery Option**
- **Excellent THD+N/ Pop Free Performance**
- **Four Selectable, Fixed Gain Settings**
- **Differential Inputs**

APPLICATIONS

- **Televisions**
- **Consumer Audio Equipment**

DESCRIPTION

The TPA3112D1 is a 25-W efficient, Class-D audio power amplifier for driving a bridge tied speaker. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection system includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The TPA3112D1 can drive a mono speaker as low as 4Ω. The high efficiency of the TPA3112D1, > 90%, eliminates the need for an external heat sink when playing music.

The outputs are fully protected against shorts to GND, V_{CC}, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

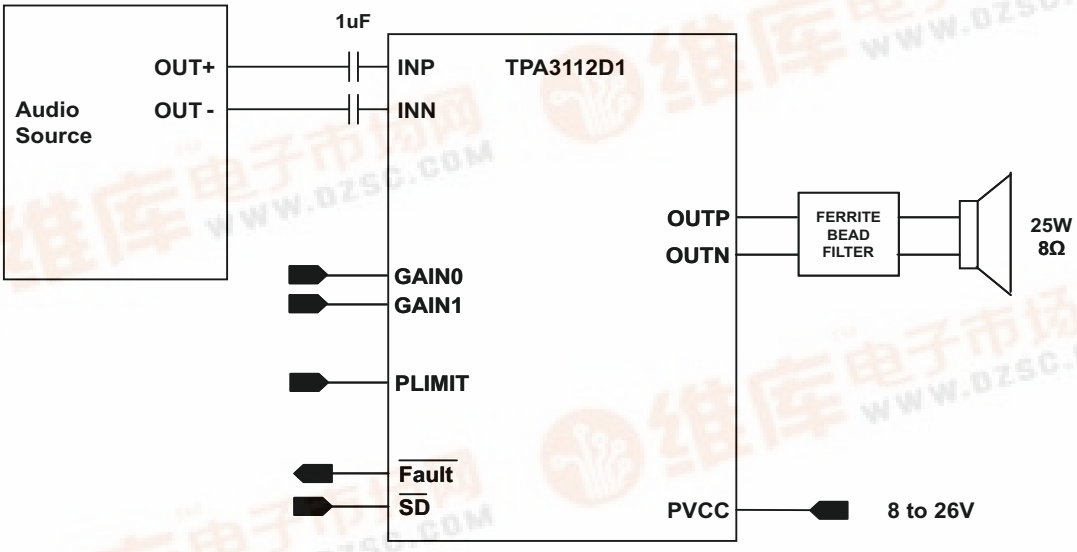


Figure 1. Simplified Application Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 V to 30 V
V_I	Interface pin voltage	$\overline{SD}$, $\overline{FAULT}$,GAIN0, GAIN1	–0.3 V to V_{CC} + 0.3 V
		PLIMIT	–0.3 V toGVDD + 0.3 V
		INN, INP	–0.3 V to 6.3 V
	Continuous total power dissipation		See Thermal Inforamtion Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range(2)		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
R_L	Minimum Load Resistance	BTL	3.2
	Electrostatic discharge	Human body model (3) (all pins)	±2 kV
		Charged-device model (4) (all pins)	±500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The TPA3112D1 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SCBA017D and SLUA271 for more information about using the QFN thermal pad. See TI Technical Briefs SLMA002 for more information about using the HTQFP thermal pad.
(3) In accordance with JEDEC Standard 22, Test Method A114-B.
(4) In accordance with JEDEC Standard 22, Test Method C101-A

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPA3112D1 PWP (28 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.5	
θ_{JB}	Junction-to-board thermal resistance	17.5	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	7.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, R_{PULLUP}=100kΩ, V_{CC}=26V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 2, V_{CC} = 18 V		50	µA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 0.8V, V_{CC} = 18 V		5	µA
T_A	Operating free-air temperature		–40	85	°C

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PVcc=21V			40		mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PVcc=21V			400		µA
$r_{DS(on)}$	Drain-source on-state resistance	I_O = 500 mA, T_J = 25°C	High Side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ = 2 V			10		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 2mA		6.5	6.9	7.3	V

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PVcc=12V			20		mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PVcc=12V			200		µA
$r_{DS(on)}$	Drain-source on-state resistance	I_O = 500 mA, T_J = 25°C	High Side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ = 2 V			10		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 2mA		6.5	6.9	7.3	V
PLIMIT	Output Voltage maximum under PLIMIT control	V_{PLIMIT}=2.0 V; V_I=6.0V differential		6.75	7.90	8.75	V

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

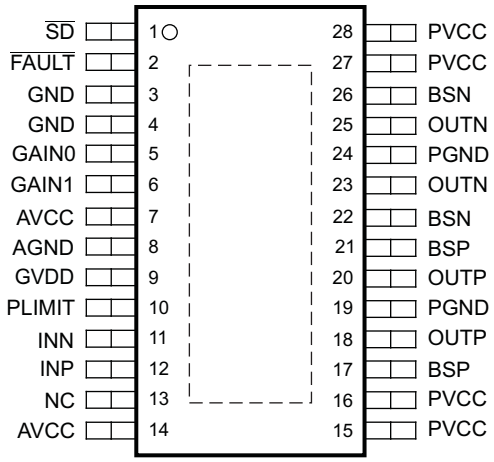
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N ≤ 0.1%, f = 1 kHz, V_{CC} = 24 V		25		W
THD+N	Total harmonic distortion + noise	V_{CC} = 24 V, f = 1 kHz, P_O = 12 W (half-power)		<0.05		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–70		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N ≤ 10%, f = 1 kHz , R_L = 8Ω		10		W
P_O	Continuous output power	THD+N ≤ 10%, f = 1 kHz , R_L = 4Ω		20		W
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 5 W (half-power)		<0.06		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	P_o = 1 W, Gain = 20 dB, f = 1 kHz		–70		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

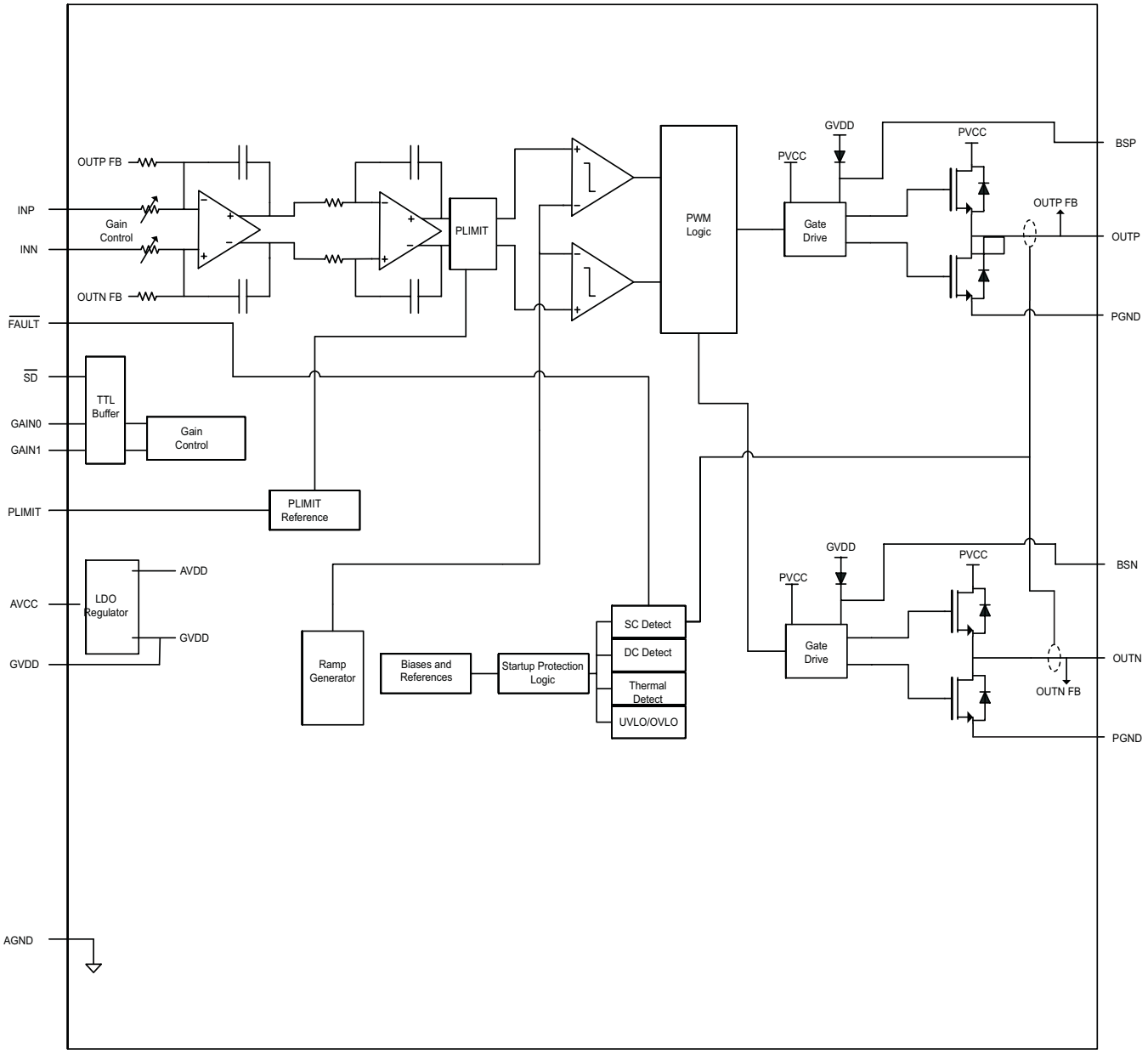
PWP (TSSOP) Package
(Top View)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	Pin #		
$\overline{SD}$	1	I	Shutdown logic input for audio amp(LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise both the short circuit faults and dc detect faults must be reset by cycling PVCC.
GND	3		Connect to local ground
GND	4		Connect to local ground
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply.
AGND	8		Analog supply ground. Connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 7V. May also be used as supply for PLILMIT divider. Add a 1μF cap to ground at this pin.
PLIMIT	10	I	Power limit level adjust. Connect directly to GVDD pin for no power limiting. Add a 1μF cap to ground at this pin.
INN	11	I	Negative audio input. Biased at 3V.
INP	12	I	Positive audio input. Biased at 3V.
NC	13		Not connected
AVCC	14	P	Connect AVCC supply to this pin
PVCC	15	P	Power supply for H-bridge. PVCC pins are also connected internally.
PVCC	16	P	Power supply for H-bridge. PVCC pins are also connected internally.
BSP	17	I	Bootstrap I/O for positive high-side FET.
OUTP	18	O	Class-D H-bridge positive output.
PGND	19		Power ground for the H-bridges.
OUTP	20	O	Class-D H-bridge positive output.
BSP	21	I	Bootstrap I/O for positive high-side FET.
BSN	22	I	Bootstrap I/O for negative high-side FET.
OUTN	23	O	Class-D H-bridge negative output.
PGND	24		Power ground for the H-bridges.
OUTN	25	O	Class-D H-bridge negative output.
BSN	26	I	Bootstrap I/O for negative high-side FET.
PVCC	27	P	Power supply for H-bridge. PVCC pins are also connected internally.
PVCC	28	P	Power supply for H-bridge. PVCC pins are also connected internally.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3112D2 EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION vs FREQUENCY

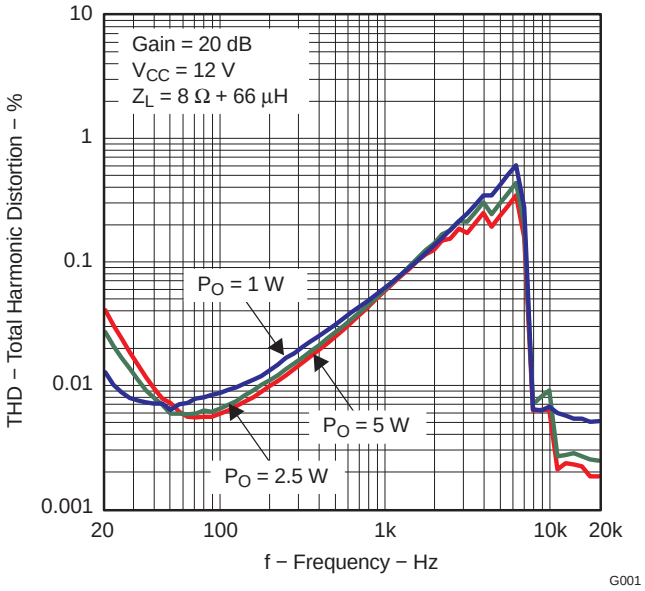


Figure 2.

TOTAL HARMONIC DISTORTION vs FREQUENCY

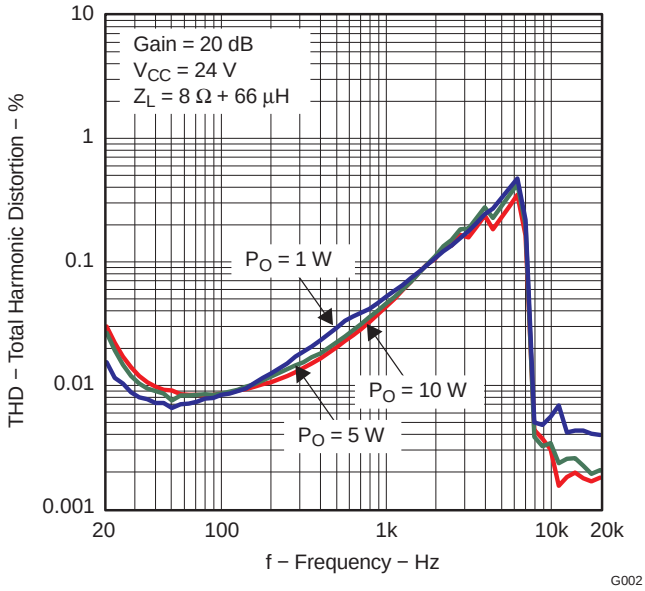


Figure 3.

TOTAL HARMONIC DISTORTION vs FREQUENCY

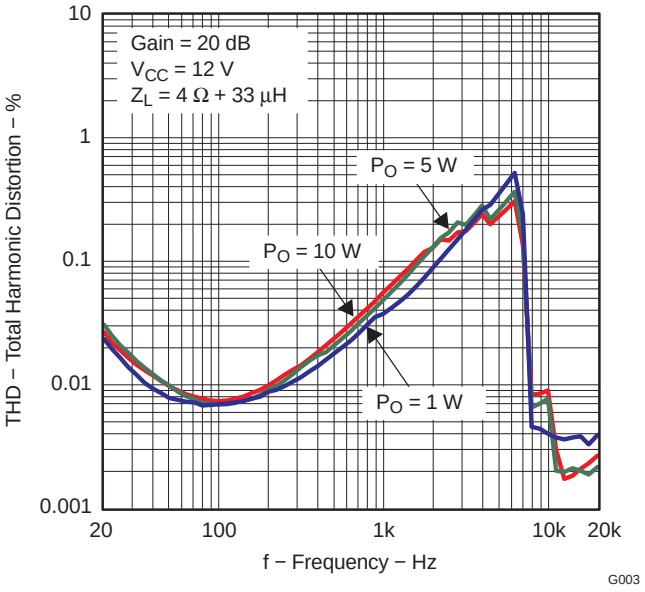


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

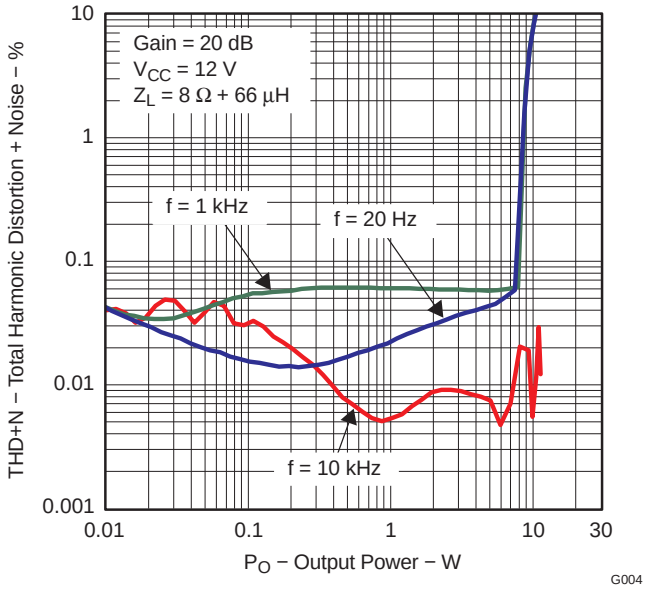
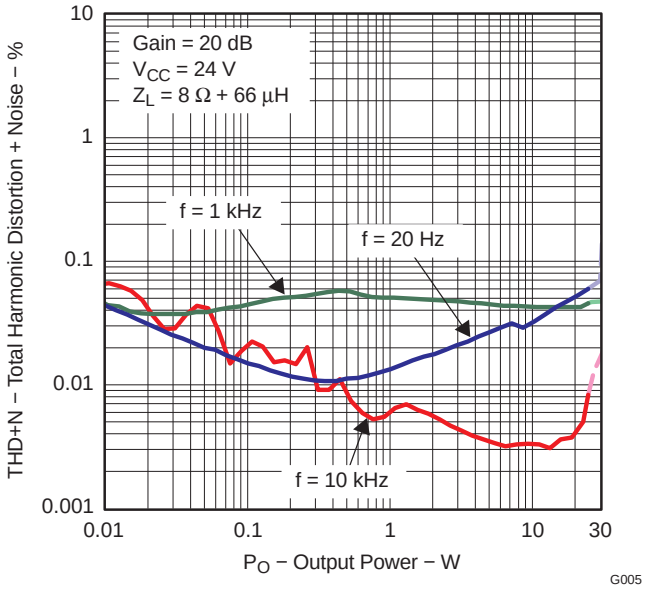


Figure 5.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3112D2 EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER



Note: Dashed lines represent thermally limited region.

Figure 6.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

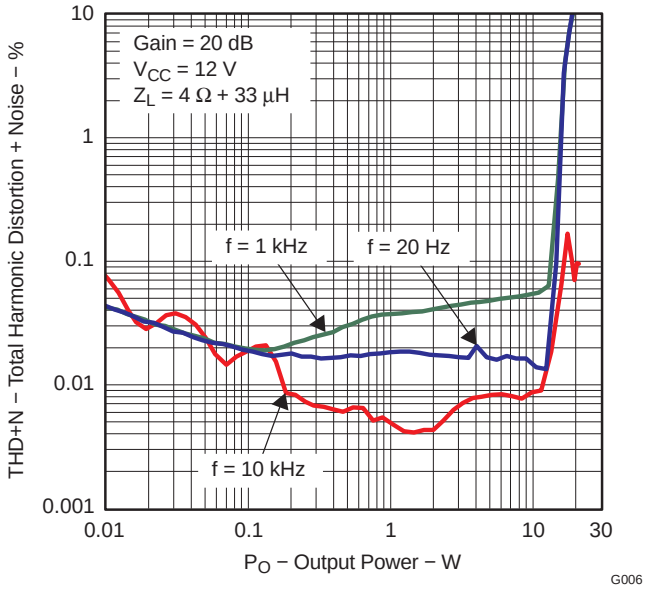
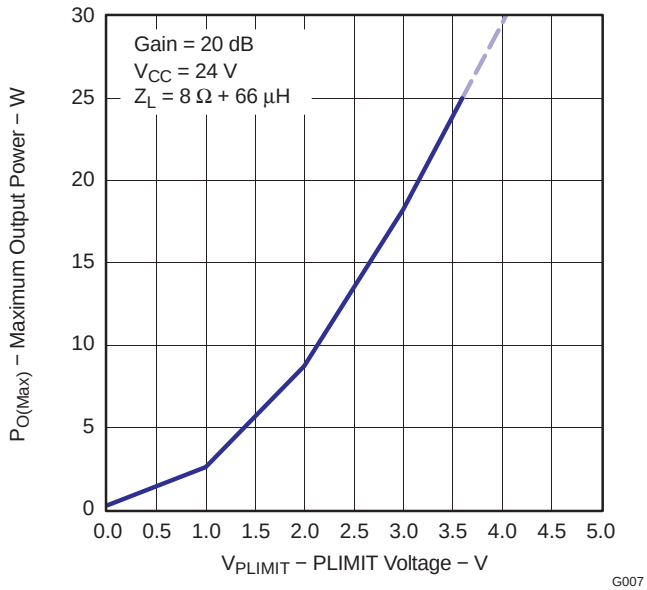


Figure 7.

MAXIMUM OUTPUT POWER vs PLIMIT VOLTAGE



Note: Dashed line represents thermally limited region.

Figure 8.

OUTPUT POWER vs PLIMIT VOLTAGE

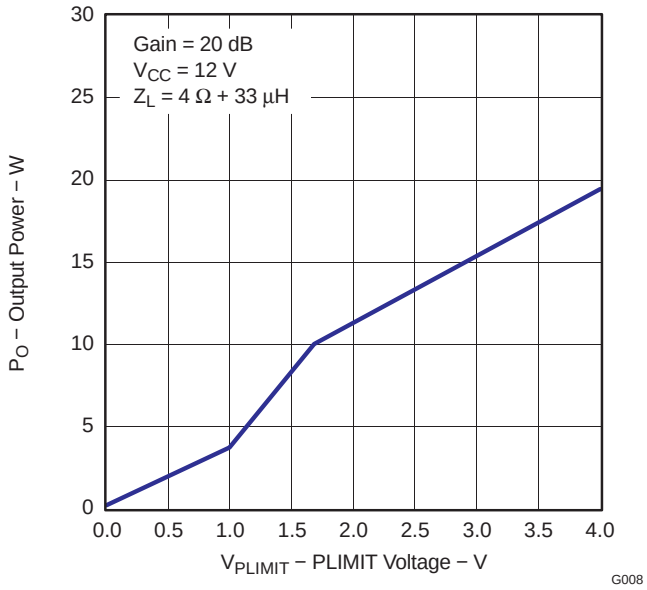


Figure 9.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3112D2 EVM which is available at ti.com.)

GAIN/PHASE vs FREQUENCY

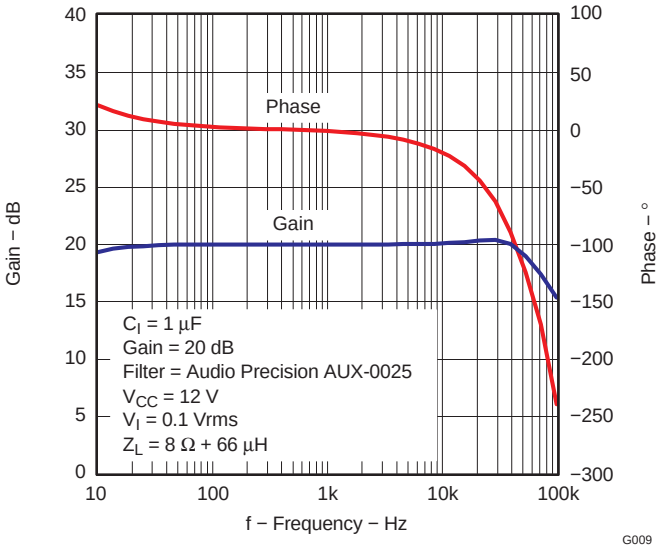
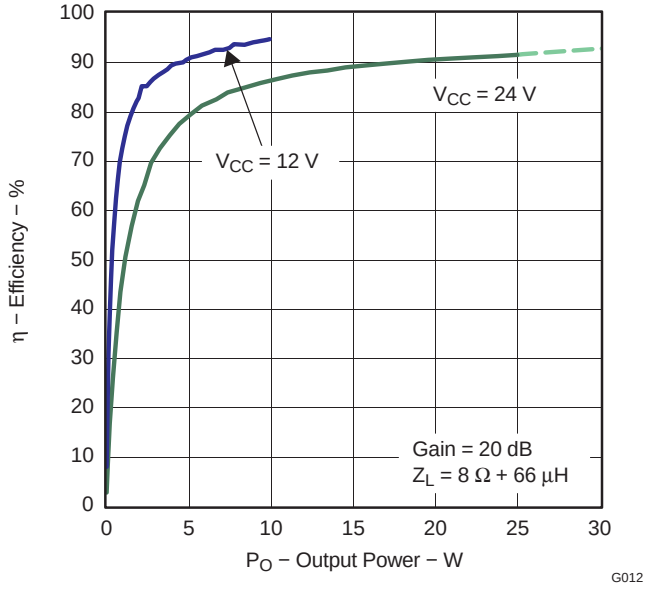


Figure 10.

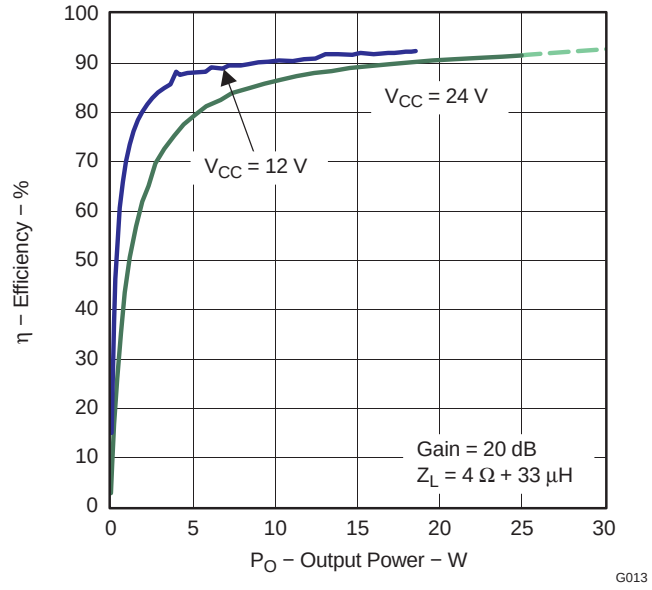
EFFICIENCY vs OUTPUT POWER



Note: Dashed line represents thermally limited region.

Figure 11.

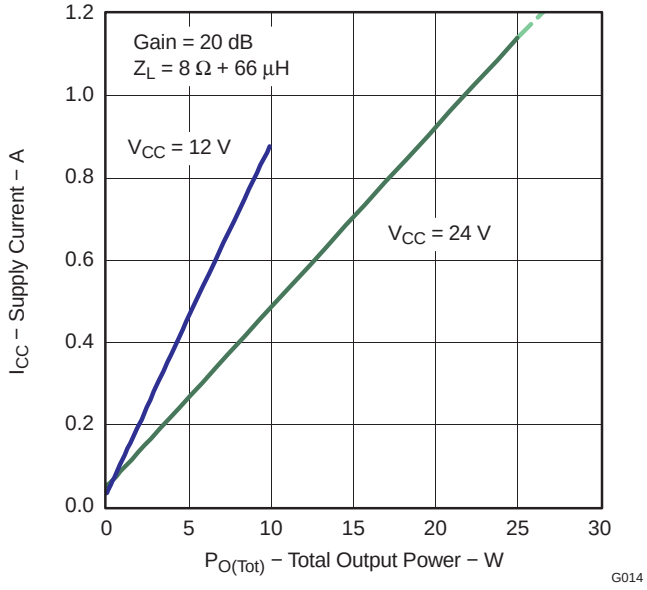
EFFICIENCY vs OUTPUT POWER



Note: Dashed line represents thermally limited region.

Figure 12.

SUPPLY CURRENT vs TOTAL OUTPUT POWER



Note: Dashed line represents thermally limited region.

Figure 13.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3112D2 EVM which is available at ti.com.)

SUPPLY CURRENT vs TOTAL OUTPUT POWER

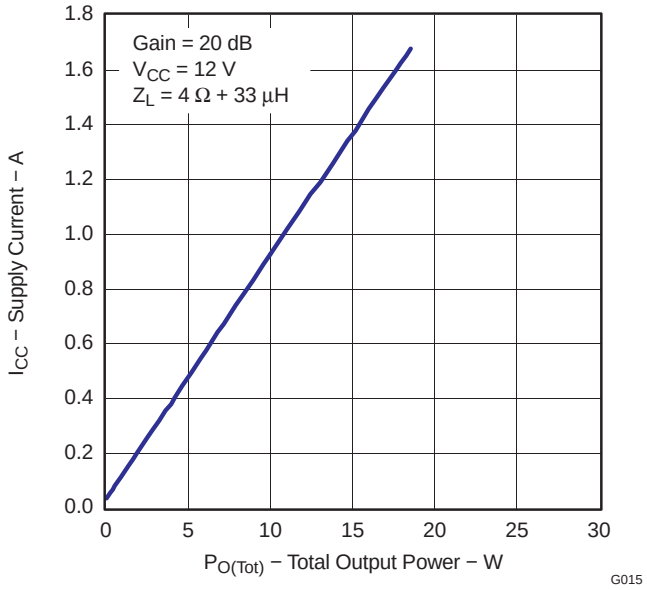


Figure 14.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

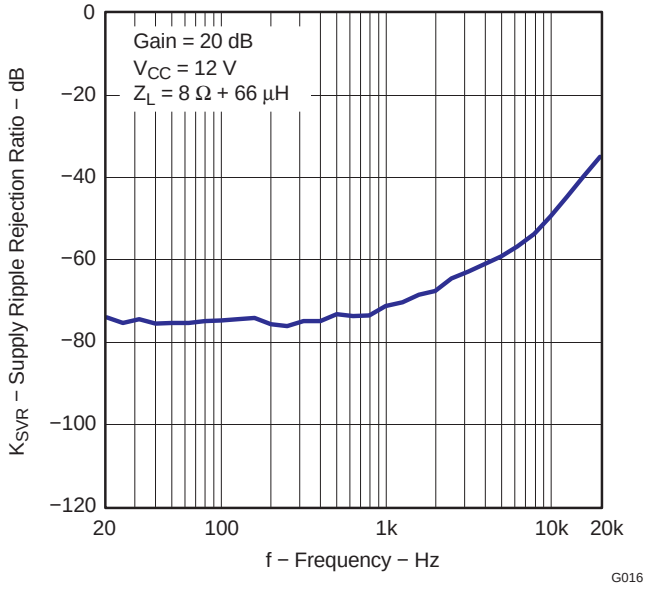


Figure 15.

DEVICE INFORMATION

Gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3112D1 is set by two input terminals, GAIN0 and GAIN1. The voltage slew rate of these gain terminals, along with terminals 1 and 14, must be restricted to no more than 10V/ms. For higher slew rates, use a 100kΩ resistor in series with the terminals.

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the TPA3112D1. At the lower gain settings, the input impedance could increase as high as 72 kΩ

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

SD OPERATION

The TPA3112D1 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{SD}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

PLIMIT

The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1μF capacitor from pin 10 to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

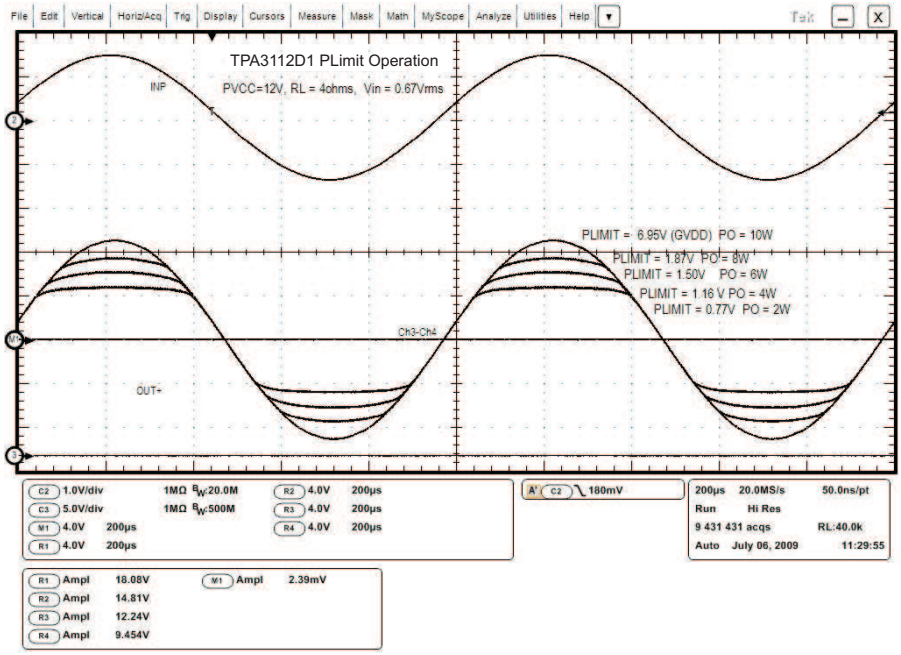


Figure 16. PLIMIT Circuit Operation

The PLIMIT circuits sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a “virtual” voltage rail which is lower than the supply connected to PVCC. This “virtual” rail is 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$ for unclipped power (1)

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P

P_{OUT}(10%THD) = 1.25 × P_{OUT}(unclipped)

Table 2. PLIMIT Typical Operation

Test Conditions ()	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (V_{P-P})
PVCC=24V, Vin=1Vrms, RL=4Ω, Gain=20dB	6.97	22.1	26.9
PVCC=24V, Vin=1Vrms, RL=4Ω, Gain=20dB	1.92	10	15.0
PVCC=24V, Vin=1Vrms, RL=4Ω, Gain=20dB	1.24	5	10.0
PVCC=12V, Vin=1Vrms, RL=4Ω, Gain=20dB	6.95	17.2	20.9
PVCC=12V, Vin=1Vrms, RL=4Ω, Gain=20dB	1.75	10	15.3
PVCC=12V, Vin=1Vrms, RL=4Ω, Gain=20dB	1.20	5	10.3

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also used to supply the PLIMIT voltage divider circuit. Add a 1μF capacitor to ground at this pin.

DC Detect

TPA3112D1 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the $\overline{\text{FAULT}}$ pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling $\overline{\text{SD}}$ will NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle exceeds 14% (eg. +57%, -43%) for more than 420 ms at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the $\overline{\text{SD}}$ pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative input to avoid nuisance DC detect faults.

The minimum differential input voltages required to trigger the DC detect are shown in Table Table 3. The inputs must remain at or above the voltage listed in the table for more than 420 ms to trigger the DC detect.

Table 3. DC Detect Threshold

AV(dB)	Vin (mV, differential)
20	112
26	56
32	28
36	17

SHORT-CIRCUIT PROTECTION AND AUTOMATIC RECOVERY FEATURE

TPA3112D2 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This will allow the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which will clear the short circuit protection latch.

THERMAL PROTECTION

Thermal protection on the TPA3112D1 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ terminal.

APPLICATION INFORMATION

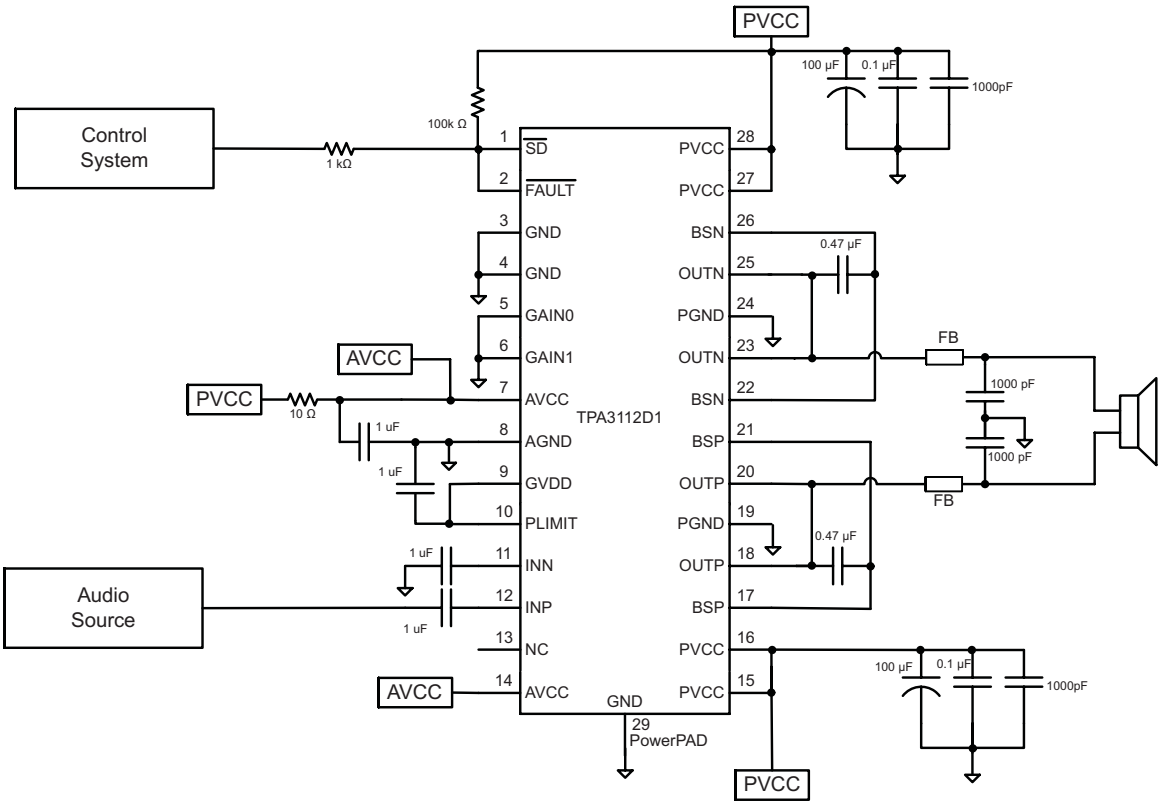


Figure 17. Mono Class-D Amplifier with BTL Output

CLASS-D OPERATION

This section focuses on the class-D operation of the TPA3112D1.

TPA3112D1 Modulation Scheme

The TPA3112D1 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

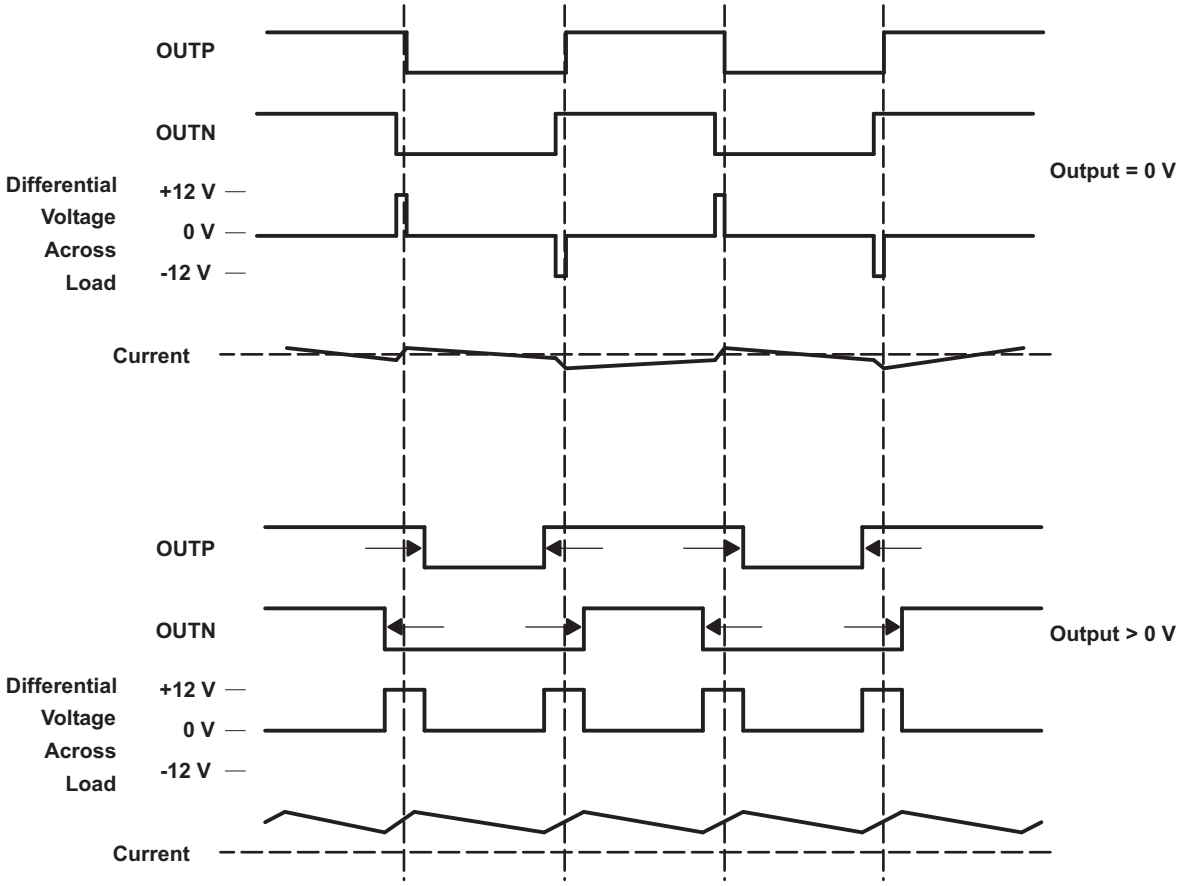


Figure 18. The TPA3112D1 Output Voltage and Current Waveforms Into an Inductive Load

Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3112D1 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. it is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class D amplifier. Many of the specifications regulating consumer electronics have

emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at very low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3112D2 include 28L0138-80R-10 and HI1812V101R-10 from Steward and the 742792510 from Wurth Electronics.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 ohms in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the PowerPad™ beneath the chip.

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 x V_{CC}, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3112D1 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of 2 x V_{CC}. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

When to Use an Output Filter for EMI Suppression

The TPA3112D1 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3112D1 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are circuits near which are sensitive to noise. Therefore, a classic second order Butterworth filter similar to those shown in Figure 19 through Figure 21 can be used.

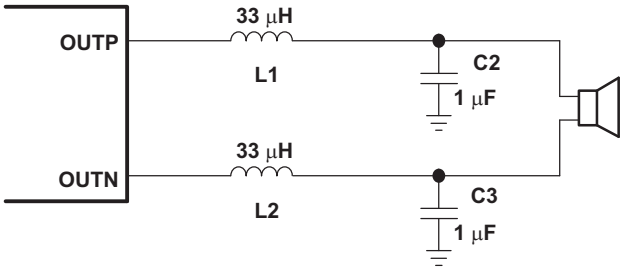


Figure 19. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

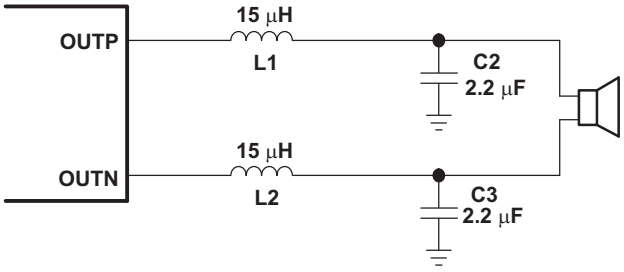


Figure 20. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4 Ω

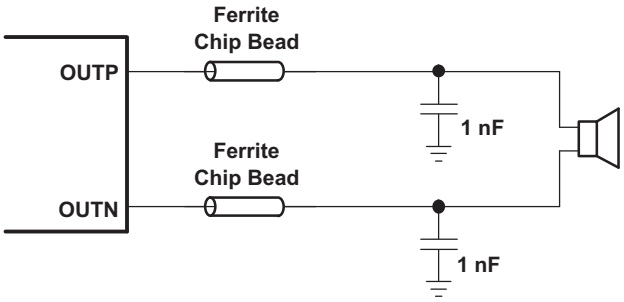
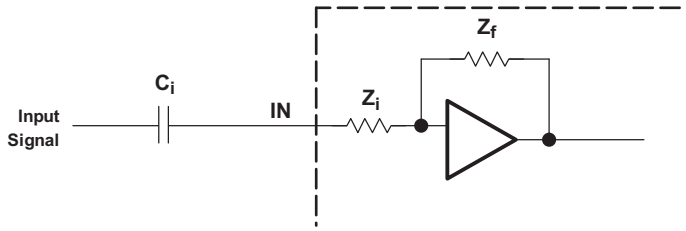


Figure 21. Typical Ferrite Chip Bead Filter (Chip Bead Example: Steward HI0805R800R-10)

INPUT RESISTANCE

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.



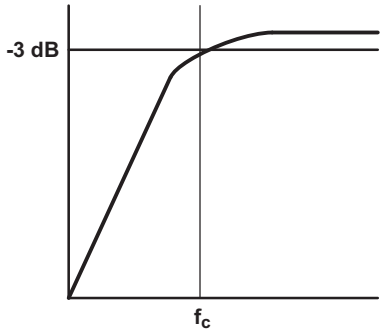
The -3-dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad (2)$$

INPUT CAPACITOR, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (3)$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (4)$$

In this example, C_I is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. If a ceramic capacitor is used, use a high quality capacitor with good temperature and voltage coefficient. An X7R type works well and if possible use a higher voltage rating than required. This will give a better C vs voltage characteristic. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

POWER SUPPLY DECOUPLING, C_S

The TPA3112D1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker.

Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond

wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 mF to 1 μF placed as close as possible to the device PVCC leads works best For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 mF or greater placed near the audio power amplifier is recommended. The 220 mF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220 μF or larger capacitor should be placed on each PVCC terminal. A 10 μF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

BSN and BSP CAPACITORS

The full H-bridge output stage uses only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 470-nF ceramic capacitor, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 470-nF capacitor must be connected from OUTP to BSP, and one 470-nF capacitor must be connected from OUTN to BSN. (See the application circuit diagram in Figure 1.)

The bootstrap capacitors connected between the BSx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

DIFFERENTIAL INPUTS

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3112D1 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3112D1 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14 msec power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

The TPA3112D1 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are very fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220 μF or greater) bulk power supply decoupling capacitors should be placed near the TPA3112D1 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-freqency cap of value between 0.1mF and 1mF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Output filter—The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm by 2.35 mm. Seven rows of solid vias (three vias per row, 0.33 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See TI Application Report SLMA002 for more information about using the TSSOP thermal pad.

For an example layout, see the TPA3112D1 Evaluation Module (TPA3112D1EVM) User Manual. Both the EVM user manual and the thermal pad application note are available on the TI Web site at http://www.ti.com.

REVISION HISTORY

Changes from Original (September 2009) to Revision A **Page**

- Added slew rate adjustment information 10
- Added updates for figure 17, pin 7 14

Changes from Revision A (July 2010) to Revision B **Page**

- In the BSN and BSP CAPACITORS section, the 220-nf capacitor rated for at least 25V was changed to a 470-nf capacitor rated to at least 16V 19

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TPA3112D1PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260
TPA3112D1PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260

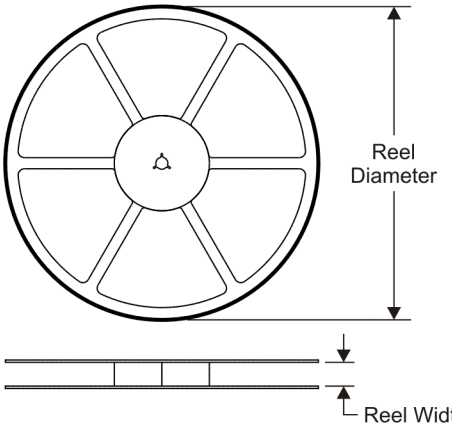
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

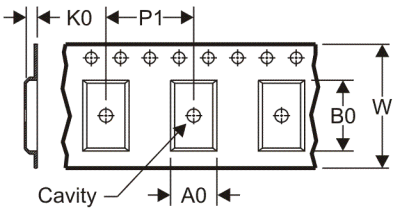
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

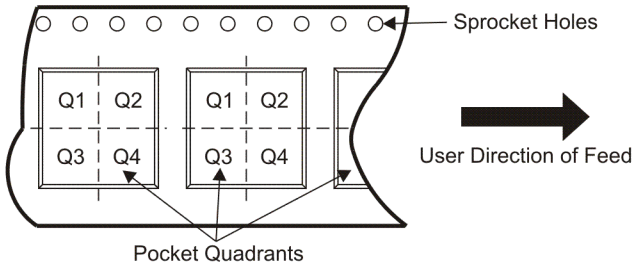


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

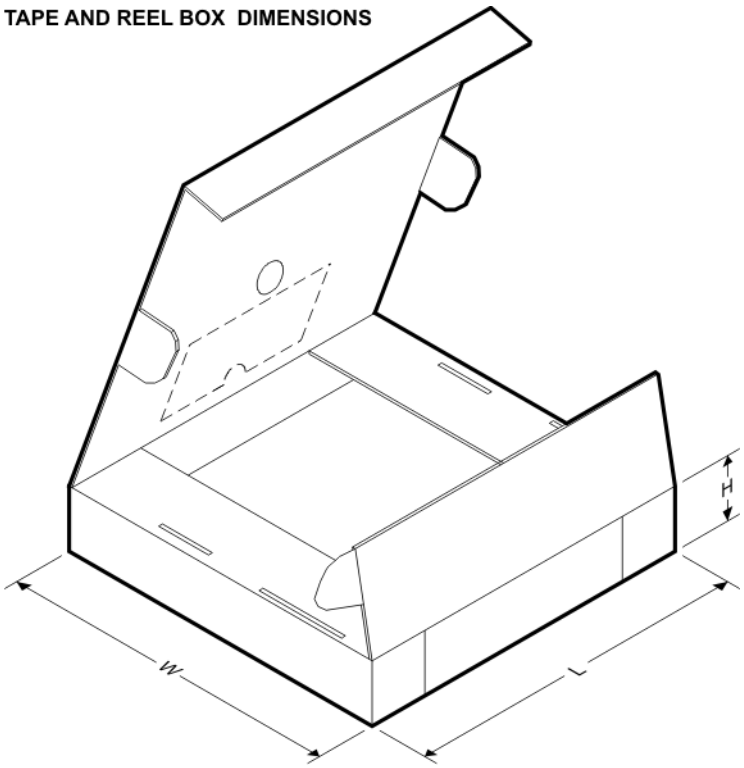
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3112D1PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

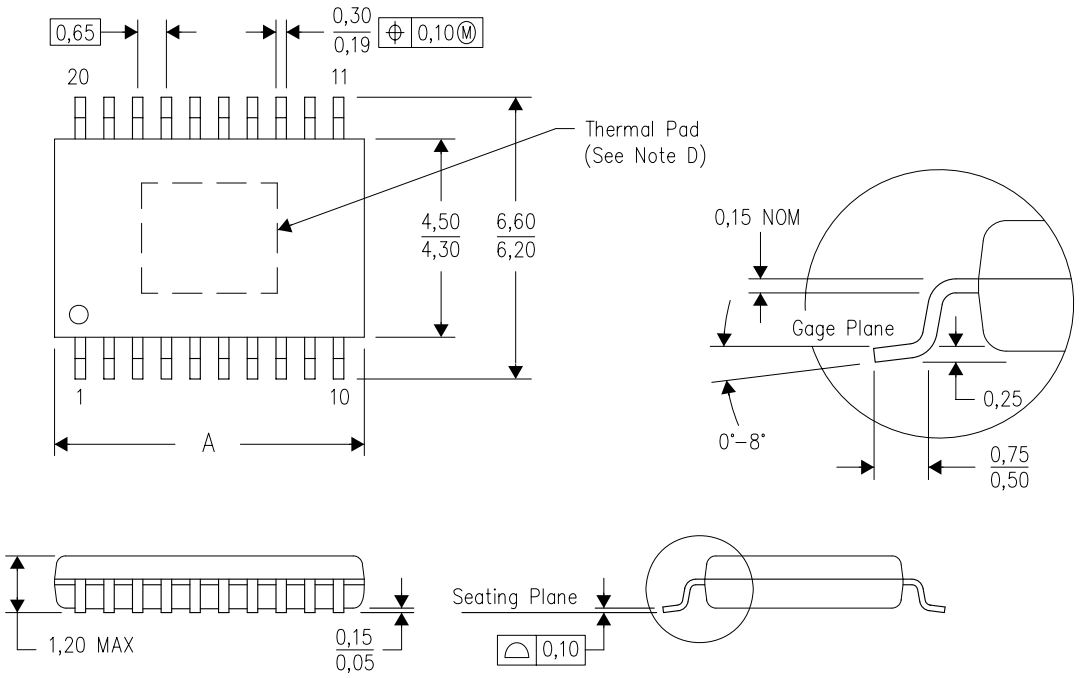


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3112D1PWPR	HTSSOP	PWP	28	2000	346.0	346.0	33.0

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

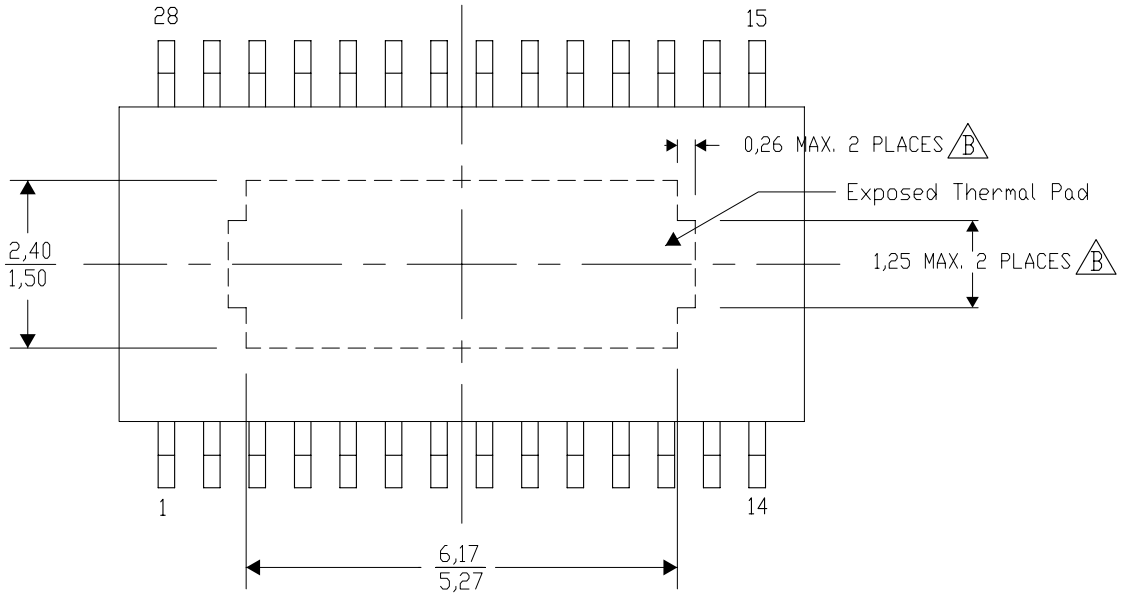
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

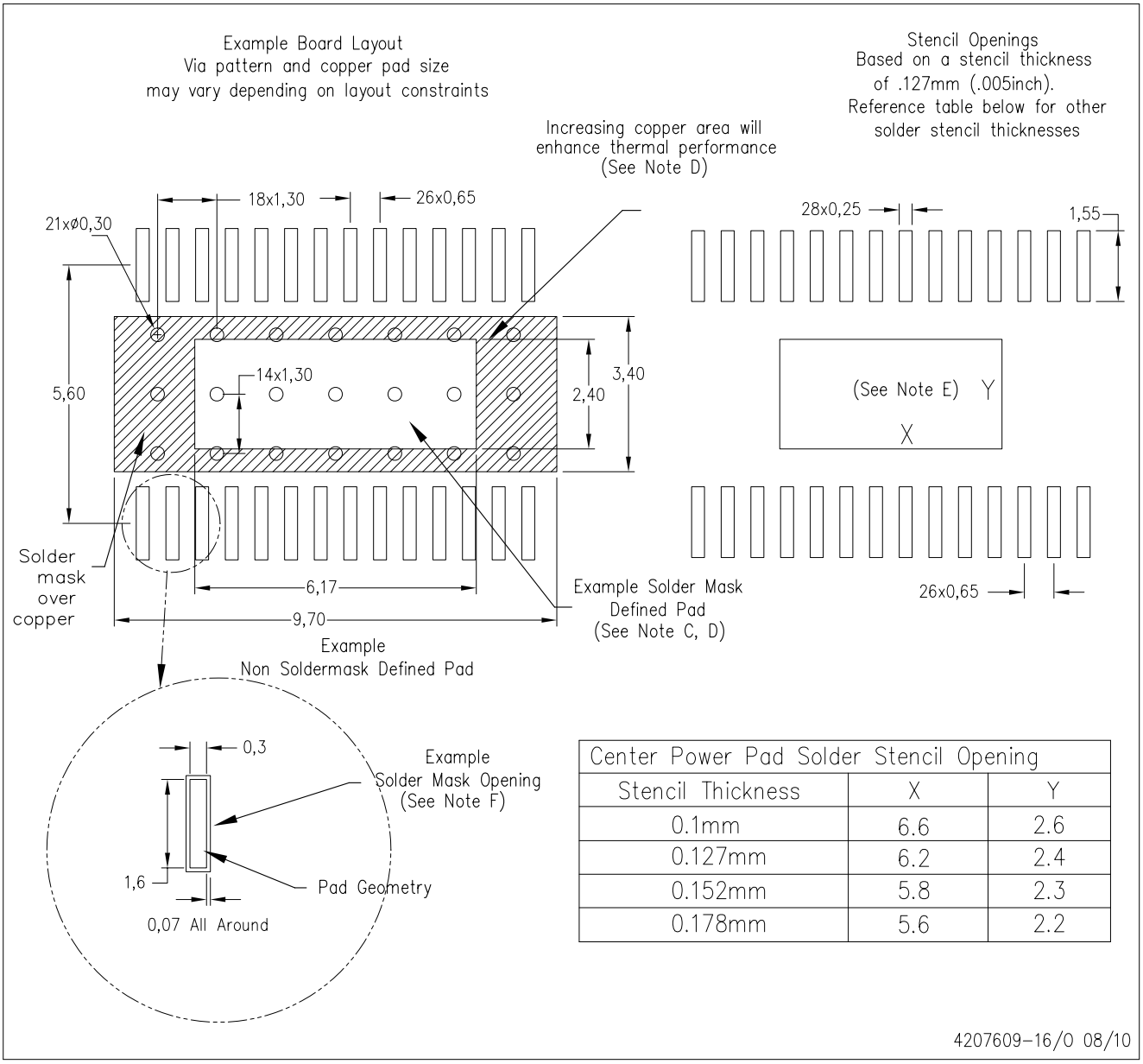
Exposed Thermal Pad Dimensions

4206332-21/S 11/10

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may vary in shape or may not be present.

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.2	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609-16/O 08/10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265