

International IR Rectifier

PD - 97352A

IRLR8729PbF IRLU8729PbF

HEXFET® Power MOSFET

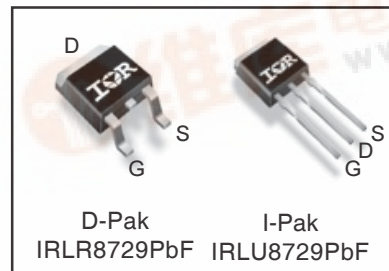
Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use

Benefits

- Very Low RDS(on) at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free
- RoHS compliant

V _{DSS}	R _{DS(on)} max	Qg
30V	8.9mΩ	10nC



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Parameter	Max.	Units
V _{DS}	30	V
V _{GS}	± 20	
I _D @ T _C = 25°C	58 ^④	A
I _D @ T _C = 100°C	41 ^④	
I _{DM}	260	
P _D @ T _C = 25°C	55	W
P _D @ T _C = 100°C	27	
	0.37	W/°C
T _J	-55 to + 175	°C
T _{STG}		
	300 (1.6mm from case)	

Thermal Resistance

Parameter	Typ.	Max.	Units
R _{θJC}	—	2.73	°C/W
R _{θJA}	—	50	
R _{θJA}	—	110	

ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.

Notes ① through ⑤ are on page 11

IRLR/U8729PbF

International
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Static @ T_J = 25°C (unless otherwise specified)

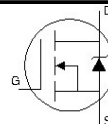
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	21	—	mV/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	6.0	8.9	mΩ	V _{GS} = 10V, I _D = 25A ③
		—	8.9	11.9		V _{GS} = 4.5V, I _D = 20A ③
V _{GS(th)}	Gate Threshold Voltage	1.35	1.8	2.35	V	V _{DS} = V _{GS} , I _D = 25μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-6.2	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	91	—	—	S	V _{DS} = 15V, I _D = 20A
Q _g	Total Gate Charge	—	10	16	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 20A See Fig. 16
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	2.1	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	1.3	—		
Q _{gd}	Gate-to-Drain Charge	—	4.0	—		
Q _{godr}	Gate Charge Overdrive	—	2.6	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	4.8	—		
Q _{oss}	Output Charge	—	6.3	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	1.6	2.7	Ω	
t _{d(on)}	Turn-On Delay Time	—	10	—	ns	V _{DD} = 15V, V _{GS} = 4.5V ③ I _D = 20A R _G = 1.8Ω See Fig. 14
t _r	Rise Time	—	47	—		
t _{d(off)}	Turn-Off Delay Time	—	11	—		
t _f	Fall Time	—	10	—		
C _{iss}	Input Capacitance	—	1350	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	280	—		
C _{rss}	Reverse Transfer Capacitance	—	120	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	74	mJ
I _{AR}	Avalanche Current ①	—	20	A
E _{AR}	Repetitive Avalanche Energy ①	—	5.5	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	58④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	260		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 20A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	16	24	ns	T _J = 25°C, I _F = 20A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	19	29	nC	di/dt = 300A/μs ③
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



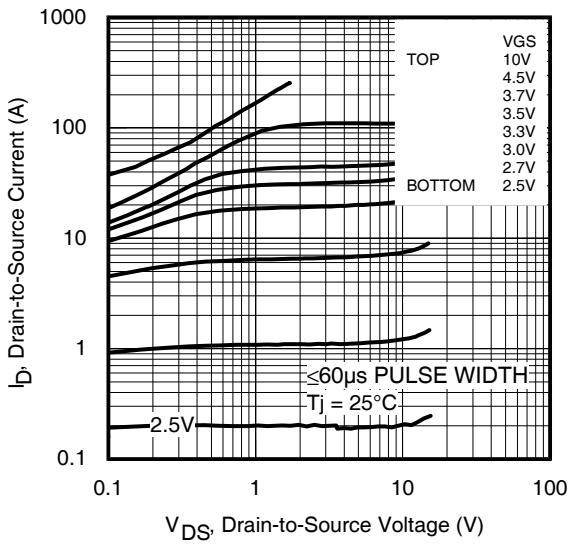


Fig 1. Typical Output Characteristics

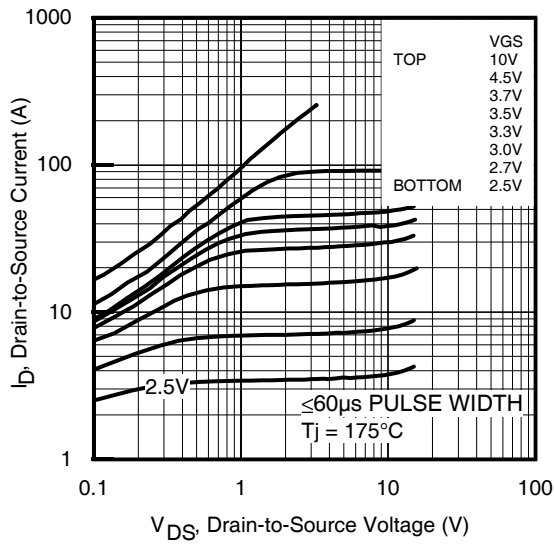


Fig 2. Typical Output Characteristics

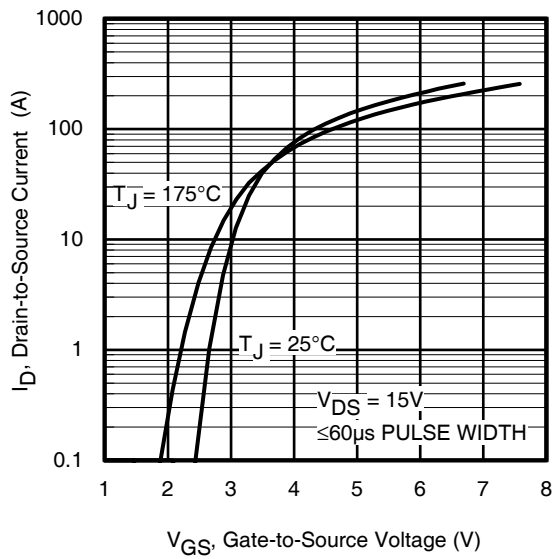


Fig 3. Typical Transfer Characteristics

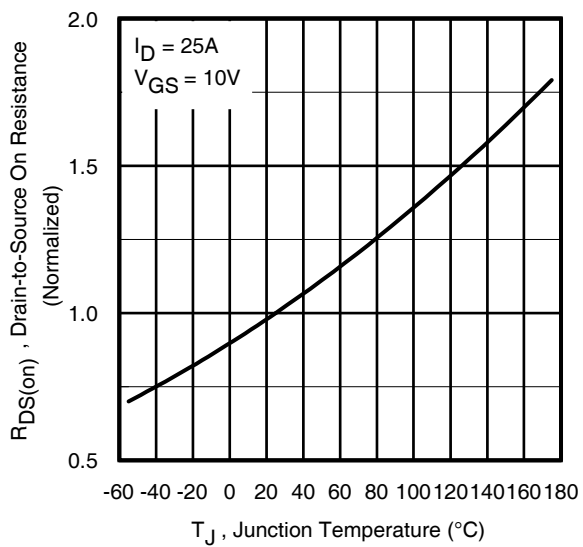


Fig 4. Normalized On-Resistance vs. Temperature

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IR Rectifier

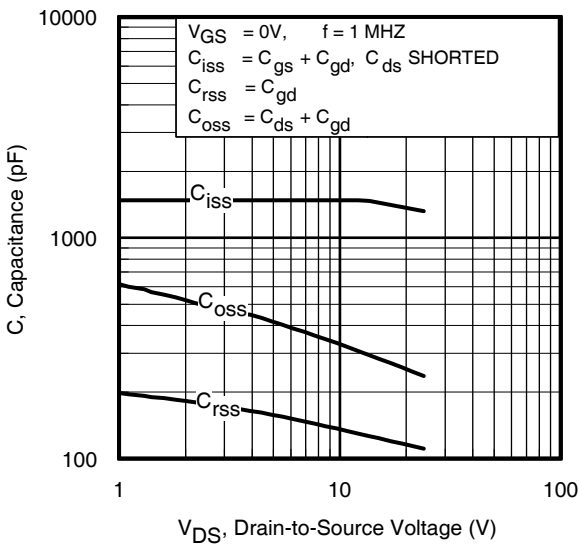


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

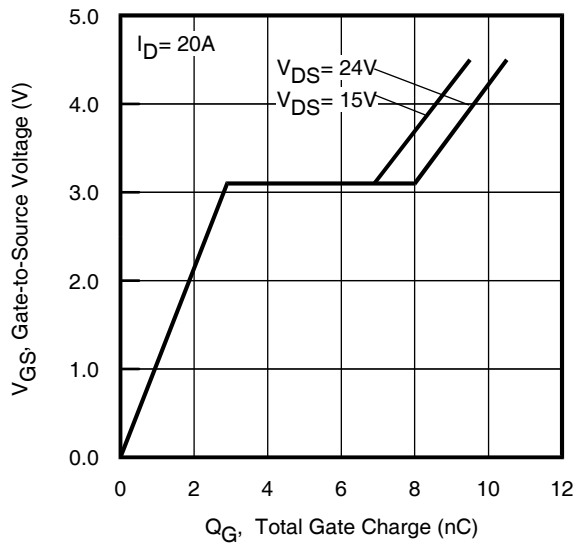


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

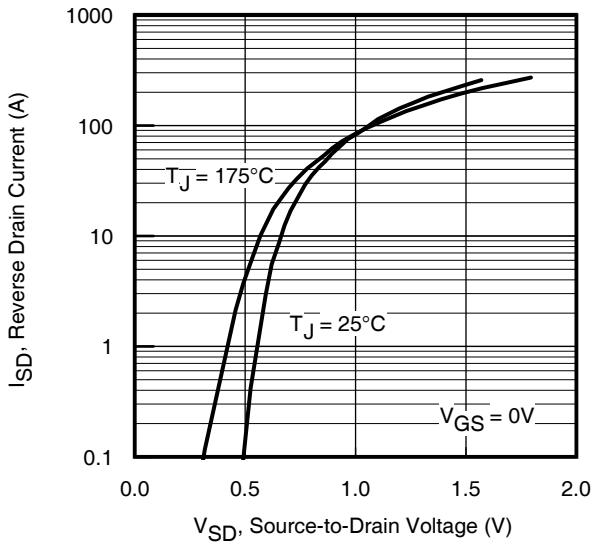


Fig 7. Typical Source-Drain Diode Forward Voltage

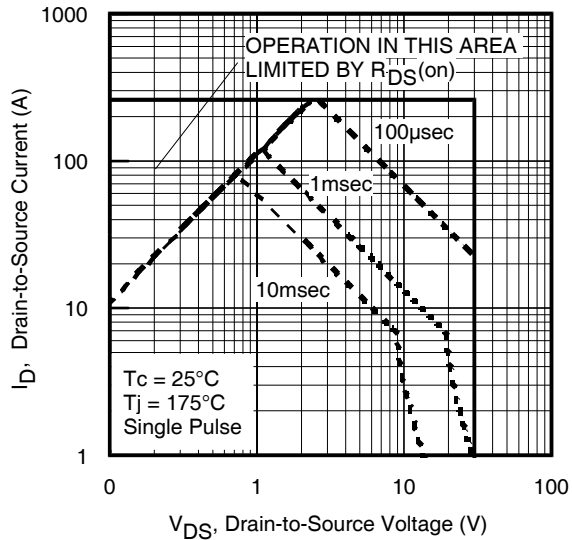


Fig 8. Maximum Safe Operating Area

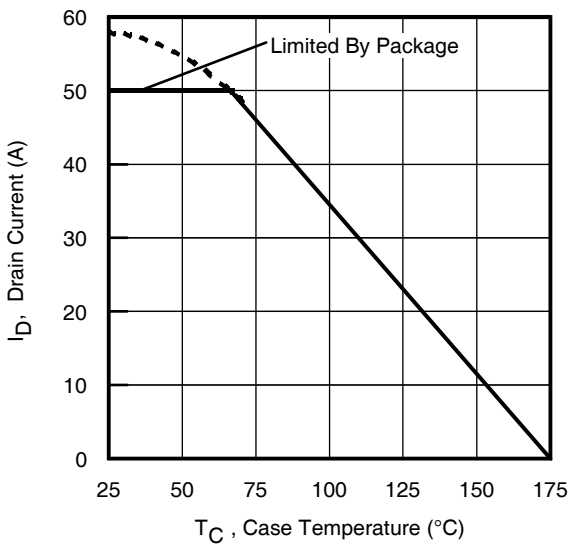


Fig 9. Maximum Drain Current vs. Case Temperature

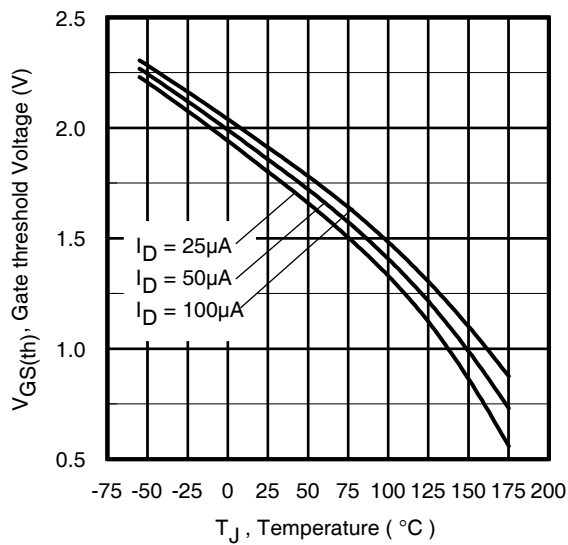


Fig 10. Threshold Voltage vs. Temperature

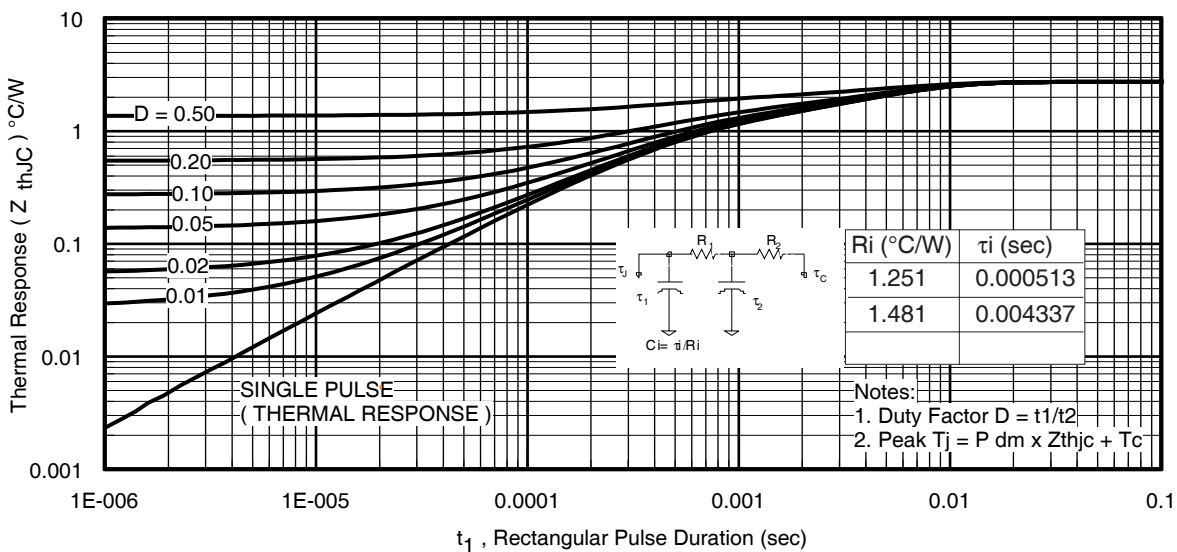


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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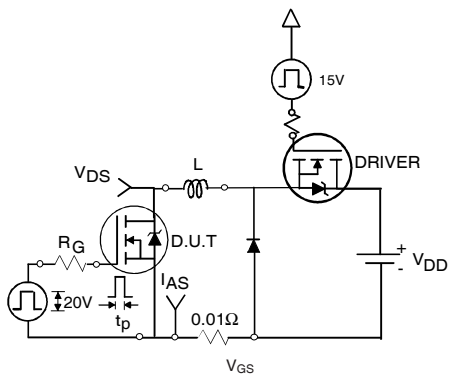


Fig 12a. Unclamped Inductive Test Circuit

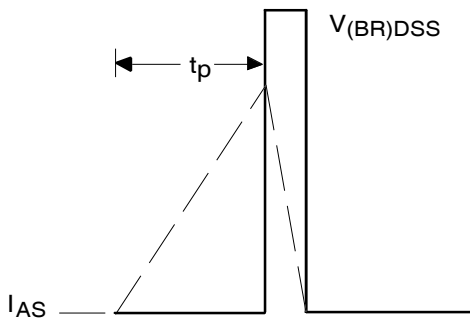


Fig 12b. Unclamped Inductive Waveforms

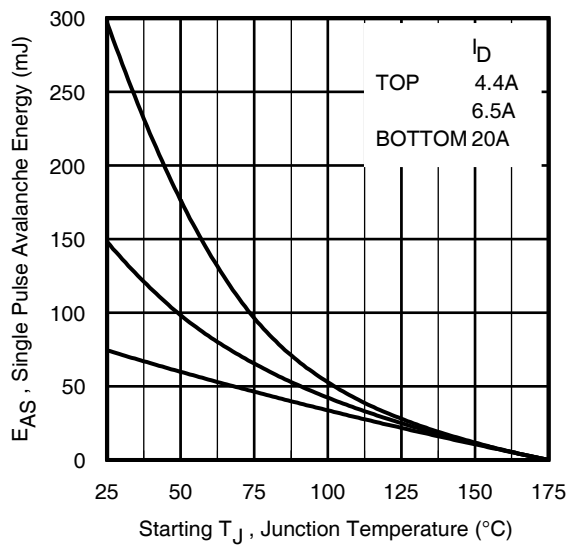


Fig 12c. Maximum Avalanche Energy vs. Drain Current

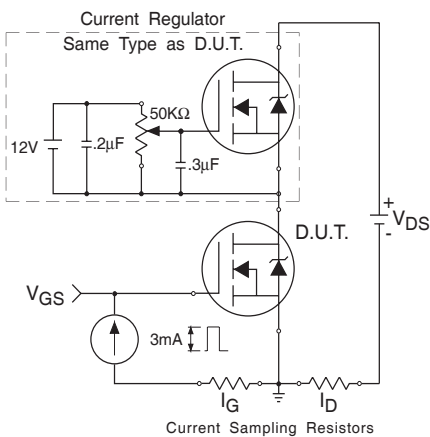


Fig 13. Gate Charge Test Circuit

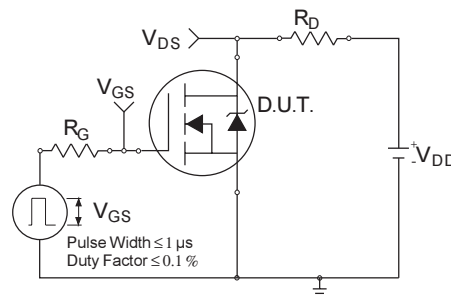


Fig 14a. Switching Time Test Circuit

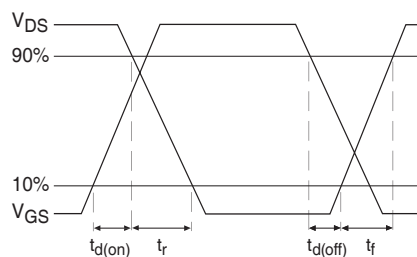


Fig 14b. Switching Time Waveforms

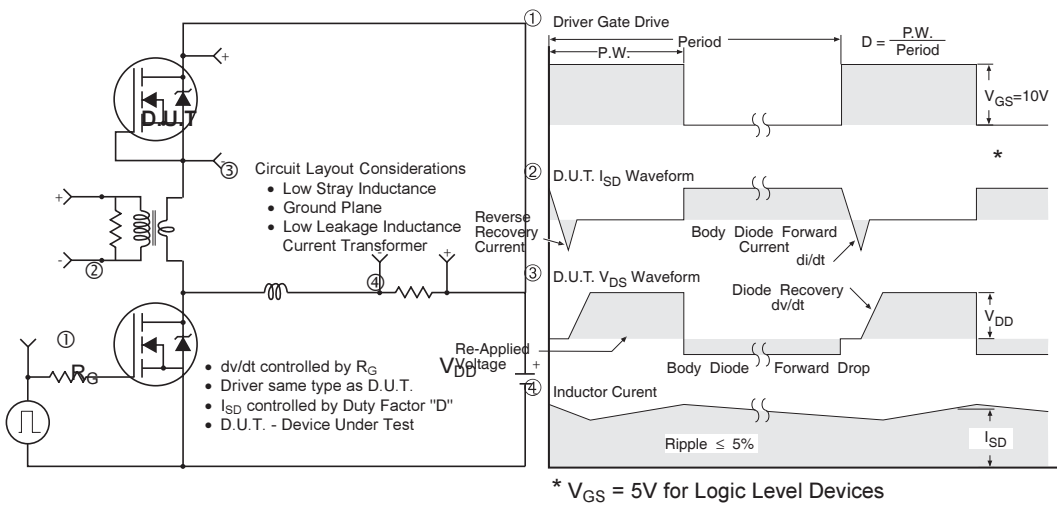


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

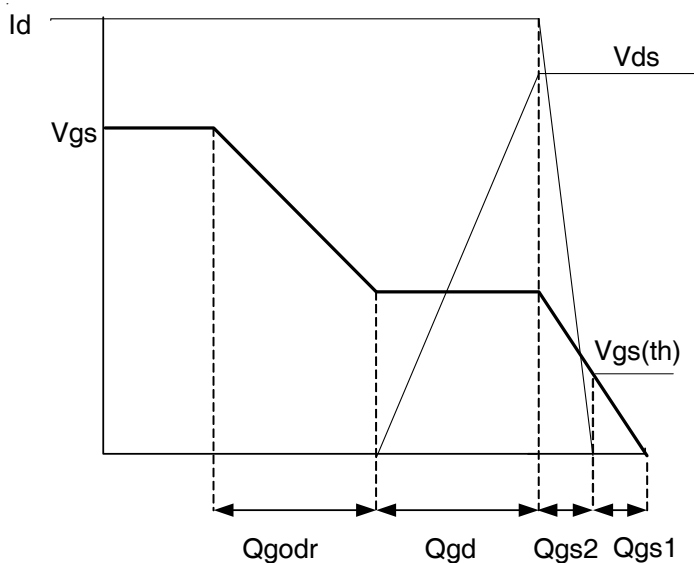


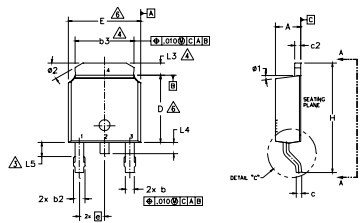
Fig 16. Gate Charge Waveform

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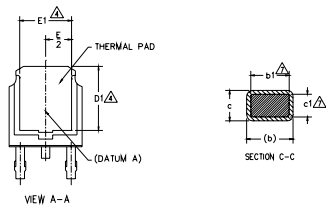
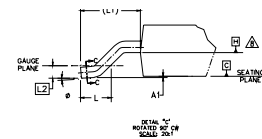
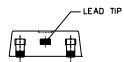


D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
 - 3.- LEAD DIMENSION UNCONTROLLED IN L5.
 - 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
 - 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 - 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
 - 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC	-	.090 BSC	-	
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC	-	.108 REF.	-	
L2	0.51 BSC	-	.020 BSC	-	
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFEEET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

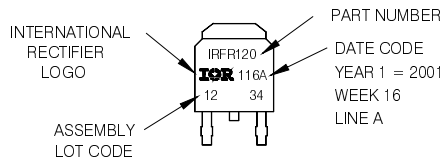
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

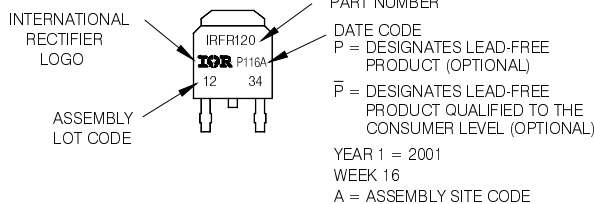
EXAMPLE: THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 1234 ASSEMBLED ON WW 16, 2001 IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position indicates 'Lead-Free'

'P' in assembly line position indicates 'Lead-Free' qualification to the consumer-level



OR



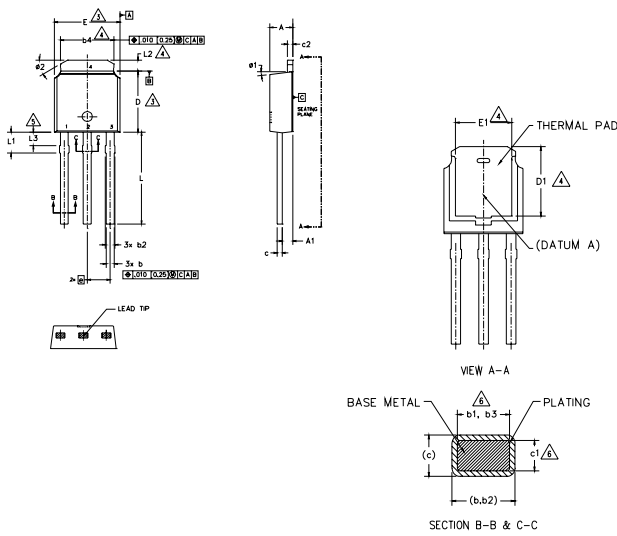
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
 - 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 - 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
 - 5.- LEAD DIMENSION UNCONTROLLED IN L3.
 - 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
 - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
 - 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29	BSC	.090	BSC	
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

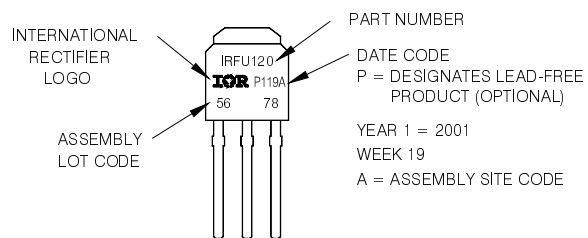
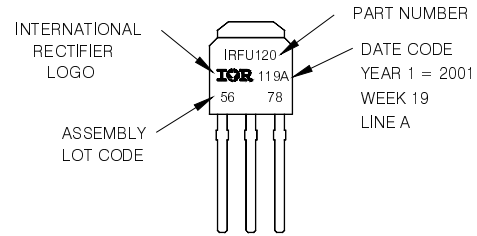
- LEAD ASSIGNMENTS**
- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 2001 IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position indicates Lead-Free'

OR



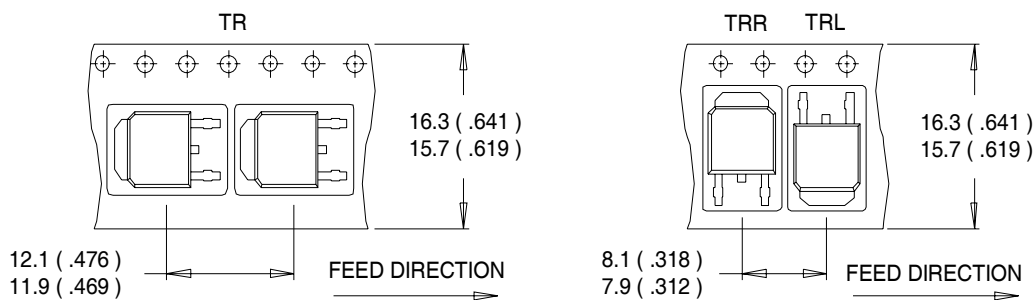
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>
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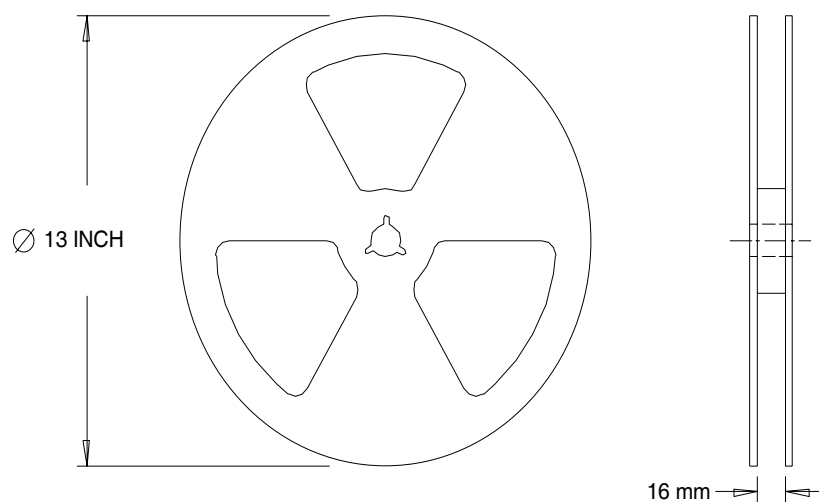
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLR8729PBF	D-PAK	Tube/Bulk	75	
IRLR8729TRPBF	D-PAK	Tape and Reel	2000	
IRLU8729PBF	I-PAK	Tube/Bulk	75	

Qualification information†		
Qualification level	Industrial†† (per JEDEC JESD47F††† guidelines)	
	Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level	D-PAK	MSL 1 (per JEDEC J-ST D-020D†††)
	I-PAK	Not applicable
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>
 †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>
 ††† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.37\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 20\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 50A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material).For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.

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