



# N-Channel NexFET™ Power MOSFET

Check for Samples: CSD16401Q5

### **FEATURES**

- Ultralow Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- SON 5-mm × 6-mm Plastic Package

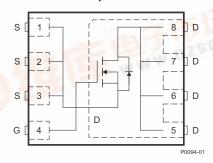
### **APPLICATIONS**

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

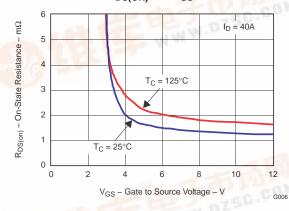
#### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.





### r<sub>DS(ON)</sub> vs V<sub>GS</sub>



#### PRODUCT SUMMARY

$V_{DS}$	Drain-to-source voltage 25			
Qg	Gate charge, total (4.5 V)			
$Q_{gd}$	Gate charge, gate-to-drain	5.2		nC
20.	Drain to source on registence	V <sub>GS</sub> = 4.5 V 1.8		mΩ
r <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = 10 V 1.3		mΩ
V <sub>GS(th)</sub>	Threshold voltage	1.5		V

#### ORDERING INFORMATION

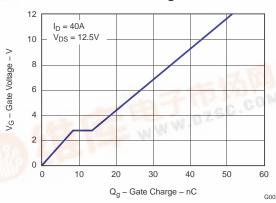
Device	Package	Media	Qty	Ship
CSD16401Q5	SON 5-mm × 6-mm plastic package	13-inch (33-cm) reel	2500	Tape and reel

#### ABSOLUTE MAXIMUM RATINGS

$T_A = 25$	5° <mark>C unless otherwise stat</mark> ed	VALUE	UNIT
V <sub>DS</sub>	Drain-to-source voltage	25	V
V <sub>GS</sub>	Gate-to-source voltage	-12 to 16	V
-	Continuous drain current, T <sub>C</sub> = 25°C	100	Α
I <sub>D</sub>	Continuous drain current <sup>(1)</sup>	38	Α
$I_{DM}$	Pulsed drain current, T <sub>A</sub> = 25°C <sup>(2)</sup>	240	Α
$P_D$	Power dissipation <sup>(1)</sup>	3.1	W
$T_J$ , $T_{STG}$	Operating junction and storage temperature range	-55 to 150	°C
E <sub>AS</sub>	Avalanche energy, single-pulse $I_D = 100 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$	500	mJ

- 1)  $R_{\theta JA} = 40^{\circ}\text{C/W} \text{ on 1-in}^2 (6.45\text{-cm}^2) \text{ Cu } [2 \text{ oz. } (0.071\text{-mm thick})] \text{ on 0.060-inch (1.52-mm) thick FR4 PCB.}$
- (2) Pulse duration ≤300 μs, duty cycle ≤2%

### **Gate Charge**



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### **ELECTRICAL CHARACTERISTICS**

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

	PARAMETER	TEST CONDITIONS	MIN TY	MAX	UNIT
Static C	haracteristics		J		
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	25		V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V		1	μΑ
I <sub>GSS</sub>	Gate-to-source leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = -12 \text{ V to } 16 \text{ V}$		100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.2 1.	5 1.9	V
	Drain-to-source on-resistance	$V_{GS} = 4.5 \text{ V}, I_D = 40 \text{ A}$	1.	3 2.3	mΩ
r <sub>DS(on)</sub>	Drain-to-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$	1.	3 1.6	mΩ
9 <sub>fs</sub>	Transconductance	$V_{DS} = 15 \text{ V}, I_{D} = 40 \text{ A}$	16	3	S
Dynamic	Characteristics				
C <sub>ISS</sub>	Input capacitance		315	4100	pF
C <sub>OSS</sub>	Output capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 12.5 V, f = 1 MHz	253	3300	pF
C <sub>RSS</sub>	Reverse transfer capacitance		17	5 230	pF
$R_g$	Series gate resistance		1.	2 2.4	Ω
Qg	Gate charge total (4.5 V)		2	1 29	nC
$Q_{gd}$	Gate charge, gate-to-drain	V 42.5.V ID 40.A	5.	2	nC
Q <sub>gs</sub>	Gate charge, gate-to-source	V <sub>DS</sub> = 12.5 V, ID = 40 A	8.	3	nC
Qg(th)	Gate charge at Vth		4.	3	nC
$Q_{OSS}$	Output charge	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$	5	5	nC
t <sub>d(on)</sub>	Turnon delay time		16.	Ĝ	ns
t <sub>r</sub>	Rise time	$V_{DS} = 12.5 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 40 \text{ A}$	3	0	ns
t <sub>d(off)</sub>	Turnoff delay time	$R_G = 2 \Omega$	2	0	ns
t <sub>f</sub>	Fall time		12.	7	ns
Diode C	haracteristics	•		•	
$V_{SD}$	Diode forward voltage	I <sub>S</sub> = 40 A, V <sub>GS</sub> = 0 V	0.8	5 1	V
Q <sub>rr</sub>	Reverse recovery charge	$V_{DD} = 15 \text{ V}, I_F = 40 \text{ A}, di/dt = 300 \text{ A/}\mu\text{s}$	7.	2	nC
t <sub>rr</sub>	Reverse recovery time	$V_{DD} = 15 \text{ V}, I_F = 40 \text{ A}, di/dt = 300 \text{ A/}\mu\text{s}$	4	5	ns

### THERMAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

( · A = - ·					
	PARAMETER	MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Thermal resistance, junction-to-case <sup>(1)</sup>			1.1	°C/W
R <sub>A.IA</sub>	Thermal resistance, junction-to-ambient (1) (2)			50	°C/W

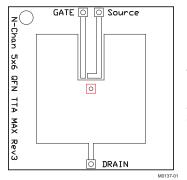
<sup>(1)</sup> R<sub>θJC</sub> is determined with the device mounted on a 1-inch (2.54-cm) square, 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.060-inch (1.52-mm) thick FR4 board. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.

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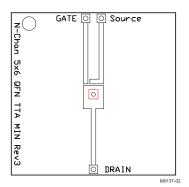
<sup>(2)</sup> Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of 2-oz. (0.071-mm thick) Cu.



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Max  $R_{\theta JA} = 50^{\circ} C/W$  when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 121^{\circ} C/W$  when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

### TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

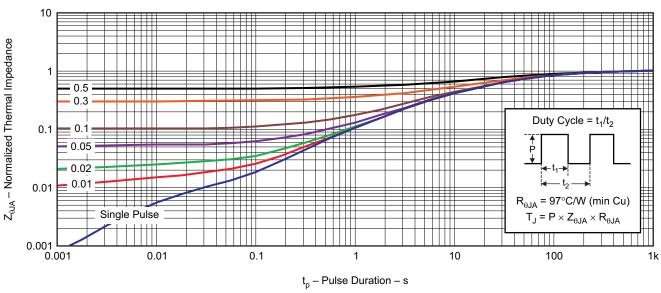


Figure 1. Transient Thermal Impedance

G012



### TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

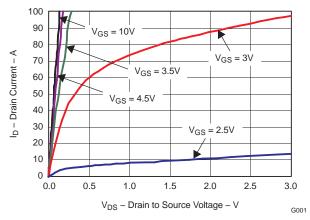


Figure 2. Saturation Characteristics

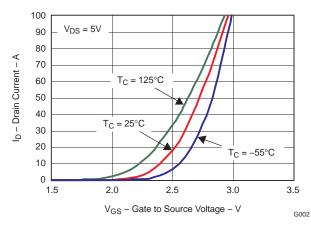


Figure 3. Transfer Characteristics

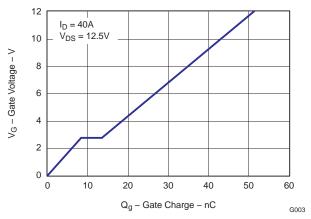


Figure 4. Gate Charge

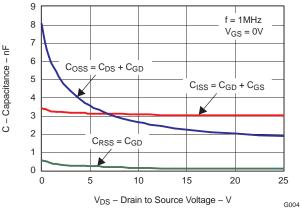


Figure 5. Capacitance

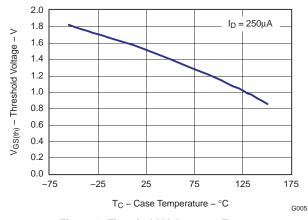


Figure 6. Threshold Voltage vs. Temperature

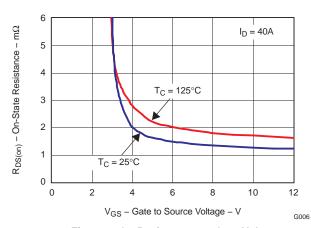


Figure 7. On-Resistance vs. Gate Voltage

**STRUMENTS** 

### TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

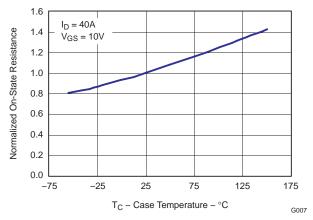


Figure 8. On-Resistance vs. Temperature

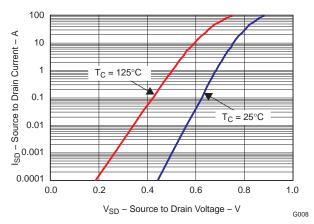


Figure 9. Typical Diode Forward Voltage

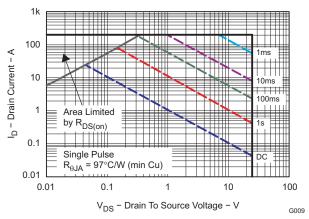


Figure 10. Maximum Safe Operating Area

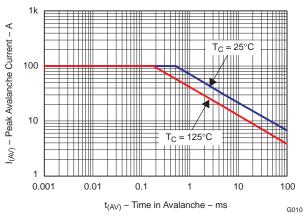


Figure 11. Single-Pulse Unclamped Inductive Switching

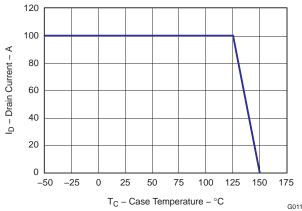
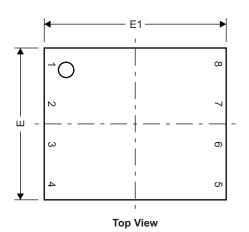


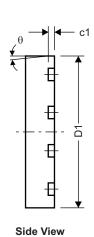
Figure 12. Maximum Drain Current vs. Temperature

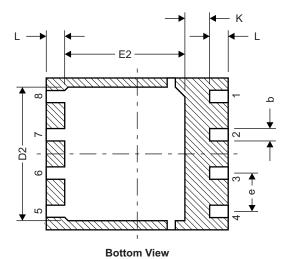


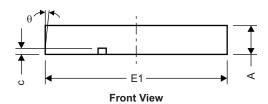
### **MECHANICAL DATA**

## **Q5 Package Dimensions**









M0140-01

DIM	MILLIM	ETERS	INC	HES
DIW	MIN	MAX	MIN	MAX
Α	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
С	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
е	1.27	TYP	0.0	050
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00			



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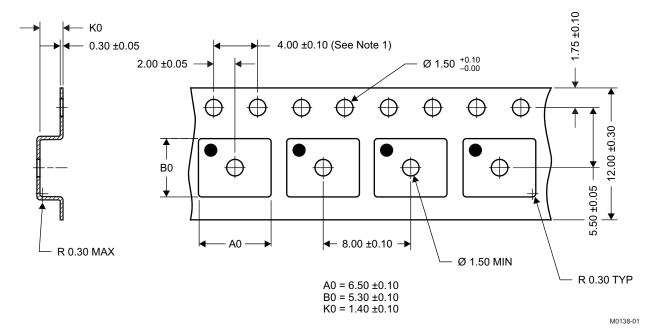
#### SLPS200A -AUGUST 2009-REVISED SEPTEMBER 2010

Recommended PCB Pattern							
F6 - F1	F7						
84 F10	M0139-01  4  7  4  8  8  8  8  9  1  1  1  1  1  1  1  1  1  1  1  1						

X
8
0
0
8
6
7
1
8
6
7
0
,

For recommended circuit layout for PCB designs, see application note SLPA005 - Reducing Ringing Through PCB Layout Techniques.

### **Q5 Tape and Reel Information**



#### Notes:

- 1. 10 sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
- 3. Material:black static dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket
- 6. MSL1 260°C (IR and Convection) PbF Reflow Compatible



### **REVISION HISTORY**

CI	Changes from Revision Original (August 2009) to Revision A						
•	Deleted environmental bullets from Features list	1					
•	Deleted Package Marking Information section at the end of the data sheet	7					



### PACKA

### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Pea
CSD16401Q5	ACTIVE	SON	DQH	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-2600

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps